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Chapter

7

Printed Circuit Board Fabrication

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7.1 Introduction

Of all of the elements of an electronic system, perhaps none is more essential than the printed circuit board. At the same time, however, no other element seems to be so underappreciated. Prior to the advent of the printed circuit, electrical interconnections between components were made in a point-to-point fashion. This was both very time consuming and highly error prone. The printed circuit offered a way to make ordered interconnections between components while radically reducing the potential for error by allowing faithful reproduction of the circuit using a combination of lithographic and etching methods. It has been that way virtually ever since.

Today, it can be easily argued that the printed circuit is the foundation of almost all electronic products and systems and a technological marvel of immense dimensions, but it is commonly overshadowed but the more glamorous integrated circuit. Interestingly, the printed circuit is likely to have served as the inspiration for the inventors of the IC, given that the concepts described by both Jack Kilby and Robert Noice appear to have borrowed from printed circuit manufacturing methods. Kilby had, in fact, joined pioneering printed circuit company, Centralab, in Milwaukee, WI, in 1947 after leaving college. Figure 7.1 shows first Kilby's IC. Regardless, the printed circuit will assuredly remain an indispensable element of electronics for many years to come.

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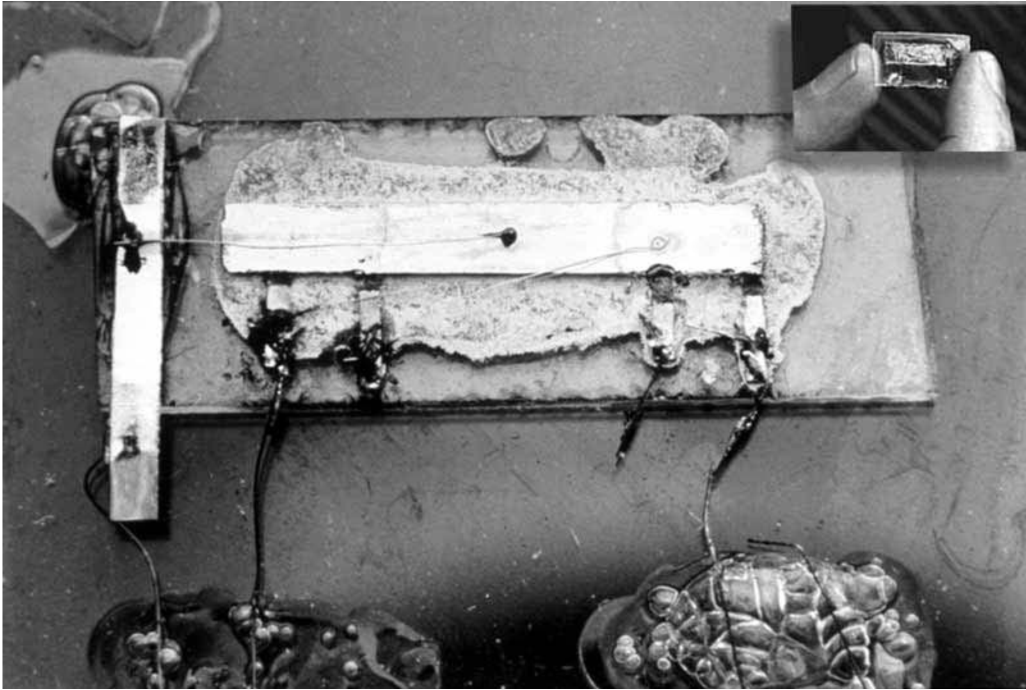

Figure 7.1 Jack Kilby's original integrated circuit. *(Photo courtesy of Texas Instruments.)*

The purpose of this chapter is to give the reader an overview of this important electronic interconnection technology. Attention will be given to the materials and processes used in their construction and, in addition, most of the many forms of printed circuits will be reviewed and described. Rigid, flexible, multilayer, metal core, and molded boards are among the types that will be covered. However, no attempt will be made to provide and exhaustive look at printed circuit technology. Rather, it is intended and hoped that the reader will be provided with a sufficient level of understanding of the printed circuit technology to feel confident and comfortable moving through the technological forest of electronic interconnection substrates. The reader will be shown many different constructions and be provided with enough information on process to have, hopefully, a good understanding of how PCBs are made, from the very simple to the very complex. Finally, it is hoped that the reader will be able to use this information to make informed choices relative to future interconnection needs.

7.1.1 Background and history

The origins of the printed circuit have been variously traced to either the late nineteenth century or the early twentieth century. That period marked the rise of useful inventions predicated on the use of electrons and wire. The telegraph, the telephone, and the radio are the hallmark inventions of the period.

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A point of entry from the wiring perspective came in 1903 from the inventor, a German by the name of Albert Hanson. Hanson conceived of a method of producing conductive metal patterns on a dielectric by cutting or stamping copper or brass foil patterns and laminating or bonding them in paraffin paper. Although only two metal layers were described, it is easy to envisage that multiple layers could be produced using his concept.

The American patron saint of inventors, Thomas Edison, also took a turn at circuit processing invention at the prodding of this then assistant, Frank Sprague, later of Sprague Electric Company fame. Sprague had challenged Edison in 1904 with finding ways to pattern conductors on linen paper. Edison responded with a number of different ideas, including two that are, at least in spirit, in use today. These methods include a crude version of today's polymer thin film technology and patterning of silver salts to be reduced in situ, which, in concept, resembles today's additive processing.

Print-and-etch methods commonly used today in circuit production can trace their roots to methods described by inventor Arthur Berry in 1913, wherein he used the method to create resistive heaters (British patent 14,699). Another method of note was conceived of by Max Schoop, who developed a method of flame spraying of metal through a mask to create circuit patterns on a dielectric base (U.S. patent 1,256,599). Electroplating of the circuit pattern appears to have been the invention of Charles Ducas, in 1927 (British patent 1,563,731). The method had the added advantage of allowing release and transfer of the circuits from the base onto which they were plated. The basic concept of transferring circuit patterns has merit and has been visited since that time by others who made improvements to the concept.

Paul Eisler is the next inventor of note in the pantheon of printed circuit technology pioneers. The self-proclaimed "father of the printed circuit," Eisler made significant contributions to printed circuit technology. Eisler's innovations spearheaded the allies' effort to make more reliable proximity fuses for munitions. The advantages offered by the PCB are credited with causing the destruction of large numbers of V2 rockets and thus ending the terror bombing of England. Examples of one of his circuit concepts are illustrated in the patent drawing shown in Fig. 7.2.

After World War II, printed circuit technology began to unfold in earnest as investigation into defining and refining their manufacturing methods began to grow and expand. The following paragraph gives and indication of how diverse the approaches were.

> ...circuits are defined as being printed when they are produced on an insulated surface by any process. The methods of printing circuits fall in six main classifications: *Painting*—Conductor and resistor paints are applied separately by means of a brush or a stencil bearing the electronic pattern. After drying, tiny capacitors and subminiature tubes are added to complete the unit. *Spraying*—Molten metal or paint is sprayed on to form the circuit conductors. Resistance paints may also be sprayed. Included in this classification are an abrasive spraying process and a die casting method. *Chemical deposition*—Chemical solutions are poured on the surface originally covered with a stencil. A thin metallic film is precipitated on the surface in the form of the desired electronic circuit. For conductors the film is elec-

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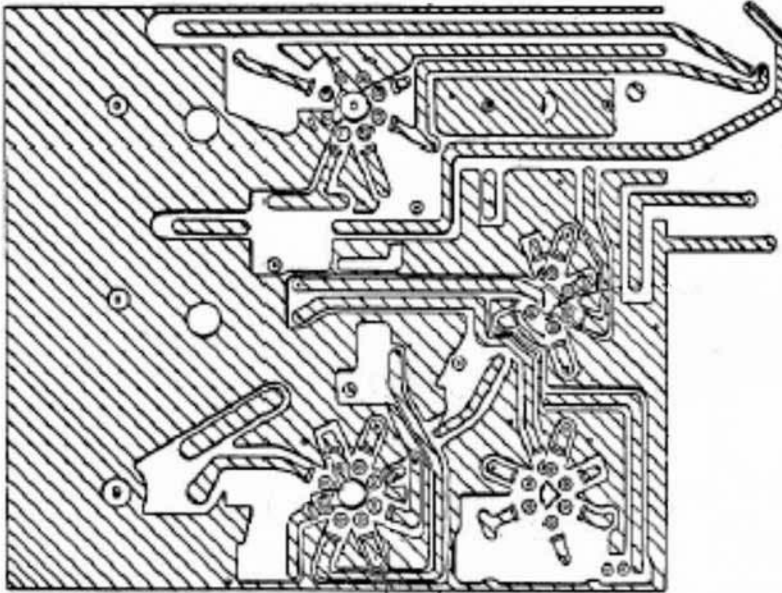

Figure 7.2 Example of an early printed circuit design layout. Note that components mainly had leads in a circular pattern consistent with vacuum tubes and the early TO packages.

> troplated to increase conductance. *Vacuum processes*—Metallic conductors and resistors are distilled onto the surface through a suitable stencil. *Die stamping*—Conductors are punched out of a metal foil by either hot or cold dies and attached to an insulated panel. Resistors may also be stamped out of a specially coated plastic film. *Dusting*—Conducting powers are dusted on, either with a binder or by an electrostatic method.... Principal advantages of printed circuits are uniformity of production and the reduction of size, assembly and inspection time and cost, line rejects and purchasing and stocking problems....

The forgoing paragraph was from a publication titled *Printed Circuit Techniques,* written by Cledo Brunetti and Roger W. Curtis and published 1947 by the U.S. government. Clearly, those involved in the early manufacture of printed circuits were very clever. Few stones, it seems, were left unturned in their efforts to find cost-effective ways of delivering patterned circuits to the nascent electronics industry.

Up to this point in this review, most of the circuit concepts described have been single sided; however, the drive for more functionality in an electronic assembly translated naturally to greater complexity and more wiring. Two metal layers became the next requirement. Interconnection between the two sides was accomplished initially by simple but slow methods. The z-wire interconnection served the purpose originally (see Fig. 7.3) but was supplanted by the use of eyelets (the same method as is used to reinforce lace holes in shoes), which were easier to use. However, as hole counts rose, there was a need to improve productivity in making side-to-side interconnection, and the plated-through hole concept was brought into practice.

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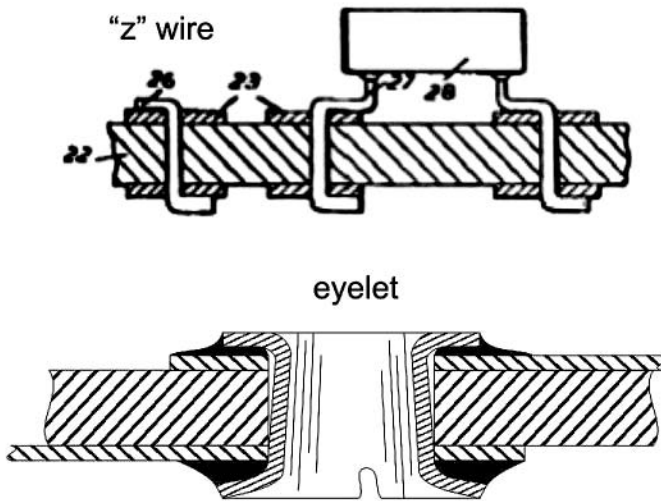

Figure 7.3 Before plated-through hole technology was developed, through-hole connections were made by wires soldered to lands on both sides of the PCB as indicated by the drawing from an early patent (top).

The multilayer board was the next important milestone on the path of printed circuit innovation. Original concepts such as the one illustrated in Fig. 7.4 had layers of circuitry being laminated to prefabricated double-sided circuits, with access being provided by larger holes in the outer layers. The plated-through hole multilayer circuit followed as a natural extension, and the multilayer circuit was later married to the flexible circuit to create the rigid flex circuit. In the time since the early days of printed circuit technology, there has been a steady stream of improvements to the fundamental technology, and it is safe to say that there will be many more improvements in the years ahead. Some potential directions are discussed at the end of this chapter.

7.2 Materials of Construction for Printed Circuit Laminates

Rigid printed circuit laminates normally consist of three fundamental elements,

1. A reinforcement, such as glass cloth, paper, or other material
2. A resin
3. A conductive or catalytic layer

Each of these element serves a specific purpose. Generally, as laminate thickness increases, heavier glass cloths or reinforcements are commonly used, and the resin content in the laminate decreases. Because laminates are commonly exposed to high temperatures both in assembly and use, many laminate mate-

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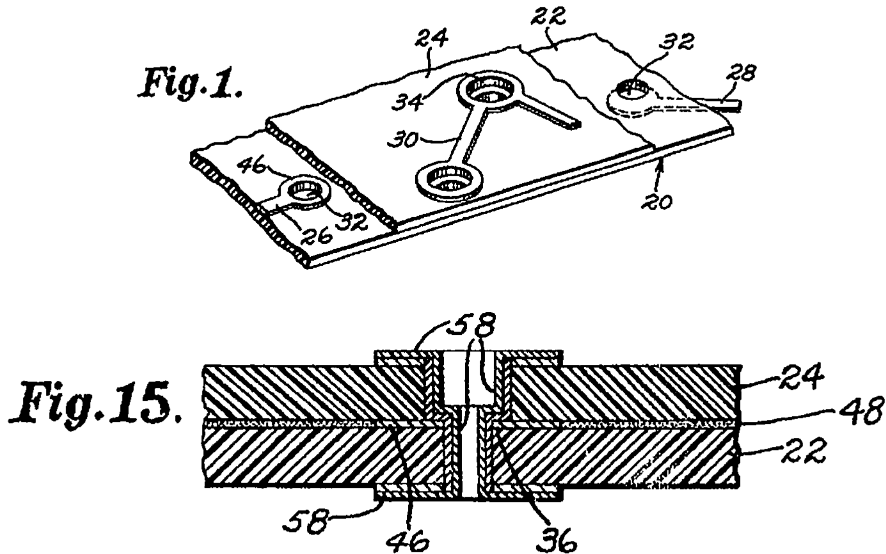

Figure 7.4 This early multilayer circuit patent used holes of different sizes to facilitate making plated-through hole connections.

rials have been engineered to roughly match the thermal expansion rate of copper. This minimizes any potential for warping in plane, which can cause problems in assembly and possibly result in reduced reliability of the plated-through hole or solder joints on the PCB.

Laminates can be made with varying resin-to-glass ratios, depending on the performance needs of the finished product. Specifically, the glass-to-resin ratio of a laminate has a direct effect on dielectric constant, with higher resin contents resulting in lower dielectric constant being obtained. However, laminates with higher resin content tend to have higher coefficients of thermal expansion (CTEs) in the z-axis and lower dimensional stability. On the other hand, if resin content is too low, weave exposure and a phenomenon called *measling* may result. In the past, this condition has been proven to be a largely cosmetic defect, but it is a concern, because it is an indication that either the resin coating or the lamination process is not in full control. Moreover, as the electronics industry moves to higher frequencies, the need for higher consistency in the laminate product is of great importance to both design and performance.

7.2.1 Reinforcements

Reinforcements are the conceptual and literal foundation of a laminate, and they provide important mechanical properties. These are the materials that,

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when coated with resin, become the individual laminae or "building blocks" of the finished laminate. Although it is possible to employ a wide variety of different materials as reinforcements, only a very limited number of choices are commonly used in printed circuit laminates.

The reinforcement serves several different functions. For example, it imparts important mechanical properties such as strength and rigidity. The reinforcement also provides the important attribute of the dimensional stability required for accurate manufacture and assembly. Electrical properties of the laminate are also affected by the reinforcement choice. The effect is not only in terms of the electrical properties of reinforcement itself; it also changes as the ratio of resin to reinforcement is altered. Finally, because they are normally less expensive than the resins with which they are combined, reinforcements also help keep cost of the laminate in line with customer expectations or demands.

The following is a review of some of the more common reinforcements used in the construction of printed circuit laminates.

7.2.1.1 Paper. Paper-based reinforcements have been used in the construction of laminates for a wide variety of products for many years and have proven to be a valuable material for use in the manufacture of printed circuit laminates. Paper is easily mass produced, and thus it is not surprisingly one of the lowest-cost options among reinforcements. One clear disadvantage of paper-based laminates is that they are much more difficult to make fireproof.

7.2.1.2 Glass fiber. Glass fibers are one of the most universally employed reinforcements for resin-based laminates. Glass fibers are an excellent choice because of the good mix of electrical and mechanical properties they exhibit. Glass fibers, for example, are not only excellent insulators, they also have the kind of physical and mechanical properties that are required to supply the strength and dimensional stability required for manufacture, assembly, and component support in use. A number of different types of glass formulations can be used to create the glass fibers. These are given letter designators. E-type glass is the most commonly used in laminates for printed circuits; however, D-type glass is used in some applications for its lower dielectric constant, and S-type glass is used in applications demanding higher strength.

Glass fibers can be employed in one of two fashions, either as a woven cloth or as a chopped glass fiber based paper (see Fig. 7.5). Both forms of glass reinforcement are used, but, of the two, woven glass cloths are by far the most common. While the potential number of choices of glass cloth is quite substantial in terms of the different fiber diameters, yarn construction, and weave, the number actually used in laminate manufacture is, fortunately, rather small. Only a few different types of glass cloth see any significant use; these are characterized in Table 7.1.

7.2.1.3 Others. Many other specialty materials have been used to reinforce printed circuit laminates, including such exotic materials as quartz cloth and

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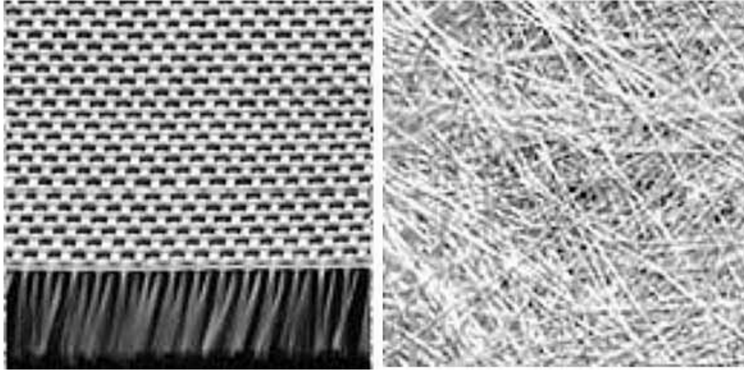

Figure 7.5 Glass cloths for reinforcing laminates can be either woven or a mat of chopped fibers as shown above.

TABLE 7.1 Characteristics of Selected Electronic-Grade Glass Cloths

Glass fabric style	Yarns per cm	Weight, g/m^2	Thickness, μm
104	~24 × 20	19.7	30
108	~24 × 19	48.5	51
112	~16 × 15	71.2	81
116	~24 × 23	107	102
2112	~16 × 15	71.6	76
2116	~24 × 23	107	102
7628	~18 × 13	203	173
7642	~18 × 8	232	279

aramid fibers. Aramid fibers have proven especially useful in applications wherein a low in-plane expansion rate is desired. These materials actually have a negative in-plane expansion rate, which helps offset the normally high expansion rate of the resin; however, this benefit is offset by the material's high z-axis expansion.

Other unusual reinforcements can and have been used. Graphite is an example of a nontraditional reinforcement. However, it requires special care in design and use, because it is conductive.

7.2.2 Organic resins

Organic resins are the second key element of a laminate. The resin serves as a binder to hold the reinforcements together and impart important electrical properties to the laminate. Resins used for electronic-grade laminates are gen-

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erally relatively low in their dielectric constant and loss tangent, which are key properties in electronic design, especially in high-performance applications. The resin system also establishes the thermal performance limits of the laminate. This is a matter of increasing importance as some companies prepare to convert to lead-free solders, which have melting temperatures up to 40°C higher than traditional solders. Flame retardants are commonly added to the resins to assure that the laminates will not support combustion and will meet Underwriter's Laboratories specification 94-V0.

7.2.2.1 Phenolics. Phenolics are among the longest used and best known of general-purpose thermosetting resins. Although their performance is limited, they have proven quite suitable for electronic-grade laminates. Phenolics are the lowest-cost resin used for laminates, and many consumer electronics are fabricated using these materials.

7.2.2.2 Epoxies. Epoxies are the most common resin materials, and they are combined with glass cloth to produce laminates. As compared to other laminate materials, epoxies offer advantages in availability and relative ease in processing. The many different types and blends of epoxies provide a wide range of selection in terms of applications and soldering processes; epoxies with a T_g (glass transition temperature) from 110 to 120°C up to 180 to 190°C are available from most laminate suppliers. However, the most commonly used are in the range of 135 to 145°C. There are also some low-loss, low-dielectric-constant epoxy materials in development that are expected to have a T_g in the rage of 210°C.

7.2.2.3 Polyimides. Polyimides are among the highest-performance resins used in the manufacture of printed circuit laminates. These materials, with glass transitions in the range of 260°C, can withstand very high temperatures for extended periods, making them a good choice for applications wherein high temperatures are experienced or the components used are high-wattage devices. The military also has special interest in high-temperature materials, as they make any required work and repair easier.

7.2.2.4 Others. A number of other resins are useful for creating laminates, such as cyanate esters and bismalamide triazine (BT). These products are seeing application in unique and special applications. For example, BT resins are proving very popular for the manufacture of organic laminate-based packages for integrated circuits. Liquid crystal polymers are also seeing greater levels of interest for certain types of applications because of their good combination of electrical and mechanical properties coupled with their very good dimensional stability.

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7.2.3 Flexible (unreinforced) laminates

Flexible circuits are a special subset of printed circuit manufacture and require their own special laminates. These materials normally consist of a base film, adhesive, and copper foil; however, there is increasing interest in adhesiveless laminates. The materials for these laminates tend to be thermoplastic in nature, which makes them better suited to flexing without fracture and failure. The adhesives, when used to create flex circuit laminates, are generally formulated to be more flexible than traditional thermoset resins. There are two basic resin systems employed in flex circuit manufacture: polyester and polyimide; however, a number of materials of intermediate performance and price have seen use. One example of note is polyethylene naphthalate (PEN).

7.2.3.1 Polyester. Polyester is a low-cost resin that is used in a substantial number of electronic products. Common examples are keyboards and printer cables. Polyester is used with both copper and polymer thick film circuits. The major limitation for polyester is related to its thermal performance. Because of its low melting temperature, it is generally considered unsuitable for soldering; however, this can be addressed by careful engineering. Major OEMs such as TI and Kodak have developed methods for special applications that require soldering to polyester, and some manufacturers have specially developed tools to address the problem.

7.2.3.2 Polyimide. Polyimide is the choice for most flex circuit applications because of its excellent thermal performance and its good electrical and mechanical properties. It also exhibits reasonable dimensional stability, which facilitates circuit manufacture and assembly. This material is also being used extensively in the creation of IC packages. One limitation of polyimide is the fact that it tends to absorb moisture, which can be a concern when soldering.

7.2.3.3 Special materials. A wide range of niche substrate laminate products have been developed in support of special printed circuit manufacturing methods. An example of such a product is resin-coated copper (RCC). This material is used for high-density buildup technologies, which are discussed later in this chapter.

7.2.4 Foils

Metal foils are commonly laminated to resin composites to complete the raw material needed for printed circuit manufacture. Many different foils are potential candidates for the creation of a metal-clad laminate, but copper is the most common because of its excellent electrical properties and its general ease of processing and amenability to solder assembly. Thinner foils are generally

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used by the printed board manufacturer for "fine-line" designs to reduce the amount of undercutting of circuit conductors that occurs during the etch operation and meet the requirements of high-density printed circuits for flip-chip and chip-scale packages.

Copper foils can be created in one of two ways: mechanical rolling and deposition. In the area of deposition, the potential methods include electrodeposition, electroless deposition, vapor deposition, and sputtering. The first of these methods is the one most commonly used to manufacture copper foil for printed circuit laminates. The other methods are generally used to deposit foil directly on the laminate without the aid of a lamination process. Electrodeposition and electroless deposition employ wet chemistry to deposit metals, whereas vapor deposition and sputtering are dry deposition methods for metal and are carried out in a vacuum. Table 7.2 lists the designations for the most common types of copper foil as called out by IPC-MF-150.

TABLE 7.2 Copper Foil Designations*

Copper foil type	Number	Designator	Description
Electrodeposited (E)	1	STD–Type E	Standard electrodeposited
	2	HD–Type E	High-ductility electrodeposited
	3	THE–Type E	High-temperature elongation electrodeposited
	4	ANN–Type E	Standard electrodeposited
Wrought (W)	5	AR–Type E	As rolled-wrought
	6	LCR–Type E	Light cold rolled-wrought
	7	ANN–Type E	Annealed rolled-wrought
	8	LTA–Type E	As rolled-wrought, low temp. annealable

*Copper foil is available in both electrodeposited and wrought forms. The IPC standard for copper foils, IPC-MF-105, has broken out these foils into eight different types, as described above.

7.2.4.1 Electrodeposited. Electrodeposited foil is most commonly used for rigid printed circuit laminates. The foil is plated onto polished stainless steel or titanium drums that are negatively charged and rotated slowly through a plating bath. The thickness is controlled by the rate of rotation, the current density, or a combination of the two. Figure 7.5 illustrates the process.

The surface is commonly provided with a roughening treatment to increase the surface area and improve the foil's peel strength. This can be important for surface mount components of large mass, lest they pull away from the surface as a result of shock and vibration. The thickness of the treatment can, however, influence processing and might limit the minimum feature sizes that can be reliably etched. This is discussed in more detail later in this chapter.

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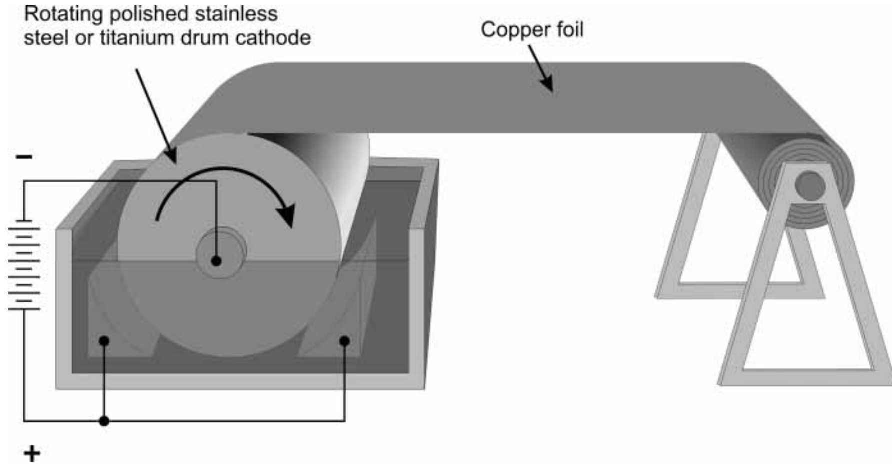

Figure 7.6 Electrodeposited copper foil is the type most often used in circuit manufacture. The foil is produced by rotating a highly polished drum of passivated stainless steel or titanium in a copper plating solution with current applied. The rate of rotation controls the copper thickness.

7.2.4.2 Rolled. Rolled copper foil is most commonly used in the manufacture of flexible circuits. Wrought and annealed foils have proven excellent for use in situations wherein the foil must be bent or formed. Figure 7.7 shows the layout of the rollers for a foil rolling mill.

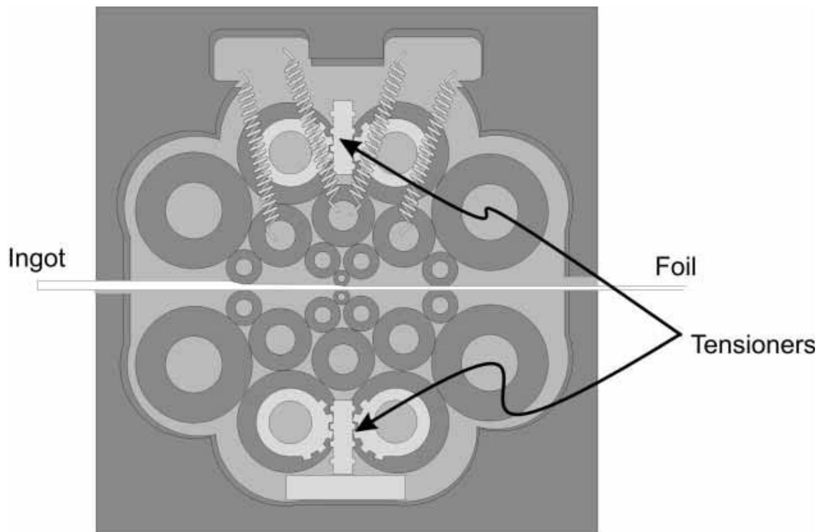

Figure 7.7 Rolled copper foil is manufactured from ingots of copper successively rolled down to the desired thickness in specially designed rolling machines such as shown above.

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7.2.4.3 Conductive inks. Conductive inks are among the oldest methods of creating printed circuits and are largely responsible for giving the technology its name. The technology is used for both high- and low-end products. For example, with ceramic substrates, it is used to create hybrid circuits and is fired in an oven to create circuits of high conductivity. For lower-end products, such as keyboards and some low-cost electronic devices, the curing is done at low temperatures and using low-cost materials for substrates such as polyester film. Other applications include migration protection for silver conductive ink, low-voltage circuits, shield areas, and heating elements.

The inks are generally combinations of resins and conductive fillers such as powdered silver. The conductivity can be modified to create resistors of varying values by the addition of more resistive fillers such as carbon or graphite powders.

Carbon-based conductive inks are easy to screen through properly designed screen fabrics. A coating thickness between 25 and 30 μm will provide sheet resistance between 14 and 20 Ω/❑. The inks are one-part systems and are thermally cured. Newer versions are IR curable, which greatly reduces the processing cycles.

The inks must be resistant to hot-air leveling and other soldering processes. It is critical that the conductive properties of the ink not change appreciably after any thermal excursion.

7.3 Laminate Types for PCBs

Laminates used in PCB manufacture, whether rigid or flexible, are created in two primary forms: single-clad and double-clad laminates. They are also produced in a number of different thicknesses to facilitate the manufacture of PCBs with different thickness requirements and for the construction of multilayer PCBs. When used in the manufacture of multilayer circuits, the laminate is commonly referred to as a *core material*.

7.3.1 Single-clad laminates

Single-clad laminates have copper on one side only and are used either for the manufacture of single-sided circuits or for the manufacture of multilayer circuits as an inner layer or, more commonly, as a cap laminate.

7.3.2 Double-clad laminates

Double-clad laminates are essentially identical to single-clad laminates in description and use except that copper is laminated to both sides of the structure.

7.4 Laminate Selection

The selection of a laminate is based on the requirements of the product, both in assembly and use. Ideally, the laminate choice should be made from stan-

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dard structures to avoid delays and potentially costly qualification of new constructions. When several laminates are potential candidates, the choice should be made in favor of the one that has the best balance of properties. Table 7.3 lists some of the different potential criteria for making a selection.

TABLE 7.3 Laminate Selection Criteria

• Coefficient of thermal expansion (CTE)	• Maximum continuous operating temperature
• Electrical properties	• Mechanical strength
• Flame resistance	• Overall thickness tolerances
• Flexural strength	• Reinforcing sheet material
• Glass transition temperature (T_g)	• Resin formula
• Machinability	• Thermal stability

As previously described, laminates come in many different resin and reinforcement combinations. The National Electronics Manufacturers Association (NEMA) and the U.S. military have both devised designators to describe the materials in a shorthand fashion. Table 7.4 provides a list of some of the most commonly used designators for different laminate types, and Table 7.5 provides examples of the applications for different constructions.

7.5 Laminate Material Preparation

The resin and reinforcement material are combined to create the raw material used for the creation of a laminate. The end product is commonly referred to as either *prepreg* or *B-stage*. *Prepreg* is short form for *reinforcement preimpregnated with resin,* and B-stage refers to the fact that the resin is dry to the touch but not fully cured.

This material is created by drawing the reinforcement material through a wet resin bath and then drying it and slightly advancing its state of cure—normally though the addition of heat. The basic manufacturing process is illustrated in Fig. 7.8.

7.5.1 Lamination methods

A lamination process is used to create laminates that can be used for manufacture of printed circuit boards. In lamination, the prepreg or B-stage material is layered, most often between to sheets of treated copper foil. Following lay-up of the material, the material stack is subjected to heat and pressure, and this drives the resin to a fully cross-linked or cured condition wherein it has all of the desired properties. There are several different methods of creating laminate material.

7.5.2 Batch

Batch processing is the simplest and was thus one of the first methods developed for laminate manufacture. In their simplest form, lamination presses for

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TABLE 7.4 Laminate Designators and Descriptions

NEMA designation	Military designation (MIL-P-13949)	Basic construction of laminate
XXXP	–	Phenolic resin with paper reinforcement, heat required for punching
XXXPC	–	Phenolic resin with paper reinforcement, room-temperature punching
CEM–1	–	Composite epoxy laminate, glass cloth outer with paper center
CEM–3	–	Composite epoxy laminate, glass cloth outer with mat glass center
FR–1	–	Similar to XXXP but flame retardant
FR–2	–	Similar to XXXPC but flame retardant
FR–3	PX	Similar to FR–2 but epoxy based and stronger
G–10	GE	Epoxy glass laminates without flame retardant
FR–4	GF	Epoxy glass laminate, flame retardant
FR–5	GH	High-temperature epoxy glass laminate, flame retardant
–	GI	Glass reinforced polyimide resin
–	GP GT, GX, GY	Fluoropolymer resins reinforced with various glass materials woven or mat fiber and having slightly different electrical properties
–	GC	Woven glass cloth with cyanate ester resin
–	GM	Woven glass cloth with bismalimide triazine resin
–	BF	Nonwoven aramid fiber with epoxy resin
–	BI	Nonwoven aramid fiber with polyimide resin
–	SC	Woven S type glass cloth with cyanate ester resin

batch processing consist of a hydraulic ramp and a heated platen, which is pressed against a parallel platen that resists the pressure of the hydraulic ram. It is obviously possible to have several openings and to have all of the platens heated. Heating can be done electrically, by steam, or by hot oil circulated through the platens. The choice is predicated on the temperature required for lamination. Figure 7.9 illustrates the basic process.

7.5.3 Continuous lamination

Continuous lamination is a somewhat self-descriptive method wherein the laminate is produced in a continuous web. The prepreg and foil are fed into a specially designed and manufactured lamination press. There are both economical and technical advantages to such methods; however, there are only a very limited number of suppliers of such products. A conceptual example of continuous lamination is provided in Fig. 7.10.

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TABLE 7.5 Substrate Materials for Electronic Devices*

Type	Composition	General properties	Applications
CEM-1	Epoxy/glass fabric surface, epoxy/cotton paper core	Punchable at room temperature, good electricals but less than polyester, good flex and impact strength	Consumer electronics
CEM-3	Epoxy/glass fabric surface, epoxy/cotton paper core	Punchable but harder than CEM-1, good electricals, suitable for PTH applications	Computers, peripherals, keyboards
FR-4	Epoxy/glass fabric	High flex and impact strength, excellent electrical properties, commonly used for PTH applications	Computers, telecom, military
G-10	Epoxy/glass fabric, non-flame-retardant	High flex and impact strength, excellent electrical properties, excellent dimensional stability	Structural
FR-5	Modified epoxy/glass fabric	Improved hot flex strength compared to FR-4, excellent electricals	Military products
High-performance	Bismalimide triazine (BT), polyimide PTFE (Teflon®), cyanate ester epoxy/PPE (Getek®)	Excellent thermal properties, lower x-y-z CTE, high reliability, excellent electrical properties	Chip interposers, mainframes, telecom, military
Flex	Polyimide, polyester, FEP	High flexibility, high-ductility copper, excellent electrical and thermal properties	Automotive, computers, military, telecom

*SOURCE: IPC.

7.5.4 Vacuum-assisted lamination

Traditional lamination methods can be improved by carrying out the process in a vacuum. The negative pressure facilitates the removal of entrapped air and can improve the quality of the laminate. The reduced pressure created by the vacuum allows for lower lamination pressures to be used with the hydraulic ram.

7.5.5 Vacuum-assisted autoclave lamination

Vacuum-assisted autoclave lamination methods were originally developed for the lamination of complex shapes. The method takes advantage of normal atmospheric pressure by simple removal of air. The effect is the same as seen in vacuum-packaged foodstuffs, whereby the vacuum bag conforms to shape of the materials contained within. The negative pressure is augmented by gas pressure in a pressure vessel. This creates an isostatic or uniform pressure from all directions on the laminate stack and allows for lower lamination pressures to be used.

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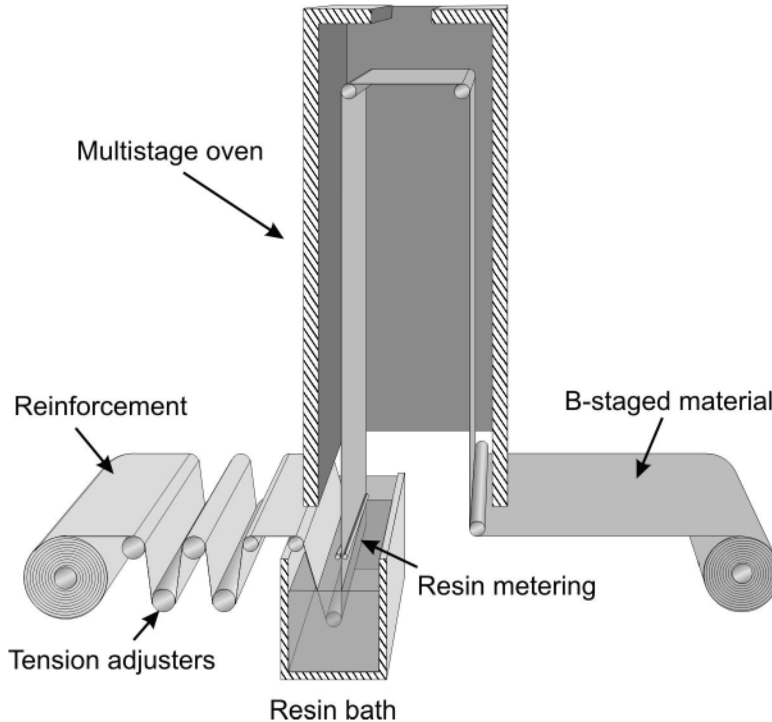

Figure 7.8 Reinforcement materials such as glass cloth are converted into prepreg materials for laminate manufacture by coating them in special resin "treaters." The material is coated with resin and then dried and partially cured in a special oven from which it emerges dry and tack free.

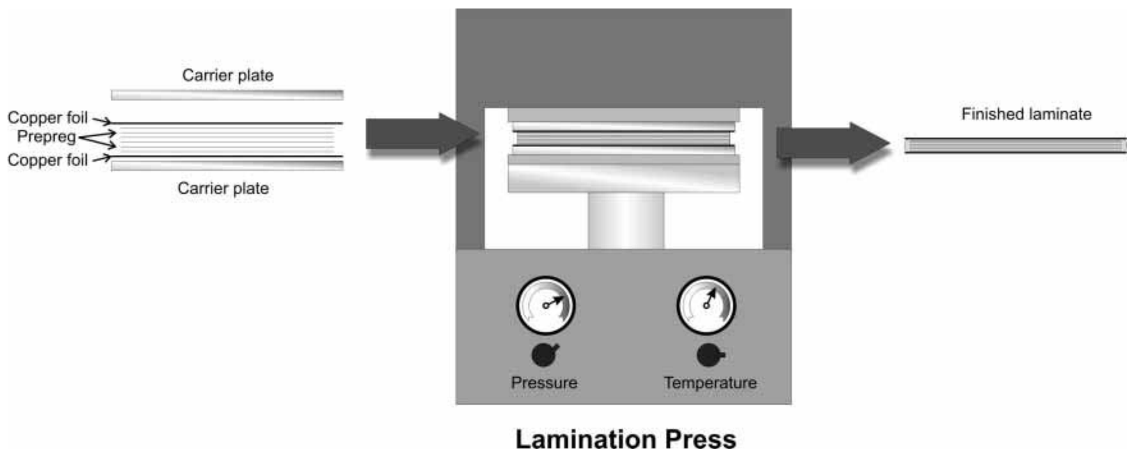

Figure 7.9 Standard laminate manufacture is accomplished by placing plies of B-stage or prepreg between sheets of copper foil and applying heat and pressure.

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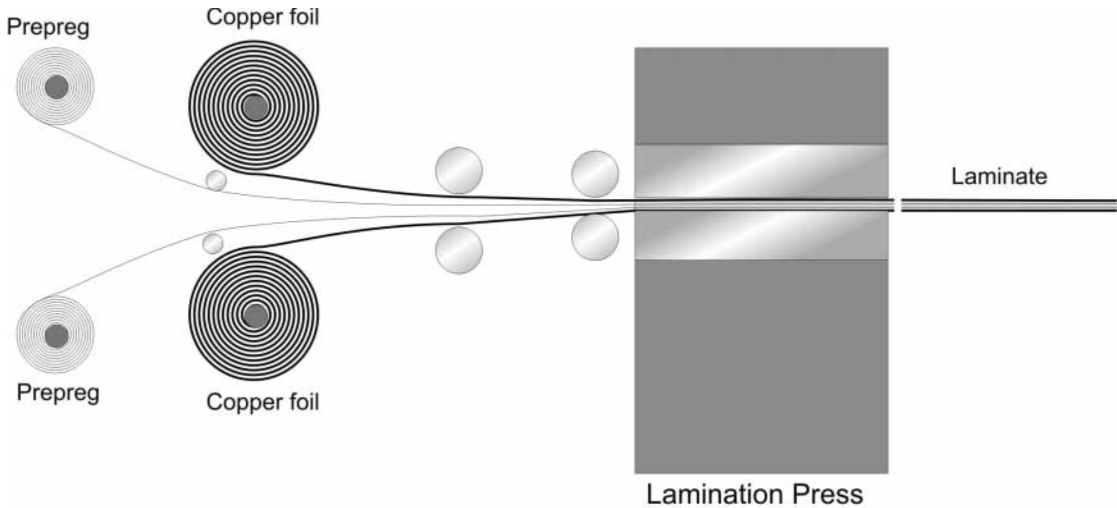

Figure 7.10 Lamination methods have been developed that allow laminates to be manufactured in a continuous fashion. The basic concept is illustrated above.

7.6 Generic Process Overview for a Plated-through Hole Printed Circuit

The processing of printed circuits varies widely. As was indicated in the background section of this chapter, many different approaches to the manufacturing process have been tried and used since PCB technology was first developed. Still, some methods are more common than others. This is because materials, processes, and equipment for PCB manufacturing needed a focal point to create a viable infrastructure. The process description that follows is a somewhat "generic" process. The term "somewhat" is used, because many subtle differences can be employed at each of the process steps described.

This particular section will describe the manufacturing steps for making a plated-through hole printed circuit board using a pattern plating process. Most of the steps described are common for both double-sided and multilayer plated-through hole PCBs. Some alternatives to this process flow are described later in this chapter.

7.6.1 Stacking and pinning

Stacking and pinning is the term used to describe the act of cutting of sheets of copper clad laminate to a common size and the stacking them and pinning them all together to allow all the laminates to be drilled at one time. This is a common method for controlling the cost of drilling.

In the process, of creating the stack a backup material is always included on the bottom and an entry material may be used on top. The purpose of the back up material it to prevent the drill from drilling into the drill bed. The entry material can be one of a number of different materials. For example it can be a

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sheet of 250-µm aluminum foil or an unclad piece of a composite material of similar thickness. The purpose of the entry material is to reduce or eliminate the formation of drill burrs at the hole edge (see Fig. 7.11).

7.6.2 Drilling

The drilling process is one of the more important steps in the manufacture of a printed circuit board. Today most if not all drilling is performed on numerically controlled drill machines. The stacked and pinned laminates are placed onto the drill bed and the pins, which extend beyond the surface of the drill stack, are placed in alignment holes located in the drill bed. The location of the holes serves as a datum for the drill program and all holes are drilled based on their location relative to these alignment pins.

Careful control of the drilling process is required to assure the quality of the final plated through hole. Hole quality is achieved by characterizing the materials in a drill study and by adjusting the in feed rate of the drill bit along with the speed of rotation of the drill bit. Excess time in the hole can cause resin smear, while too fast an in feed rate can break drills or result in rough holes.

7.6.3 Hole preparation and metallization

Hole preparation and metallization are also very important elements in the creation of a reliable plated-through hole PCB. A well plated through hole is highly reliable, but a poorly plated though hole may not be. The hole preparation steps vary from process to process and can be quite extensive. In addition, the metallization may be replaced with a coating of carbon or graphite film. The flow chart in Fig. 7.12 illustrates process flow for typical through hole preparation steps for electroplating. A general over view of hole wall preparation and metallization is provided below.

7.6.3.1 Drill smear removal. No matter how diligent one is in drilling the via, inevitably, the smear remaining on interconnect faces and the less-than-opti-

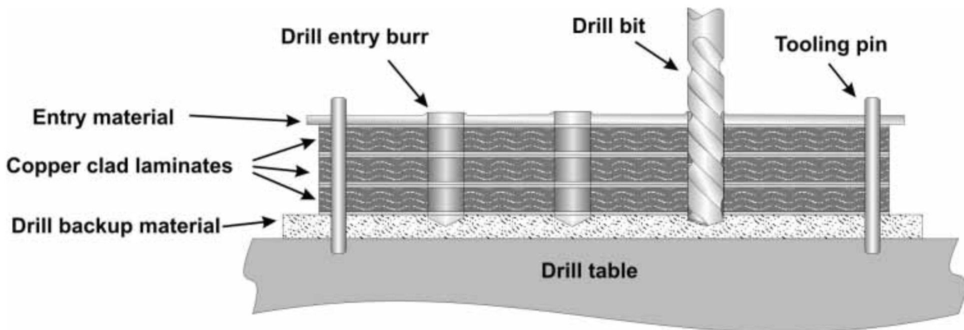

Figure 7.11 Stack drilling greatly improves drill process productivity. The stack height can vary with the material, its thickness, and the drill diameter. Entry and backup materials play very important roles in the drill process.

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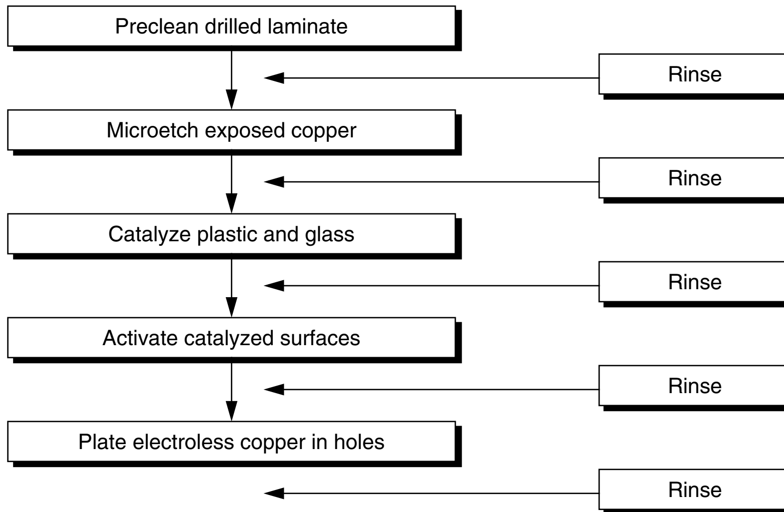

Figure 7.12 Basic electroless copper process flow.

mal topography of the hole wall present a significant challenge with respect to metallization. The goal of the metallization process to produce a continuous-void copper deposit that remains tightly adherent to the hole wall, resin, glass, and copper surfaces. While this sounds like a tall order, setting and controlling the desmear process will ensure that such a goal is met.

With respect to smear removal, several of wet-chemical, and one dry-chemical, methods can be utilized. These are sulfuric acid, chromic acid, alkaline permanganate, and plasma. Alkaline permanganate is by far the method of choice. Plasma, described as a dry chemical desmear process, is often employed when processing materials such as Kapton® or other very difficult-to-process materials such as polyphenylene oxide and epoxy resins. Otherwise, alkaline permanganate processes are very versatile for the majority of the fabricator's needs. The main issue with plasma is that it tends to leave the resin surface somewhat inert. This condition makes it difficult to achieve optimal adhesion of copper metal deposited during the metallization step. Common practice is to follow plasma with alkaline permanganate to impart a reasonable topography on the resin surface.

It is important to keep in mind that different resin types react differently to the alkaline permanganate process. Generally, the higher the degree of cross-linking, the less the degree of resin removal. For example, standard FR-4 (T_g of 140°C) will experience a greater degree of resin removal (measured by weight loss) than a 170-T_g material under the same conditions. Process engineers must adjust parameters of the alkaline permanganate process so as to achieve sufficient resin removal.

7.6.3.2 Metallization. The metallization of PWB substrates (in particular, the metallization that is necessary to render through holes and vias conductive

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and reliable) is one of the critical success factors in PWB fabrication. Numerous experts in the field of plated-through via/blind via reliability have proven that long-term reliability is heavily dependent on the quality and uniformity of the copper deposit within the through hole and blind via.

The data largely support this fact. However, it is often not recognized that, to deposit a uniform copper layer in a blind via or through hole, the metallization process that precedes the application of the electrodeposited copper is the critical success factor. It is the process of making the via conductive that determines whether the subsequent electrodeposited copper will be continuous and adherent to the resin and any supporting structures such as glass or other fiber material. Today, several processes can be utilized to render vias conductive. These are as follows:

1. Electroless copper
2. Palladium-based direct metallization
3. Graphite
4. Carbon black
5. Conductive polymer

Electroless copper. Long considered the standard for metallization, electroless copper process consists of numerous steps. These steps are outlined in Fig. 7.12. The precleaning/conditioning step is required to remove oils, soils, and other contaminants. In addition, the resin surfaces and glass fiber bundles are conditioned to accept the tin-palladium catalyst. The microetch solution removes oxides from the copper surfaces and, in particular, the copper interconnects and the capture pads. This step is required to promote copper-to-copper adhesion to the critical interconnect interfaces such as the interlayer post or capture pad of a blind via. The predip is designed to minimize drag-in of copper to the tin-palladium activator. The palladium acts as a catalyst for the electroless copper plating process. Employing a complex chemistry (see Table 7.6), which normally utilizes formaldehyde as a reducing agent, a thin coating of copper is deposited on hole walls, interconnects, and, in the case of blind vias, the capture pad. However, a by-product of the electroless copper, hydrogen gas, is believed to interfere with the complete and uniform deposition of the copper. All chemical steps and rinses for the electroless copper process must be controlled. The process manual, detailing optimal operating conditions and chemical parameters, must be strictly followed.

The three most critical defects that manifest themselves at this stage are

1. Voids on the glass, resin, or both
2. Hole wall pull-away, whereby the plated copper fails to adhere to the hole wall
3. Interconnect defect, also known as *post separation*

Direct plate. Direct plating onto a palladium seed layer is a viable alternative to electroless copper. In the basic process, the palladium seed layer is of suffi-

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TABLE 7.6 Electroless Copper Bath Constituents

Bath constituent	Examples of sources	Purpose
Copper ions	$CuSO_4$, $Cu(NO_3)_2$	Metal source for reduction and deposition
Complexing agent	EDTA, quadrol	Prevents formation of Cu OH, acts as primary stabilizer
Formaldehyde	37% H_2CO (13% methanol)	Reducing agent for electroless copper
Hydroxl ions	NaOH, KOH	Raises pH to levels required for autoreduction reaction to occur
Stabilizers	Inorganic and organic sulfur compounds, oxygen, addition reagents for formaldehyde, metal salts, cyanides, and nitriles (additives typically present in the 0.001 to 200 ppm range)	Serve as secondary stabilizers moderating the rate of reaction and preventing spontaneous plate-out
Surfactants	Many different types of surface active agents explored, including cationic, anionic and nonionic types	Improve plating uniformity, effect mass transfer at metal surface, help to moderate evaporation

cient thickness to allow electrolytic plating of the through holes to be achieved.

Graphite and carbon black. Graphite and carbon are both sufficiently conductive to allow the circuit manufacturer to plate though holes with them, creating a carbon-based conductor. The plating rapidly coats the though hole in the process. Special processes are normally required, and care must be taken to ensure that the copper surfaces on the inner layers are cleaned before plating is applied.

7.6.4 Resist coating

Resist coating of drilled and metallized boards can be accomplished using any of several methods. Screen printing has been a mainstay process for many years; however, it is limited in terms of the features it can define. While it can be very cost effective, screen printing also has relatively long setup times as compared to other resist coating methods.

The other methods for resist coating are normally associated with photoimagable resists. These methods include, roll coating with dry film resist, flood printing with a liquid resist, and electrophoretic coating. The latter process is similar to electroplating except that a polymer film is plated rather than a metal one.

Roll coating of dry film is one of the most popular methods because of its relative ease and cleanliness. It also is capable of producing fine-line circuit images such as required by many of today's advanced products. In addition to variations in resist applications, there are two different forms of resist, based

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on their exposure mechanisms and chemistry. The variations are called *positive working resists* and *negative working resists*. The former is less commonly used than the latter, although it is generally capable of resolving finer features. With positive working resists, the areas exposed to light are developed away; with negative working resists, the opposite is the case (i.e., where the light strikes the surface, the resist will remain after development). See Fig. 7.13 for examples of imaging processes.

7.6.5 Image patterning

An imaging step is required for all photoimagable plating resists. The process is self-descriptive; however, there are a number of potential variations on the exposure process. Perhaps the most common form of exposure is contact printing, wherein a film containing the desired circuit pattern is aligned with the drilled hole pattern, and the two items are brought into intimate contact by means of a vacuum frame. Exposure is done by means of a UV light source, and exposure length is determined by the type of resist and its thickness.

Other processing methods include off-contact printing and laser-direct writing. In the former case, exposure is accomplished by image projection over a short or long distance. In the latter case, a laser is used to scan the image onto the resist. These methods may see increased use in the future.

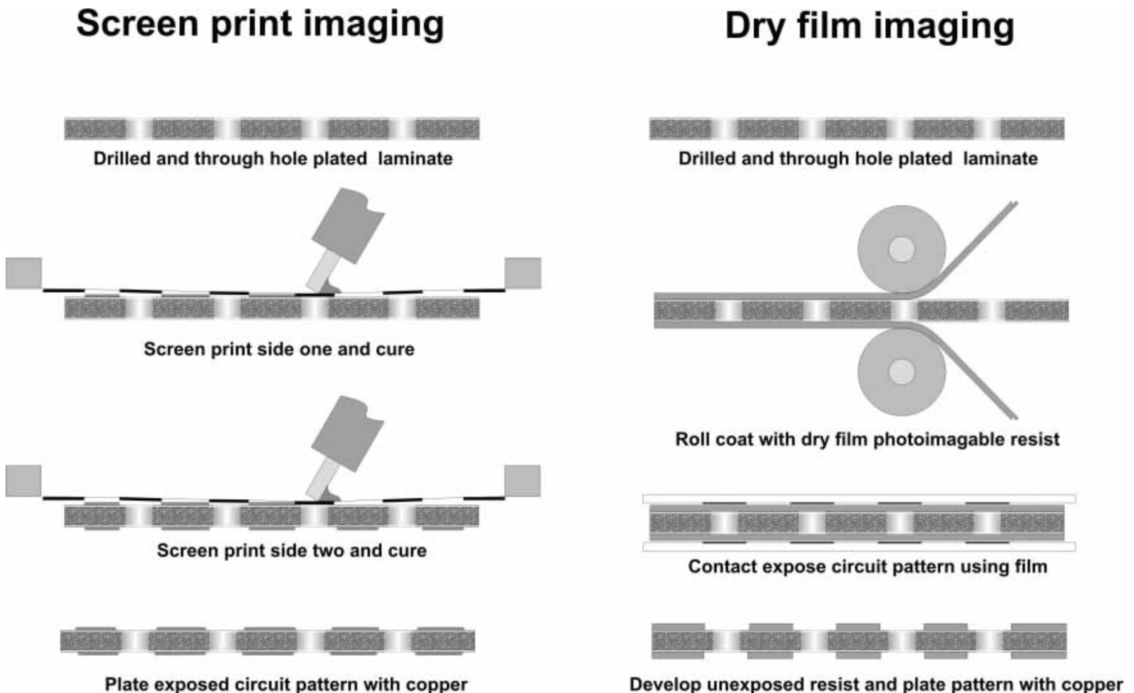

Figure 7.13 Imaging process comparison between screen printing and dry film lamination.

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7.6.6 Image development

Development is normally carried out using a conveyorized process whereby the exposed panels are passed between spray banks of a solution that is designed to dissolve the unexposed resist (or exposed resist, in the case of a positive working resist). Presently, the solutions used are relatively benign and consist of heated dilute (~1 percent) solutions of sodium or potassium carbonate. Care must be taken to avoid overexposure and underexposure and, similarly, to neither overdevelop nor underdevelop the resist. Failure to do so can lead to problems in later processing steps.

7.6.7 Electroplating of the circuit pattern

Electroplating processes are used to bulk metallize the circuit patterns on the surface and through the holes. Because a negative image of the circuit is most commonly patterned onto the drilled and metallized panel, this process is called *pattern plating*.

In the process, the panel is clamped in a plating rack of some sort so that an electric potential can be applied. Because the metal ions in solution are almost invariably positively charged, a negative potential is placed on the rack. The panel is called the *cathode* in this case. The thickness of the copper and other plated metals is controlled by a combination of time and current. Normally, copper is plated to a total thickness of approximately 25 μm (0.001 in), but thicker callouts are common in military boards. Other metals are often plated over the top of the copper. These metals include, tin, tin-lead solder, nickel, gold, and others. The thickness of these metals is normally substantially less, as they serve as finishing metals only.

7.6.8 Resist stripping

After all the required metal plating layers are completed, the plating resist is no longer required, so it can be removed. This is accomplished by exposing the plating resist to a suitable chemistry. The chemistry will vary with the chemistry of the resist, but it is normally an alkaline solution with surfactants. A suitable resist stripping chemistry will safely remove the resist without damaging the metal finishes. Whereas resist stripping can be performed using a batch dipping process, conveyor-based processes, vertical and horizontal, are very common. Care must be taken to fully remove the resist and properly rinse the boards after stripping, or problems can arise during the etching process. The greatest concern is shorts or bridges between circuit traces caused by leftover resist.

7.6.9 Copper pattern etching

An etching step normally follows the stripping process. The etching step removes all of the copper that is not coated with either a suitable etch resistant metal or polymer etch resist. When metals are used as the etch resist, they obviously must be resistant to the etching chemistry. For example, when tin or

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tin-lead is employed as the etch resistant metal, ammonia-ammonium chloride and sulfuric-hydrogen etchants can be used, but cupric chloride etchants cannot. Etching must be controlled so as not to neither overetch nor underetch the circuits. The effects of both are illustrated in Fig. 7.14. Etching can result in shorts. Close spacing of traces with thicker copper foils are often contributing factors.

7.6.10 Solder mask

Solder masks are used to prevent solder from being deposited or flowing onto circuit features other than the proper areas of interest, such as points of attachment. Solder masks were originally developed for PCBs that were to be assembled using wave soldering methods, and they were originally applied only to one side of the PCB—the side that was to be exposed to the solder wave. Without a solder mask, circuit traces on the bottom of the assembly were subject to shorting with solder bridges. Later, as line traces and spaces became finer, the application of solder mask to both sides of the board was implemented to protect the traces from physical damage and inadvertent shorting. Today, with double-sided assembly in widespread use, it is very common for solder mask to be applied to both sides of the PCB.

With the technology trending toward finer lines and tighter spaces, and with the proliferation of microvia technology, solder mask is assuming even greater responsibilities in bare-board fabrication. Liquid photoimagable solder masks (LPISMs) are clearly leading the market. Screen print masks, which dominated the industry for many years, are only marginally reliable for today's products, given their great difficulty in resolving lines and spaces smaller than 10 mils in width. Clearly, liquids have made significant inroads.

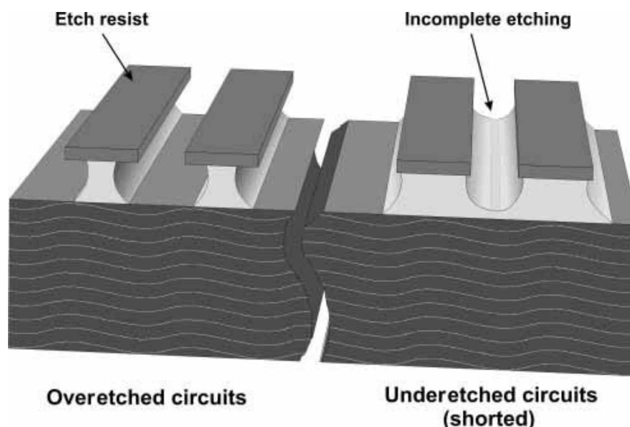

Figure 7.14 Control of the etching process is vitally important to the successful manufacture of a printed circuit. Overetched circuits may not meet designed performance requirements, and underetching can result in shorts. Close spacing of traces is often a factor in both cases.

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Presently, solder masks are available in several forms and chemistries. These are reviewed in the following sections.

7.6.10.1 Solder mask, general types. Solder masks are provided in several different formats, each having different curing mechanisms. There are three general types.

Heat-curable resins. Heat-curable resins are a common type of solder mask. They are commonly applied using screen printing methods. In application, the solder mask resin, normally an epoxy, is screen printed onto everything except the areas and through holes that will be used for assembly.

UV-curable resins. UV-curable resins are normally applied in the same fashion as described for heat-curable resins; however, they have the advantage that they can be quickly cured by exposure to UV light. The properties of these masks differ somewhat from the heat-cured types, but they are generally well suited to the task.

Photoimageable resins. Photoimagable resins are similar to UV-curable resins but with the added advantage that they can be easily photodefined or exposed and developed with an appropriate chemistry. These materials can be applied in wet form by spraying, dipping, curtain coating, or flood screening, or in dry form as a laminated film.

7.6.10.2 Solder mask formulations. Typically, the chemistry used in LPISMs falls into three general categories.

1. Epoxy
2. Acrylate
3. Epoxy-acrylate

It is generally accepted that the "epoxy-only" formulations offer superior adhesion and resistance to solvents than do the acrylate or epoxy acrylate blends. These facts, however, do not obviate the latter two from the market. The epoxy-only masks display a toughness and resistance to chemical degradation as a result of a high degree of cross-linking. Because these bonds occur in three dimensions, the epoxy presents an excellent barrier to moisture and other solvent penetration. Epoxy coatings are compatible with the epoxy of the substrate, thus promoting excellent adhesion.

Acrylates, the other major material category, are known for processing speed. UV curing, as opposed to thermal cycles required of epoxy-only masks, offer very fast curing times. Some suppliers market epoxy acrylate blends that offer properties that lie in between the epoxy- and acrylate-only systems.

Today, most all LPISMs contain some epoxy oligomers and polymers formulated with the acrylate-based chemistries. The acrylate groups are bound to the epoxy molecules to speed up exposure time. This type of mask is given a fi-

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nal cure to complete the cross-linking reaction and advance the physical and electrical properties of the mask.

As one may surmise, LPISM formulations are much more complicated than described above. Listed below is one formulation gleaned from several patents and private conversations over the last few years. Each component listed has a specific purpose, and substitutes are probably available.

Ingredient	Purpose	Wt%
Butyl cellosolve	Solvent	8.5
Carboset resin (Goodrich)	Cross-linking resin	30
Triethylene glycol diacrylate	Oligomer	18
N-methylol acrylamide	Monomer	5
Syloid (WR Grace)—silica	Filler	15.5
Kynar 301F (polyfluoride)	Filler	13
Irgacure 651 (photoinitiator)	Photoinitiator	4
Carboxybenzotriazole	Adhesion promoter	6
Antioxidant 2246	Oxidation inhibitor	0.1

A proper balance of resin, filler, photoinitiators, and acrylate materials will is critical for the success of the LPISM.

It should be noted that some LPISMs currently on the market contain solvents (as in Table 7.6), but others are aqueous based. Generally, if the mask requires a drying step before exposure, it most likely contains a solvent. Another caveat: is the exposed mask aqueous and solvent developable? Solvent-based processing brings its own issues to the board fabrication facility and must be dealt with on a case-by-case basis.

Another aspect of solder masks is whether the formulation is a single-part product or requires a mix on site. The single-part variety is preferred, because it eliminates the possibility of operator error in the form of adding too much or too little of a component. With single-pack materials, however, the shelf life is limited. It may be important for any company serving this market to offer both types of mask.

7.6.10.3 Solder mask selection criteria. A number of criteria are of the utmost importance to the fabricator, end user, and assembly house. Table 7.7 lists these criteria.

If a particular solder mask process has any chance of market penetration, the process must meet UL and IPC standards (IPC-SM-840C). Certainly, the mask must also have been qualified and approved by the end user. In addition, the 2000 IPC Technology Roadmap noted that, in the year ahead, LPISM

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TABLE 7.7 Important Solder Mask Selection Criteria

Manufacturing area of concern	Selection criteria
PWB fabricator	UV cure needed Smallest hole size cleared Acts as plating resist (nickel-gold) Solvent content—low VOCs Tack dry process window Material costs Photo speed Fine pitch resolution
PWB assembler	Adhesion to metallic surfaces Hardness Glossiness Dam holding capability Flux compatibility Solder paste compatibility
Final product vendor	Surface insulation resistance Breakdown voltage Ionic retention Coverage thickness Performance UL approval Key OEM acceptance Conforms to IPC-SM 840 C

must be capable of holding 2-mil solder dams and have uncompromising compatibility with a variety of assembly materials and electroless plating processes.

7.6.10.4 Solder mask application. Solder mask coating operations vary with the type of mask being applied. For example, screen printing can be used to apply the solder mask everywhere except the areas where soldering is to take place. In contrast, dry film solder masks are roll laminated onto the circuit using heat and pressure. The coated circuit is exposed and developed in a fashion nearly identical to the process used for circuit patterning with dry film.

Several methods are available for applying the liquid photoimageable solder masks.

1. Curtain coating
2. Electrostatic spray
3. High-volume, low-pressure (HVLP) spray
4. Screen printing (either horizontal or vertical)

Curtain coating. With this method, a PCB is transported horizontally along a conveyor, and the solder mask is applied as a liquid stream or curtain. The curtain is formed as the ink falls through the coating head. Only one side of

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the board can be coated at a time. Ink formulations for curtain coating are lower in solids content than standard screen coating inks. Thus, the mask will not plug holes in curtain coating applications. The speed of the conveyor transporting the board determines wet ink thickness, and subsequently, mask thickness.

The advantages of curtain coating are as follows:

- high productivity
- relatively uniform resist coating thickness
- good coverage over circuit traces in general
- relatively little waste of material

The disadvantages are

- Low resist viscosity may lead to resist falling off traces (excess solvent added).
- Low solids and high solvent content make it less economical than a screen coat.
- Some issues exist with air entrapment.
- Only one side of panel can be coated at a time.
- High solvent content may cause regulatory problems.

Electrostatic spray coating. From an academic point of view, electrostatic coating of a printed wiring board is not purely electrostatic. Because the PCB is mostly an insulator at the point of solder mask application, a pure electrostatic process is questionable. To make this coating process work, the solder mask material is conducted into a high-rotation spray bell under high voltage. The resist flow tears off at the bell edge to form microdroplets. These droplets become charged at the spray bell then deposit on the PCB and discharge electrically. The printed wiring board must be earthed so that the droplets of resist can discharge. An electric field develops between the first very thin resist coating on the board and the spray bell. Electrical lines of flux concentrate on circuit traces. This allows for the resist coating to build up, starting from the edge. One can achieve excellent coverage this way.

Electrostatic processing has the following advantages:

- High productivity
- Plated-through holes not filled with resist
- Resist thickness easily adjusted
- No entrapped air in the coating

The following disadvantages are involved with electrostatic coating:

- High resist consumption due to overspray
- Coating thickness fluctuations

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- Relatively high capital investment
- Tenting very difficult

High-volume, low-pressure spray. There are two variations to spray coating: (1) horizontal and (2) vertical. In horizontal processing, only one side of the board is coated at a time. In most such systems, the panel is tack dried before the second side is coated. Some systems include a variation whereby, after coating one side, the panel is carried on a V belt. The panel is flipped and the second side coated before the tack dry is carried out. In this case, the panel is tack dried only once. However, it is difficult to process very thin panels in such a system.

Newer models transport the panels on a conveyor. The heated spray guns first coat the bottom side of the panel, which is followed by a coating of the panels on the top side prior to tack dry. With vertical HVLP spray applications, both sides of the PWB are coated simultaneously. Typical equipment utilizes four heated spray heads with overlapping spray patterns. Models are available to coat are 100, 200, and 300 panels per hour.

The advantages of HVLP spray processing are

- Excellent coverage of dense circuit traces
- High productivity
- Relatively low capital costs

The major disadvantages of HVLP include

- Overspray major issue/contamination of equipment
- Tenting/plugging of holes impossible
- Spray coatings exhibit a slight orange peel appearance

Screen printing. Screen printing is accomplished either horizontally or in a double-sided vertical mode. On a worldwide basis, screen coating of solder mask is the most popular means of application. Single-sided methods, primarily for hand screening, are easy to use and have a low entry cost.

In double-sided screen coating, the panels are fixed vertically, and the screens are fixed at an equal distance to the vertical panels. Squeegees on both sides of the panel are placed in exactly the same position on the opposite side of the panel while utilizing identical squeegee angle.

Double-sided vertical coaters made popular by Circuit Automation boast high productivity as a result of their ability to coat both sides of the board simultaneously. Other advantages of the double-sided method are

- Tack dry of both sides simultaneously
- No risk of over drying one side
- Consistent exposure and development

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- High solids content; economical usage compared to other methods
- Lower wet ink weights; uniform edge coverage

The major disadvantages of the double-sided screen print method are

- Low productivity as compared to other methods
- Skipping possible on very dense circuitry
- Screen printing stencils require setup time and increased cost
- High squeegee velocities may cause skips and blisters

7.6.10.5 Performance requirements. Solder masks in general are facing much more stringent performance requirements. Liquid photoimageable solder masks in particular are viewed as being a key enabling type for future products and are thus being required to meet an ever more challenging set of performance criteria. Generally, solder mask performance is measured based on the following:

- Ability to hold 2-mil solder mask dams
- Sufficient coverage over traces without high thickness on laminate
- No bubbles or pinholes in the mask
- Shortest possible processing times
- Ink easily developed out of holes
- Nearly vertical sidewalls
- Ability to be processed in nickel-gold plating solutions

Liquid photoimageable solder masks must meet all the criteria set forth in

- IPC-SM 840C
- Siemens SN 57030
- UL 94 V-0
- Bellcore NWT-TR-000078
- Thermal shock testing according to IBM

Typically, all solder masks must be able to resist attack by solvents and other chemicals that may come in contact with the mask during plating and assembly operations. A critical feature desired of all solder masks presently is to serve as a low-level environmental protectant. That is, the mask must provide a minimum acceptable insulation resistance; must not exhibit evidence of electrical migration; and shall not exhibit blistering, delamination, or crazing when tested under TM 2.6.7.1 of the IPC-TM-650.

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7.6.11 Solderable finishes

Surface finish is critical to the creation of reliable interconnections. Connection from the board to a device occurs at the surface. However a surface finish used for solderability purposes only is at best a compromise. In an ideal world, the assembly engineer would receive bare copper PWBs for assembly. There would be no issues with flatness, product density, cleanliness, and so on. Unfortunately, this is not an ideal world. The ability of the assembly process to deal with oxidized copper as the solderable surface, with the flux activity used in today's assembly industry, is not presently a possibility. Because of this, the assembly engineer/designer needs to choose a surface finish that will meet, to the maximum extent possible, the product's needs, also keeping in mind that in today's highly cost-sensitive environment, the choice of the surface finish may be influenced heavily by its per-unit cost.

7.6.11.1 Tin-lead finish. The original surface finishes were by-products of PWB manufacturing; tin-lead (SnPb) as an etch resist, subsequently reflowed and fused, became the surface finish of preference for many years. This was commonly accompanied by a mix of electrolytic nickel gold to plate the tabs for edge connectors, and the combination directly reflected the technology of the components and assembly techniques of the time.

The introduction of SMT technology forced a change from the simple reflow SnPb surface finish to one that would meet the demands of the assembly industry. New designs required innovative solutions. Ball grid arrays, wire bonding pads, press fit, and contact switches were all outside the traditional realm of HASL and electrolytic nickel gold.

In addition, supposedly environmental concerns are being focused on the elimination of lead. No data has ever been presented to show that lead in electronic solders causes harm; however, marketing pressures and legislation are driving many companies to provide lead-free solutions. As a result, it can be anticipated that HASL will be modified from a standard solder to a new lead-free HASL and a new series of surface finishes.

7.6.11.2 Organic solderability preservatives. Organic solderabilty preservatives (OSPs), as the name implies, are organic coatings that preserve the copper surface from oxidation until it is soldered. The two most widely used preservatives are nitrogen-bearing organic compounds. *Benzotriazoles* is one class, and *imidazoles* is the other. Both of these organic chemicals have the ability to complex with the exposed copper surface. In that respect, they are copper specific and do not adsorb to the laminate or the solder mask.

Benzotriazoles form a monomolecular layer and protect the copper until it is exposed to a single thermal excursion at assembly. The coating will readily volatilize under reflow thermal conditions. Imidazoles form a thicker coating and will survive multiple thermal excursions at assembly.

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Process. The following is a representative process for coating copper circuits with an OSP:

Process step	Temp., °F	Temp., °C	Time, min*
Cleaner	95–140	35–60	4–6
Microetch	75–95	25–35	2–4
Conditioner	85–95	30–35	1–3
OSP	120–140	50–60	1–2

*For conveyorized equipment, the dwell time must be reduced. Consult with equipment and chemical suppliers.

OSP finish. A thin layer of organic compound coats the copper surface. The coating is as low as 100 Å for benzotriazoles and as high as 4000 Å for imidazole-type preservatives. The coating is transparent and not easily discernible, making inspection difficult.

Component assembly and joining using OSP. During the assembly and joining (i.e., soldering) process, the organic coating is readily dissolved into the screened paste or into the acidic flux, in either case leaving a clean active copper surface for soldering. The solder then forms a copper/tin intermetallic joint. Imidazoles may require a more aggressive flux after the first and second thermal excursions. Assemblers who use OSP are very familiar with the fluxing requirements for this finish.

Limitations of OSP. Because the coating is transparent and colorless, it is difficult to inspect. The organic coating is nonconductive. Benzotriazole, being a very thin coating, does not interfere with electrical testing. Some imidazoles, on the other hand, are thick enough to interfere with electrical tests. Most shops that use these thicker coatings do their electrical testing prior to OSP applications.

7.6.11.3 Electroless nickel immersion gold (ENIG). In this finish, a layer of electroless nickel with a thickness of 120 to 240 μin (3 to 6 μm) is deposited on the copper surface. The electroless nickel plating is followed by deposition of a thin coating (2 to 4 μin) of immersion gold. The nickel is a diffusion barrier to copper and is the surface to which the soldering occurs. The function of the immersion gold is to protect the nickel from oxidation or passivation during storage.

ENIG process. The following is a representative process for coating a copper surface using ENIG:

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Process step	Temp., °F	Temp., °C	Time, min.*
Cleaner	95–140	35–60	4–6
Microetch	75–95	25–35	2–4
Catalyst	RT	RT	1–3
E nickel	180–190	82–88	18–25
I gold	180–190	82–88	6–12

**Note:* The long dwell times needed for this process make horizontal conveyorization impractical.

Applications for ENIG. ENIG gives a flat coplanar surface. It is solderable, wire bondable, and ideal as a switch contacting surface. ENIG has excellent solder wettability characteristics. The gold readily dissolves in the molten solder, leaving a fresh nickel surface to form the solder joint. The amount of gold that dissolves in the solder is insignificant and will not cause solder joint imbrittlement. The nickel forms a tin/nickel intermetallic joint.

7.6.11.4 Electroless nickel/electroless palladium/immersion gold (ENEPIG). This finish has proven useful to some circuit providers. In the process, an electroless nickel layer of 120 to 240 μin (3 to 6 μm) is deposited on the copper surface. This is then coated with an electroless palladium layer of a thickness of 4 to 20 μin (0.1 to 0.5 μm) and, finally, topped with immersion gold at 1 to 4 μin (0.02 to 0.1 μm). The electroless palladium layer eliminates any probability of corrosion that may be caused by the immersion gold deposition reaction and creates an ideal surface for gold wire bonding. The gold layer caps the palladium and ensures that its catalytic activity is contained.

Process steps. The sample process steps for a process to produce circuits with electroless nickel with palladium finish are provided in the following table:

Process step	Temp., °F	Temp., °C	Time, min.
Cleaner	95–140	35–60	4–6
Microetch	75–95	25–35	2–4
Catalyst	RT	RT	1–3
E nickel	180–190	82–88	18–25
Catalyst	RT	RT	1–3
E palladium	120–140	50–60	8–20
I gold	180–190	82–88	6–12

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Applications for ENEPIG. ENEPIG gives a flat coplanar surface. ENEPIG is the universal surface finish. It is capable of functioning as the ENIG finish. In addition, the electroless palladium at this thickness makes an ideal surface for gold wire bonding.

During soldering, the palladium and the gold both eventually dissolve in the solder, and the joint forms a nickel/tin intermetallic. During wire bonding, the aluminum and the gold wires bond to the palladium surface. Palladium is a hard surface and is suitable for contact switching.

Limitations of ENEPIG. The primary limitation for this finish is the additional cost of palladium as well as the added processing steps at the board shop.

7.6.11.5 Immersion silver. In principle, immersion silver deposits provide a thin (5 to 15 µin or 0.1 to 0.4 µm) dense silver deposit incorporating an organic. The organic seals the surface and allows for extended shelf life. Silver offers a flat. extremely solderable surface that may be applied with high productivity in conveyorized equipment. The surface is also bondable for both aluminum and gold wire.

Process steps. The process steps are as shown in the following table:

Process step	Temp., °F	Temp., °C	Time, min.*
Cleaner	95–140	35–60	4–6
Microetch	75–95	25–35	2–4
Predip	RT	RT	0.5–1
I silver	95–115	35–45	1–2

*For conveyorized equipment, the dwell time must be reduced. Consult with equipment and chemical suppliers.

Application of immersion silver. Immersion silver is an ideal surface for soldering. During assembly, the silver readily dissolves into the solder, allowing the formation of a copper/tin intermetallic solder joint, similar to HASL and OSP. It offers the coplanarity that HASL lacks, and it is also lead free. Unlike OSP, it offers ease of inspection with no compromise in performance after the third thermal excursion. Immersion silver lends itself well to electrical testing in the board shop. At this time, the application as a contact surface for extended use remains to be demonstrated.

Limitations of immersion silver. The concern with silver has always been silver migration in electronic environments. This is a result of the property of silver to form water-soluble salts when exposed to moisture and electrical bias. Using immersion silver with the incorporation of organics minimizes this phenomenon. In addition, the immersion silver as a surface does not survive the assembly process. After wire bonding, the exposed silver is encapsulated and hence is isolated from the environment.

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7.6.11.6 Immersion tin. Immersion tin became viable as a surface finish when two problems, grain size and copper/tin intermetallics, were overcome. The deposit was engineered to be very fine grained and nonporous. A thick deposit of 40 μin or 1.0 μm was feasible, thus ensuring a copper-free tin surface. A new class of immersion tin processes provide exactly that.

Process for immersion tin. The following are representative processing steps for the immersion tin process:

Process step	Temp., °F	Temp., °C	Time, min.*
Cleaner	95–140	35–60	4–6
Microetch	75–95	25–35	2–4
Predip	75–90	25–30	1–2
I tin	140–160	60–70	6–12

*For conveyorized equipment the dwell time must be reduced. Consult with equipment and chemical supplier.

Application of immersion tin. Immersion tin is a highly solderable surface and forms the standard copper/tin intermetallic solder joint. Tin provides a dense, uniform coating with superior hole wall lubricity. This characteristic makes it the choice for backplane panels that are assembled by *press fit* or *pin insertion*.

Limitations of immersion tin. The bath makeup entails the use of thiourea, which is banned in certain geographical locations for environmental reasons. During processing in the board shop, the primary by-product in the bath is copper thiourea. Waste treatment allowance must be made for the containment of the thiourea and its copper-salt by-product.

The shelf life of the surface is, to some extent, limited (less than one year). This is a result of the progression of the copper/tin intermetallic until it reaches the surface and renders the product nonsolderable. This could accelerate under excessive temperature and humidity conditions.

7.6.11.7 Surface finish summary. Each one of these surface finishes offers connectivity solutions in some areas. Only one ENEPIG is capable of meeting all the different assembly requirements. It is often referred to as the "universal finish." The cost of such a process is very high. However, the ENEPIG surface finish offers both wire bondability and solderability.

7.6.12 Edge card contact plating

Edge card contacts are a convenient way of interconnecting the circuit card to a next level or system board. The process of plating edge card circuits consists of a few modest steps. First, the area above the contacts is masked off using a

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suitable "plater's tape." If a metal etch resist was used, this is removed using an appropriate chemistry (i.e., one that does not aggressively attack copper). The exposed copper is overplated first using nickel and then (normally) gold. The nickel acts as a barrier layer to prevent diffusion of copper into gold. It also serves as an anvil of sorts, because both copper and gold are relatively soft metals and can be easily galled. The process steps are illustrated in Fig. 7.15.

7.6.13 Depanelization processing

Once all major processing steps are completed, the panel can be separated into individual circuits. This process is called *depanelization*. The two primary methods for separating out the circuits are punching and profiling. Punching requires a tool and die set and tooling holes to ensure the parts are properly aligned for punching. Profiling is commonly done using a numerically controlled (NC) router. Again, tooling holes are required to ensure accuracy. Other numer-

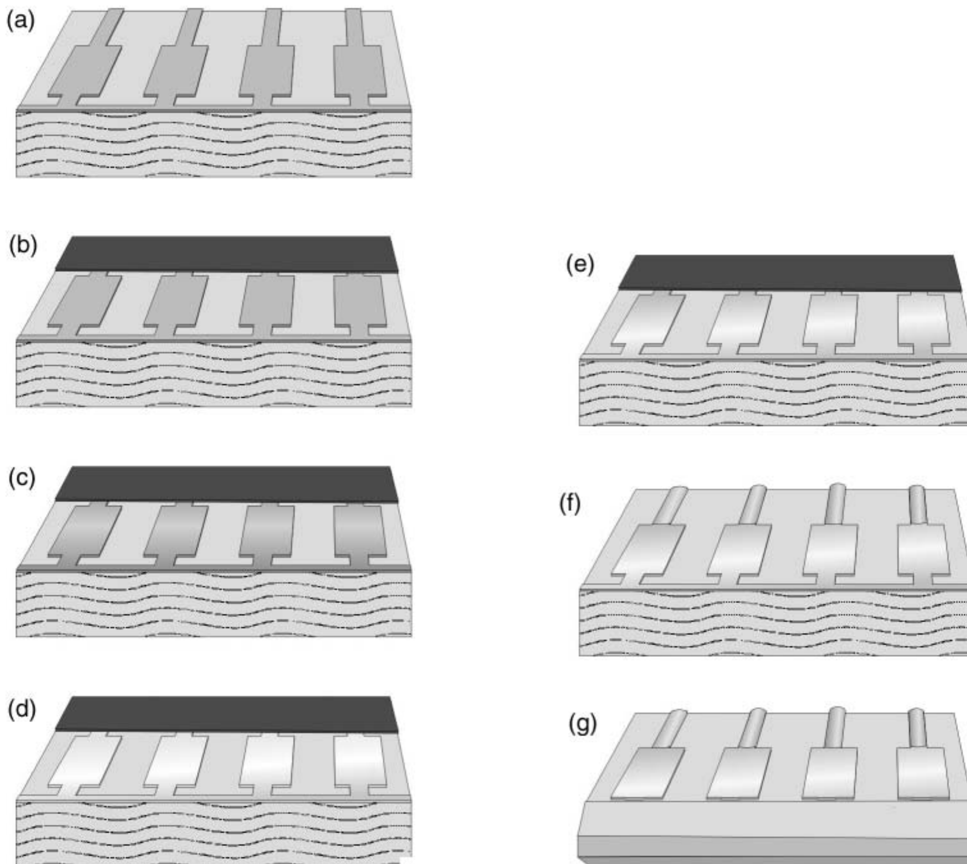

Figure 7.15 Edge card contact manufacturing steps: *(a)* etched contacts with bus, *(b)* apply chemical resistant tape, *(c)* etch solder (or other metal), *(d)* plate nickel barrier metal, *(e)* plate gold over nickel, *(f)* remove tape from circuit, and *(g)* shear bus and bevel edge.

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ically controlled cutting methods are potential candidates for depanelization of circuits, including the use of lasers and high-pressure water jet cutters.

When small circuits are being designed, it is normally advantageous to assemble the circuits in panel form. In such cases, the circuits are commonly cut only part way out of the panel. Following assembly, the circuits can be separated into individual parts by cutting the tabs that hold the circuits in the panel. For rectangular circuits, one- or two-side scoring of the panel can be used instead. This allows the assembly to be easily snapped apart in chocolate bar fashion. A word of caution is offered, however. One must exercise care, as it is possible to crack solder joints and components when snapping apart such assemblies. Figure 7.16 illustrates the general concepts just described.

7.6.14 Edge beveling

Following depanelization, it is common practice to bevel the edges having contacts to facilitate insertion. Special tools have been developed that make this process very simple. The last step in Fig. 7.15 illustrates a beveled edge.

7.6.15 Additive and subtractive processing

There are two primary methods for creating metal circuit patterns on insulating base materials, additive and subtractive. There are also a number of potential variations on these two common themes; for example, there are processes that use combinations of these two, such as so-called *semiadditive* or *semisubtractive* processes. A brief examination of some of these themes will help to clarify the differences.

7.6.15.1 Additive processes. There are several approaches to making additive circuits, so there is potential for some confusion in the terms used for some of

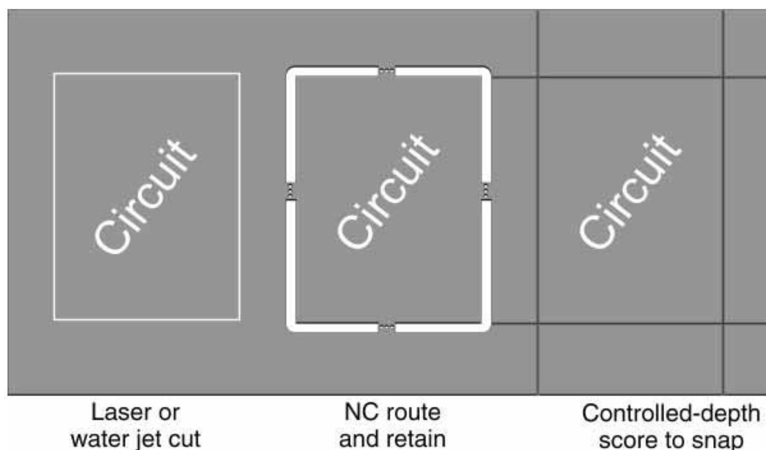

Figure 7.16 Methods for depanelizing finished circuits.

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these manufacturing concepts, which are similar in intent but very different in process. Some of the first circuits manufactured in volume used what must be considered, in practical terms, additive processing methods. These circuits were produced by screen printing circuits directly onto insulators. The insulators could be either organic (such as epoxy or polyester resin) or inorganic (such as ceramic or glass) in nature. Other methods for creating additive circuits include electroless copper-plated circuits and transfer laminated circuits. Figure 7.17 illustrates the process steps for a simple two-sided additive board.

7.6.15.2 Subtractive processes. Subtractive processes were also used very early on in the development of circuit manufacturing methods. While the so-called "print-and-etch" process is the most common image of subtractive processing, there are a number of possible variations. These include punching of copper foil, embossing and milling, and various plate-and-etch processes. The panel plate subtractive process in Fig. 7.17 illustrates the process steps for manufacture of a two-sided subtractive PCB.

7.6.15.3 Semiadditive processes. There is a crossover point at which the line blurs, regardless of whether a process is additive or subtractive. Such processes are most often called *semiadditive,* but the term *semisubtractive* is also used occasionally. The term is most often used for describing processes wherein a very thin layer of copper foil is used on the other layers. The chief advantages are that it allows very fine line circuits to be produced and that a lesser amount of materials, such as etching solutions, are consumed in processing. Figure 7.17 provides a simple example of this process for manufacturing a two-sided PCB.

7.7 Single-Sided Circuit Process Examples

Having earlier described a general process for a double-sided PCB, it is now possible to describe fairly easily some common single-sided circuit processes. A number of potential methods and variations on their themes exist. The following are a few examples.

7.7.1 Print-and-etch

Print-and-etch processing is perhaps the least complex method for making a simple printed circuit. In processing, the metal foil clad laminate is coated with a circuit pattern using any of the previously describe processes, and the circuit is etched. Holes, if needed, can be drilled before or after etching. Figure 7.18 shows a cross section of the simple construction.

7.7.2 Foil routing

A novel method for producing single-sided (also double-sided, with special processing) circuits is to rout the metal-clad laminate to a controlled depth, re-

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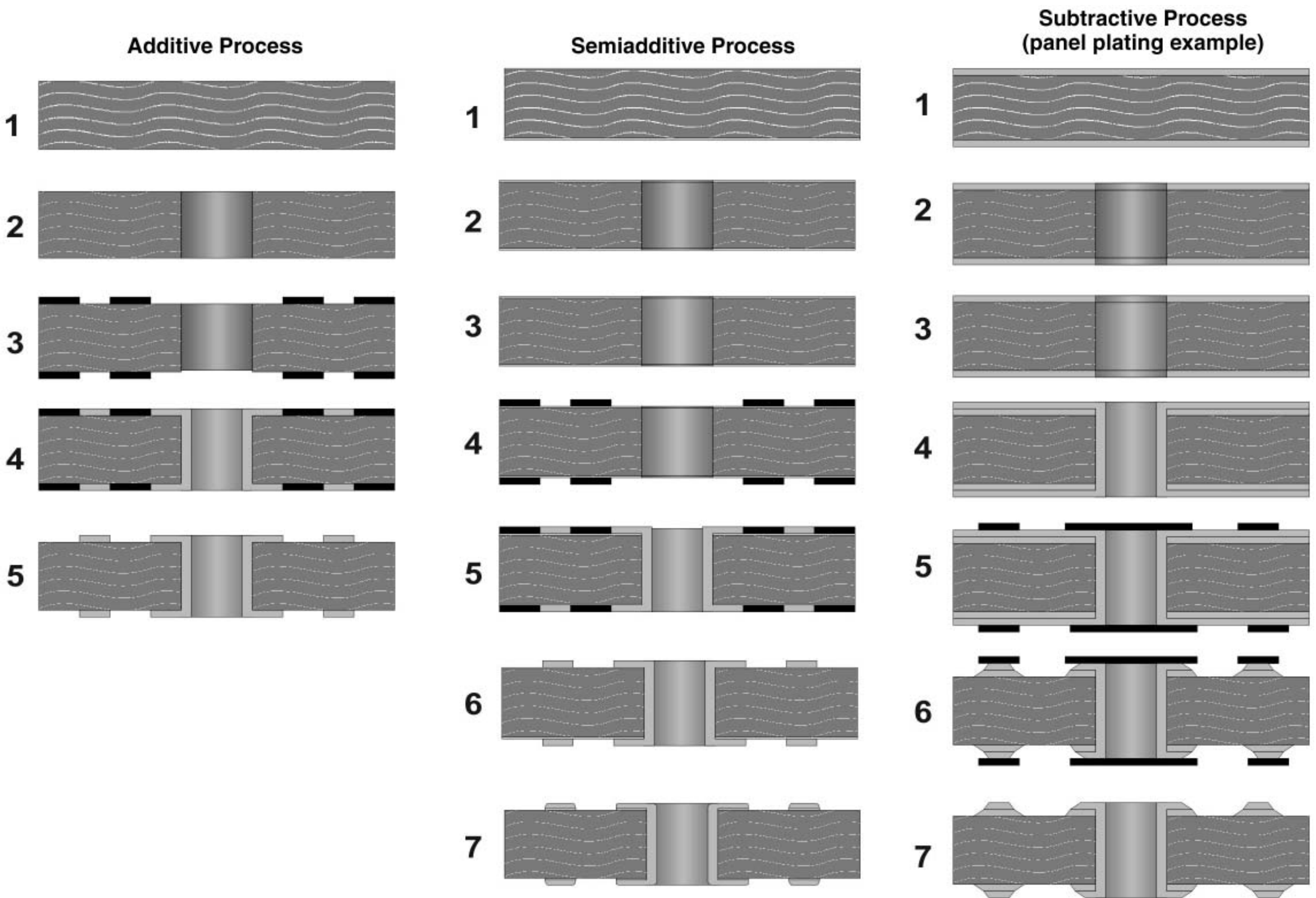

Figure 7.17 Comparison of three different PCB manufacturing methods.

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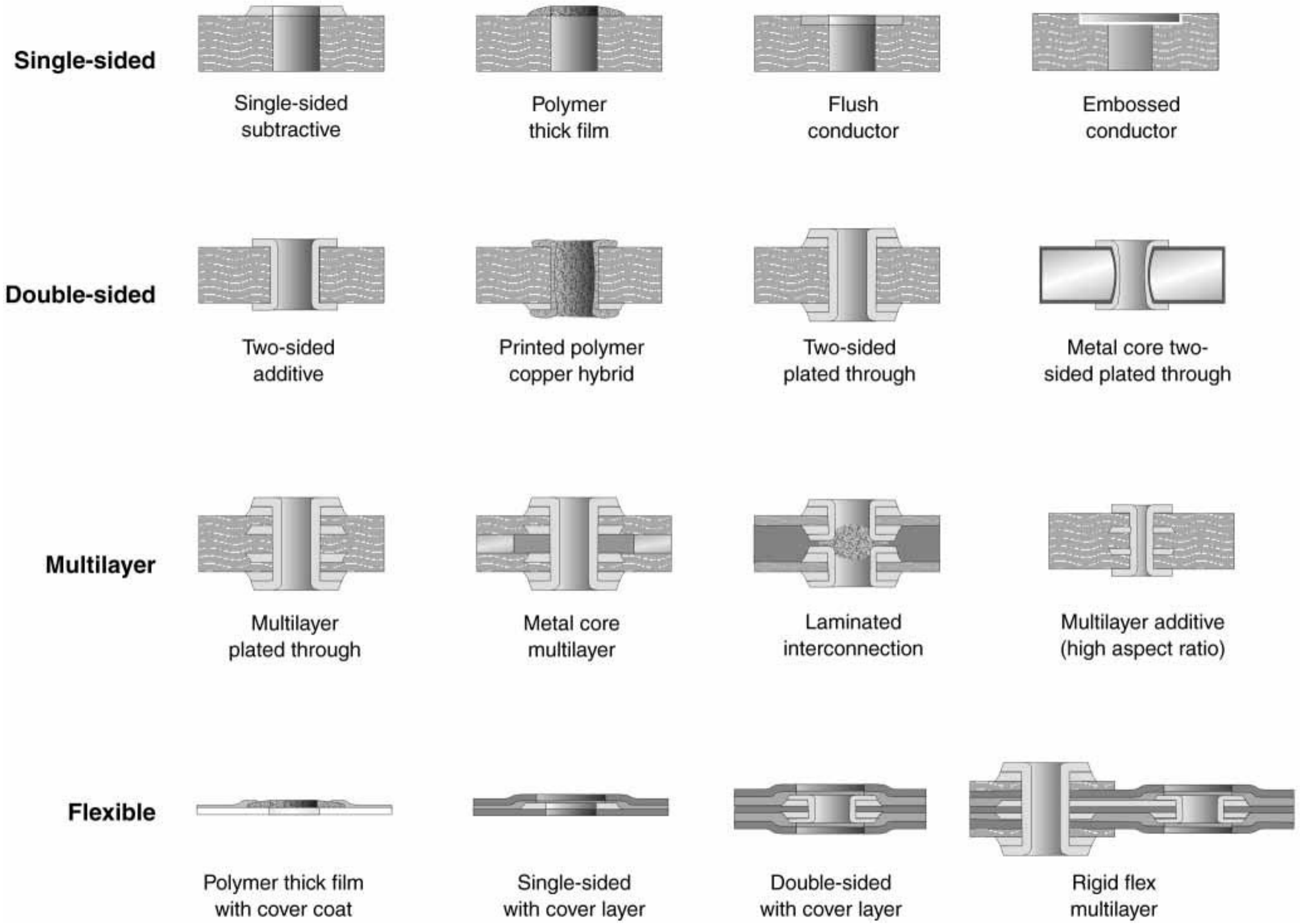

Figure 7.18 Numerous ways exist to fabricate PCBs, and there are also many different possible constructions. Shown above are samples of some of the constructions used. (Note: The cross sections are not all drawn to a common scale.)

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moving the copper that is not needed for the circuit. Thus, each circuit trace is individually defined by routing completely around its periphery. The process is obviously slower than etching and allows only one circuit to be manufactured at a time, but it is nonpolluting and can be done in a small space. Figure 7.19 provides examples of product produced in this fashion.

7.7.3 Direct printing with conductive ink

Direct printing of the circuit pattern with conductive ink is one of the oldest methods and was described briefly earlier in this chapter.

7.7.4 Flush grinding

It is possible to emboss a plastic material with a circuit pattern and then metallize the result using one of several processes. The panel can then be ground flat to expose the raised portions of the polymer while the circuit pattern at the lower level remains.

7.8 Double-Sided Circuit Process Examples

As in single-sided processing, there a number of different ways to create double-sided circuits. The following are brief looks at some of the more common processes.

7.8.1 Panel plate, tent, and etch

Panel plate, tent, and etch processing can be very reliable and economical, depending on the approach and materials chosen. Ideally, a very thin copper foil

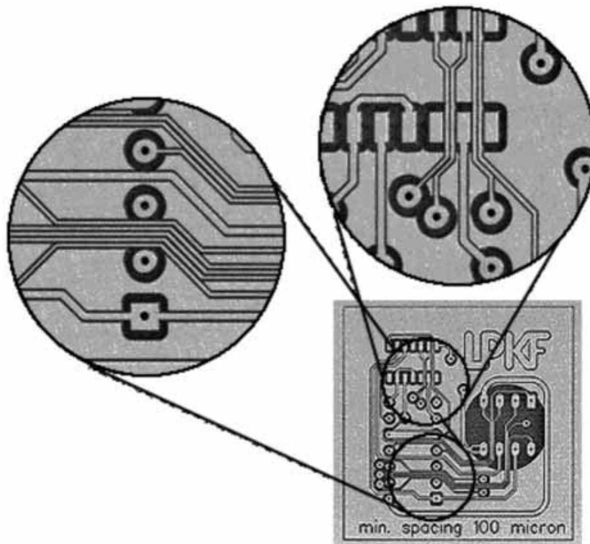

Figure 7.19 Example of foil routed PCB. *(Courtesy of LPKF Laser & Electronics AG.)*

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should be used to start. This makes etching easier and more accurate. The method also obviates the need for an etch metal resist layer removal before solder mask coating. The process follows the steps outlined in Fig. 7.17 under the heading of "subtractive process."

7.8.2 Panel plate, pattern plate

Panel plate, pattern plate processing is similar to the previous method except that, in place of tenting, a circuit pattern of an etch-resistant metal is plated, and the circuit is etched. This method obviates the concern for holes in the etch resist or breaks in the resist over holes, which can result in all the metal being etched out of the through hole. As in the case above, a very thin copper foil ideally should be used to start to make etching easier and more accurate.

7.8.3 Pattern plate

Pattern plating is a very common method used in circuit processing. Most often, it follows the process steps described in Sec. 7.9. When a thin copper foil is used to start, a semiadditive process can be used. This allows the processor to avoid having to plate and later remove an etch resist metal layer. The process steps for pattern plating using the semiadditive method are shown in Fig. 7.17.

7.8.4 Printed-through hole

An unusual method for making side-to-side connections on a PCB is to use conductive inks printed through the holes following a double-sided etch process. The ink is normally screened or stenciled on while the plane is placed on a vacuum table, which draws the ink down through the holes. The process is normally repeated from the other side to ensure full coating.

7.9 Standard Multilayer Circuit Process Example

There are many ways to produce a multilayer printed circuit, but only a few methods see any major use, and these are the products of many years of experiments and experience. The following are brief discussions of some of the key process steps in the creation of a multilayer printed circuit.

7.9.1 Inner layer image requirements

In the construction of a multilayer circuit, it is necessary to carefully control every step of the manufacturing process. Thus, the images that are to be generated for the circuit patterns should adequately address the needs of production. This is manifest in several ways (depending on the complexity of the design) but normally includes, as a minimum, the retention of copper around the circuit to improve dimensional stability and an adjustment of the circuit trace widths to compensate for the effects of the etching process. For contact exposure, a negative image is normally used (clear traces and opaque spaces), as negative-acting resists are most common.

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7.9.1.1 Inner layer material preparation. Unless materials are purchased precut, the first step in the manufacture of a multilayer is to cut laminate sheets to the appropriate panel size. Normally, this is a size that is acceptable to all of the following processes. Depending on how the material is cut, the inner layer material (also commonly called *core material*) at this time may have the edges cleaned to minimize the potential for imaging defects caused by fragments or particles of glass or epoxy.

7.9.1.2 Tooling hole generation. Tooling holes are a vital part of multilayer manufacture. They are the key element of the registration system, which will be required to successfully produce the multilayer circuits. Highly accurate tooling hole punching systems have been developed that allow all the tooling holes to be punched at one time. Whereas the minimum number of tooling holes, in theory, is two, most tooling systems punch four holes. These holes are most often at the centers of the laminate sides near the edge (see Fig. 9.20). This approach has been developed with the intent of making the center of the panel the 0/0 point minimizing runout in any on direction.

7.9.2 Resist coating

The resist coating process is similar to that described earlier, except that, because of accuracy limitations, screen printing is rarely if ever used for such

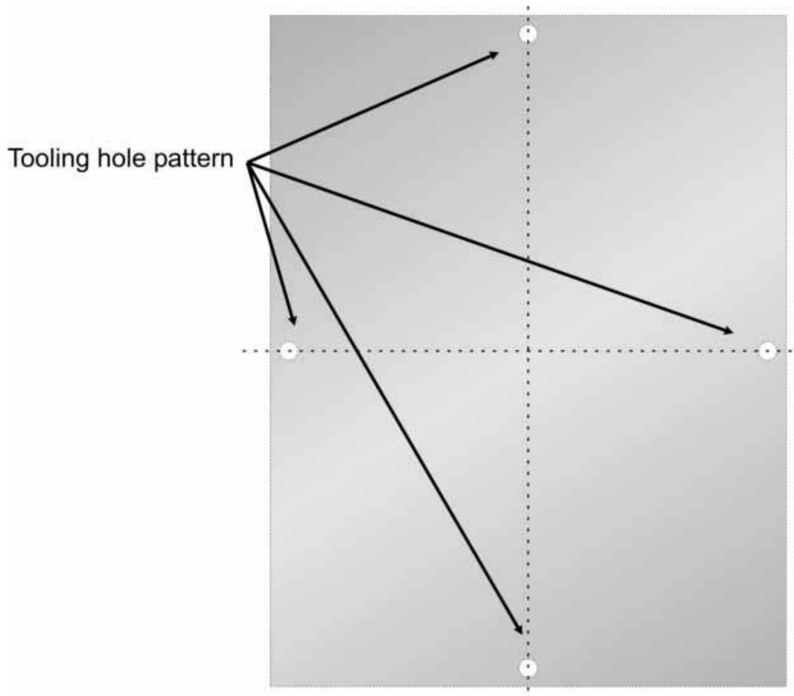

Figure 7.20 Illustration of typical tooling hole layout.

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purposes. The panels must be clean and free of any foreign materials that might be impervious to or alter the etching rate. Roll coating of dry film resist is very common at present; however, other methods based on electrophoretic deposition of resists are proving popular for very fine-line circuits.

7.9.3 Exposure methods

There are several methods that can be used to expose the resist-coated laminate. Contact printing remains popular at present, wherein the coated core material is mated to the film containing the correct circuit pattern on top and bottom, using the tooling pin system, and then exposed to UV light. Although this method is still the most widely used, off-contact and laser-direct-write methods are showing some promise.

7.9.4 Development

Development methods are identical to those described earlier; however, because the laminates are very thin, special care in handling is required.

7.9.5 Etching

The etching process is a critical step in the processing of a printed circuit inner layer. This is especially true in the case of circuits being designed for controlled-impedance applications. The processes used are the same as those described earlier in this chapter.

7.9.6 Resist stripping

The resist stripping process step follows the etching step. The process is very simple, with the only major concern being that the stripping be complete and that the panels be adequately rinsed.

7.9.7 Copper circuit surface preparation

The surfaces of the copper circuits on the laminate are normally provided with an oxide treatment to improve the adhesion of the resin to the circuits. A number of different oxide treatments are available. Black oxide (cupric) was very common in the past, but newer methods have been developed that leave the exposed copper with a brown oxide (cuprous) finish that has some improved characteristics. The use of a so-called “double-treatment” copper foil can obviate the need for such a process and is favored by some manufacturers.

7.9.8 Lay-up for lamination

Circuit lay-up for lamination is accomplished by laying down circuit layers in an ordered fashion on a carrier plate of steel, which shares the same tooling hole layout as the punch. Plies of prepreg are placed between each of the inner layer cores until the stack is complete. The type of prepreg, in terms of cloth

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type and resin formulation, is prescribed by the circuit design needs. Normally, two plies or sheets of the chosen prepreg are used between each of the layer pairs. A number of multilayer circuit panels can be laminated at one time. To facilitate handling of copper foil when cap foil lamination is desired, it is possible to purchase the thin copper foil preattached to a thicker metal carrier. This method obviates the need for separator plates between multilayer circuits in the stack. Figure 7.21 provides an example of a possible circuit lay-up.

7.9.9 Lamination methods

A number of different approaches to multilayer lamination have been developed over the years. Traditional lamination methods are still suitable for many products, but advanced high-density circuits often can be better served by other methods. One important method is to augment the process by the application of a vacuum during lamination. This approach helps to expel air from the laminate and prevents its entrapment during lamination. Entrapped air can cause problems in processing and weaken the laminate. To assist in air removal, methods have been developed wherein lamination takes place in a vacuum. Other nonstandard methods have also been developed such as vacuum autoclave lamination. In this process, the circuits are laminated by placing them in a high-temperature bagging material, drawing a vacuum on the bag to expel the air, and then placing the bagged circuits into a pressure vessel. Pressure is applied by adding CO_2 gas and heating the gas to lamination temperature by means of a convection oven inside the pressure vessel. This method is very popular with flex circuit manufacturers.

Beyond the lamination processes described earlier, there is one other that is quite unusual. In lay-up, a double sheet of copper foil is rolled back and forth between the individual circuit panels, forming a continuous dual-foil sheet. This assembly is then placed in a vacuum lamination chamber, and pressure is applied. Heat is generated by passing high-electric DC current through the

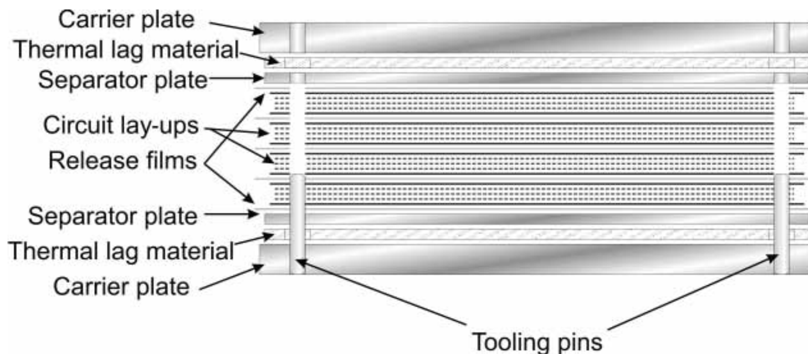

Figure 7.21 Example of a possible lay-up for multilayer lamination. Variations are possible in terms of materials and stack-up heights, depending on the needs and preferences of both the product and the manufacturer.

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copper foil, which causes it to heat up to temperatures at which the prepreg resin can flow, fill, and encapsulate circuit features and cure.

Following lamination, the panels are normally trimmed to remove resin flash at the edges of the panel. Again, it is advisable that the edges be dressed so that they do not cause problems in later steps such as imaging of the outer layers.

7.9.10 Drilling

Accurate drilling of a multilayer circuit is integrally linked to the tooling system. The tooling holes serve as a collective datum for the drilling machine. As such, the tooling holes must accurately link to the circuit patterns that were imaged, etched, and laminated to become internal elements of the PCB and invisible to the unaided eye.

The process of drilling must be very well controlled to ensure its quality. It is common to reduce the drill stack height for multilayer circuits to ensure drilled hole quality. This is especially true when very small holes are being drilled or when design features are especially small.

7.9.11 Hole cleaning and etchback

Following drilling, it is fairly common to perform some sort of cleaning process to remove any resin that might have smeared over the surface of the copper inner layers. Failure to remove such resin smear could degrade the reliability of the plated-through hole interconnection to the inner layer, or it could completely block the interconnection, depending on the severity of the smearing. Some customers request etchback of the resin from the inner layer lands. Doing so creates a so-called “three-point interconnection.” This is commonly referred to as *positive etchback* and is normally deemed to be a more reliable interconnection. In contrast, some board users suggest that negative etchback has advantages. Here, the copper is etched back slightly and provides easily verifiable evidence of resin removal, because it would otherwise interfere with the copper microetching process used as a part of the hole-plating process. Figure 7.22 illustrates the difference between the two methods.

7.9.12 Subsequent processes for multilayer PCB manufacture

The process steps following hole cleaning are essentially the same as those used for double-sided processing and can be used for reference as benchmark processes.

7.10 Mass Lamination

Mass lamination describes a technology wherein the laminate manufacturer fabricates multilayer panels in full sheet form, normally as a service to printed circuit manufacturers who either do not have lamination technology in house or whose lamination manufacturing capacity is limited.

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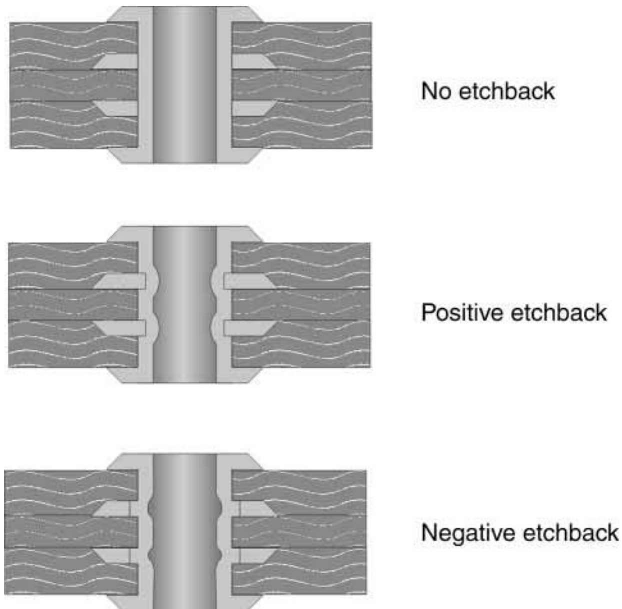

Figure 7.22 Etchback can be either positive or negative, as illustrated above.

The method is generally limited to use with relatively simple multilayers and is most often used for four-layer multilayer circuits. However, higher layer counts have been achieved using modified approaches. Mass lamination differs from traditional lamination in that it is pinless. The inner layer cores are produced by accurately registering the top an bottom films of the inner core material (normally ground and power layers, which are not very complex) to the resist-coated panels and then exposing, developing, and etching them in the same fashion as is used for normal multilayer cores. Targets are etched into the copper foil in the locations where the tooling holes normally would have been punched and after lamination. The targets are accessed either by carefully milling through the copper and laminate above to expose them for accurate drilling or by means of an X-ray-assisted drill or punch. Once the tooling holes are drilled, the panels can be accurately registered with subsequent drilling of normal plated-through holes. The general process steps are illustrated in Fig. 7.23.

7.11 Metal-Core Printed Circuit Boards

Metal-core PCBs are a special subset of printed circuits. The name is adequately self-descriptive, and the purpose of these structures is normally to facilitate the rapid and efficient removal of heat from the board. These constructions are most desirable for use with products that will be generating large amounts of heat or that operate in conditions (e.g., aerospace) where convection cooling is of limited potential or value. There are a number of potential

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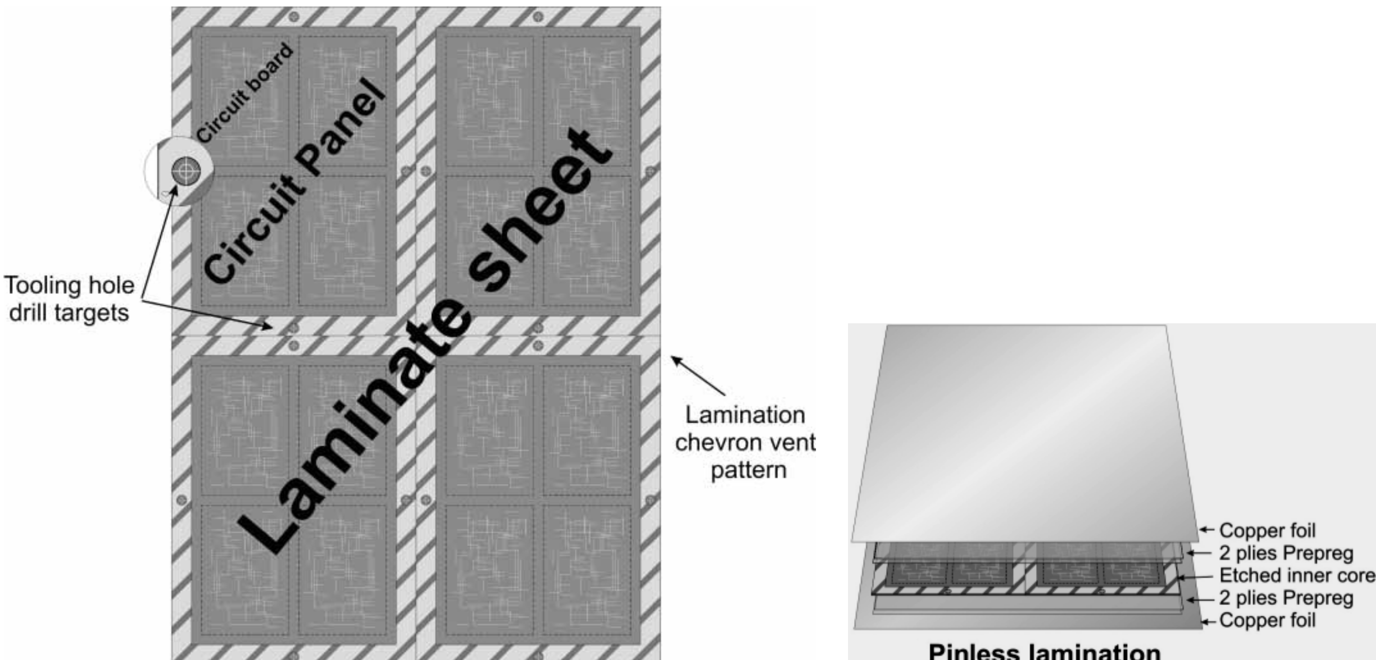

Figure 7.23 Mass lamination methods are used to laminate full sheets of circuit panels. After lamination, the sheet is cut into panels, and the tooling holes are drilled using the etched targets to ensure proper placement.

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constructions of these boards; however, if one is to keep true to the definition provided, there are only two general forms of metal core PCBs, double sided and multilayer. The following are descriptions of basic metal core structures.

7.11.1 Double-sided metal-core

Double-sided metal-core boards are the simplest form of the product. The fundamental structure consists of a piece of metal with holes, over which lies a coat of insulation topped with metal circuit patterns. The insulation material can vary. Porcelain, baked, enamel, and various organic coatings can be used. The choice is a function of the application and the amount of heat being generated and dissipated. Figure 7.18 provides an example of a simple structure.

7.11.2 Multilayer metal core structures

Multilayer metal core structures are also found in a variety of formats. The most common again follows the precepts of the basic definition of metal core, which consists of a multilayer circuit fabricated on either side of a central metal core. However, certain other constructions are included under the umbrella of metal core. These would include constructions where copper clad Invar is used to control the in-plane expansion of the board and where they might also serve as power and ground planes. An example of a basic metal-core board is illustrated in Fig. 7.18.

7.12 Flexible Circuits

Flexible circuits are a unique and very important form of printed circuit. The IPC standards document IPC-T-50, Terms and Definitions for Printed Boards, defines it as follows:

> A patterned arrangement of printed wiring utilizing flexible base material with or without flexible coverlayers.

This is an accurate but somewhat limited definition, as it fails to consider fully how the technology can be applied. For example, flexible circuits can be used statically, in a "flex-to -fit" fashion, or they can be dynamically flexed either intermittently, such as when used in hinge applications, or nearly continuously when used in disk drive applications. Flexible circuits are most fundamentally a three-dimensional interconnection technology. Special design practices are required to create reliable flexible circuits, and potential users are advised to familiarize themselves with flex circuit design information before embarking on a flex circuit design to avoid potential problems. There are several different types of flexible circuits. These are described in the following sections.

7.12.1 Single-sided

Single-sided flex circuits are the most commonly produced members of the family. They are the lowest-cost variant and the type best suited to dynamic flexing applications. They can be produced using either etched metal or

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printed conductive inks to create the circuit patterns. The metal can be accessed from one or both sides if desired. In the latter case, the polymer base film is removed by a suitable means, such as a laser. A special-case variation involves selective etching of the copper to create a circuit that has copper of different thickness along the length of the circuit patterns—thin in areas to be flexed, and thicker in areas where interconnection is desired. A cover layer is commonly applied to protect the circuits and to improve their longevity in dynamic flexing applications. See Fig. 7.24 for an example.

7.12.2 Double-sided

Double-sided flex circuits are the second most common form and are used where higher-density interconnection is required. These flex circuits obviously have two metal layers, and they are normally interconnected by means of a plated-through hole, although this is not always necessary. For example, the so-called "type 5" flex circuit is a nonplated-through hole flex wherein both metal layers are accessed from the same side. See Fig. 7.25 for examples.

7.12.3 Multilayer

Multilayer flex circuits are used in applications requiring higher-density interconnections. They are similar to their rigid counterparts but are often more complex and very engineering intensive. Very fanciful looking but highly practical multilayer flex circuits have been fabricated to solve complex electrical and electronic interconnection problems. It is possible to build multilayer flex

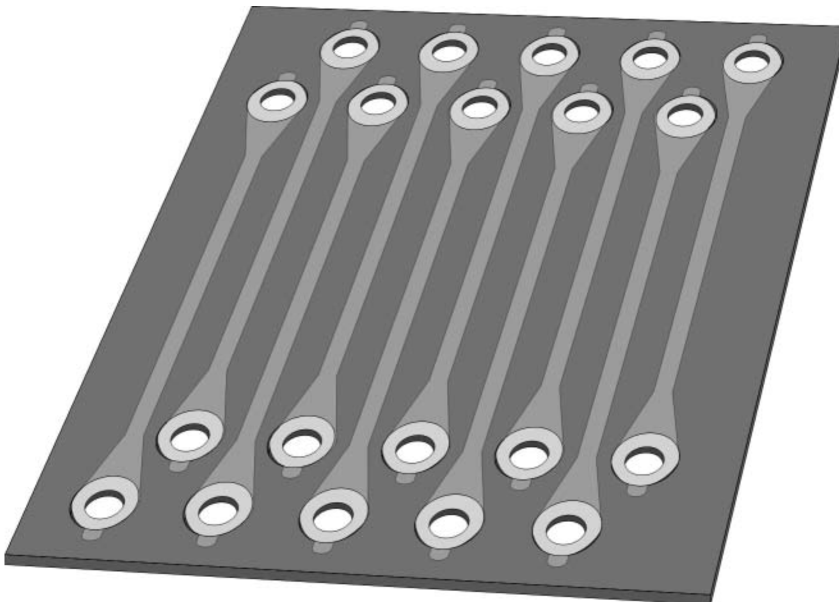

Figure 7.24 Example of the construction of a simple single-metal-layer flex circuit.

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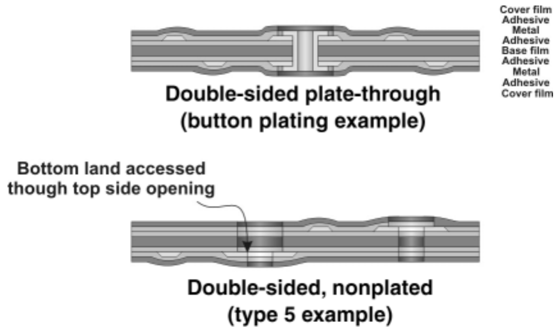

Figure 7.25 Two-metal-layer flex circuits can be fabricated in one of the two basic ways shown above.

circuits with tentacles having varying numbers of layers broken out from a central section. See Fig. 7.26 for example.

7.12.4 Rigid-flex

Rigid-flex circuits are the final variation of flex circuits. As the name suggests, they are a hybrid construction that brings together construction elements of both rigid and flexible circuits. Most often, the rigid portions of the rigid-flex circuit are used to support connectors and or components, and the flexible portions are used to interconnect the rigid sections. The technique won the favor of military product designers in the 1970s as a means of creating higher-reliability and lighter-weight interconnection structures than the wire harness alternatives that they often replaced. Like multilayer flex circuits, these circuits are frequently highly engineered and require a great deal of understanding of manufacturing process for them to be designed properly. Figure 7.27 provide an examples of a rigid-flex construction.

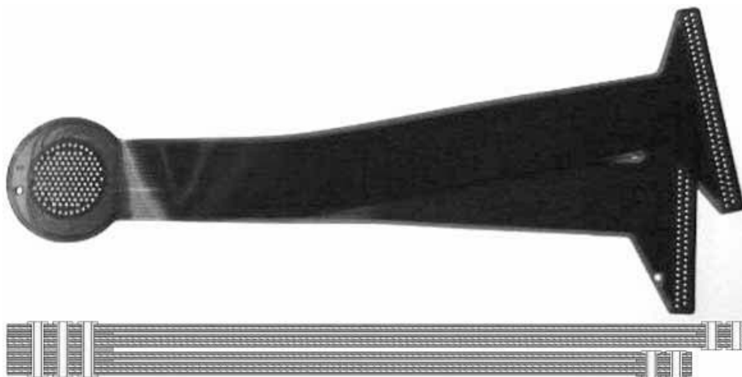

Figure 7.26 A deceptively simple looking multilayer flex circuit with a complex construction as can be seen in cross section. Single and doubled sided flex circuits are pre fabricated, joined and plated through and the those structures are joined and plated through again to create the finished circuit.

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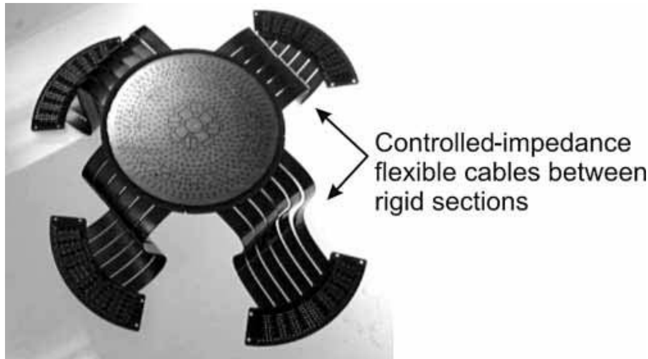

Figure 7.27 An example of a rigid-flex circuit with integral controlled impedance sections between rigid elements of the circuit.

7.13 High-Density Interconnection (HDI) Structures

Semiconductor manufacturing technology is the driving force behind the electronics industry. Semiconductor integrated circuit features continue to be reduced in size to meet the demand for more function in lesser amounts of space. This in turn has resulted in the creation of devices that operate at higher speeds and with greater efficiency with each new generation of product. However, as more recent generations of IC devices pressed the limits of older traditional IC packaging technologies, new technologies had to be developed. The early 1990s saw a number of different attempts to create substrates to meet this challenge and provide solutions. These products were generally referred to as *multichip modules* or *MCMs*. The substrates used for these structures were really the first of the HDI substrates, and they drew heavily from the technologies used to create ICs. They were, however, very expensive, and the final products were vexed by their inability to obtain reliable sources of known good die (KGD), without which their yields were low enough to be viewed as impractical.

About the same time, there was a surge of interest in a new IC packaging methods based on the used of printed circuit technology. The new approach, based on area array interconnections, was a response to the rising pin counts and the inability of industry to obtain good yields with the more traditional peripherally leaded packages. These devices are known now as *ball grid arrays* (BGAs). While the early structures were rather simple (beyond the need for relatively small holes) and presented little challenge to PCB manufacturers, as chip I/O counts increased, there was a need for additional layers of circuitry. The additional circuit layers were required to help redistribute the circuitry to a pitch more suitable to the needs of next-level PCB design, manufacture, and assembly. HDI concepts explored for MCMs were reexamined for use with these new packages but using advanced PCB technologies in place of the semiconductor technologies that were dominant in the earlier effort. This became a proving ground of sorts for a number of HDI manufacturing concepts.

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7.13.1 HDI substrate construction types

Presently, a significant number of different processes have been proposed and/or developed for manufacturing high-density interconnection substrates. The IPC has attempted to bring some order to the matter by identifying and classifying, into general types, the various HDI PCBs that have been described in the literature. Thus far, six general types of HDI structures have been identified. These are described in the following sections.

7.13.1.1 Type 1 construction. The Type 1 HDI structure is typified by a circuit having a rigid core that could have multiple circuit layers on which microvia buildup layers and through holes can be plated simultaneously. Normally, the microvia layers can be plated up on either or both sides of the circuit core (see Fig. 7.28).

7.13.1.2 Type 2 construction. The Type 2 HDI structure is typified as a circuit having a rigid core that could have multiple circuit layers and that has holes plated through with copper. These holes are filled with resin before further processing and thus become blind vias (or possibly semiblind vias) on completion of the fabrication process. Completion is effected by plating microvia buildup layers on either or both sides of the circuit core (see Fig. 7.29).

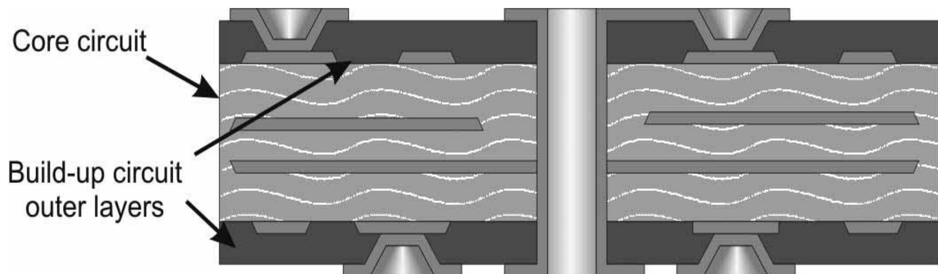

Figure 7.28 HDI construction Type 1, described in text.

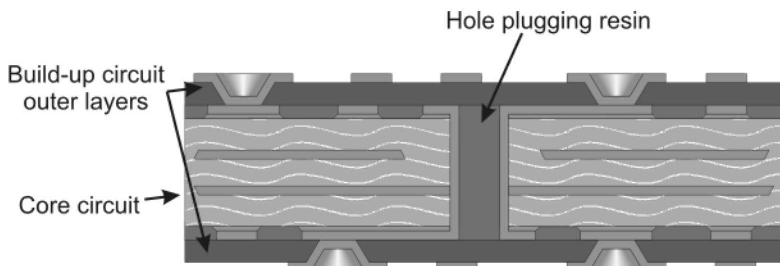

Figure 7.29 HDI construction Type 2, described in text.

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7.13.1.3 Type 3 construction. The Type 3 HDI structure is typified by a circuit having a rigid core with buried vias (as in Type 2) and one or more microvia buildup layers on one side and two or more on the second side. These structures also have plated-through vias, which make direct connection from side to side (see Fig. 7.30). (Note: unbalanced structures are not recommended.)

7.13.1.4 Type 4 construction. The Type 4 HDI structure is typified by a circuit having rigid insulating or metal-core substrate with two or more buildup layers on each side. It also has plated-through vias connecting the two sides of the PCB (see Fig. 7.31).

7.13.1.5 Type 5 construction. The Type 5 HDI structure is typified by co-laminated circuit structures with circuit layers interconnected during lamination to achieve vertical interconnection using conductive pastes or alloys. There are several variations on this basic theme (see Fig. 7.32).

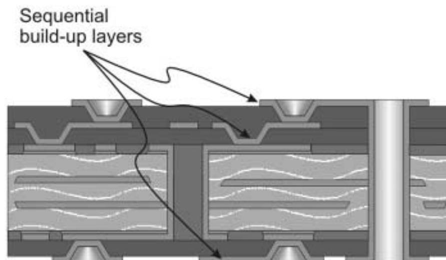

Figure 7.30 HDI construction Type 3, described in text.

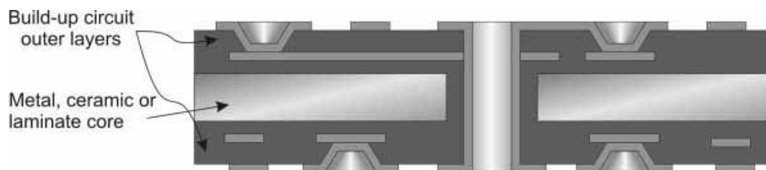

Figure 7.31 HDI construction Type 4, described in text.

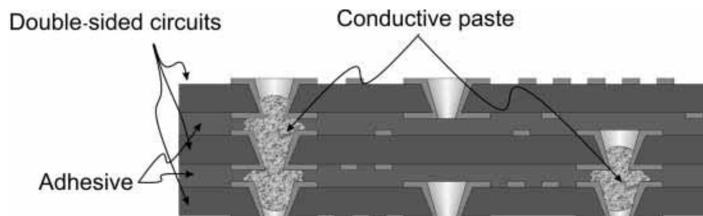

Figure 7.32 HDI construction Type 5, described in text.

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7.13.1.6 Type 6 construction. The Type 6 HDI structure is typified by circuits fabricated using insulation-piercing features of integral metal or stenciled conductive polymer, which make interconnection during a lamination process (see Fig. 7.33).

7.13.2 Build-up board example

The concept of the organic laminate build-up board was likely inspired by the technology used to fabricate hybrid circuits. Hybrid circuits are routinely fabricated by sequentially layering circuits and insulating materials to create the final product. However, hybrids generally employ inorganic materials in their construction and use a different set of manufacturing processes and equipment. The major attraction was hybrid circuit technology's small via structures that offered better routing space potential and improved electrical/electronic performance. As was illustrated in the foregoing discussion of HDI types, there are numerous variations on the basic HDI concept. Most of those are build-up type structures. The flow diagram in Fig. 7.34 provides a general illustration of the basic build-up board process.

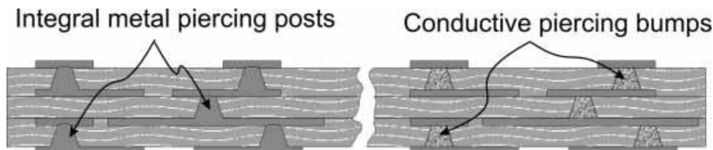

Figure 7.33 HDI construction Type 6, described in text.

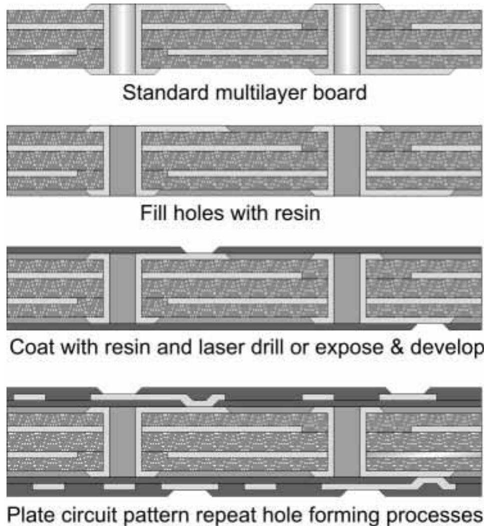

Figure 7.34 Simplified example of the basic process steps in the manufacture of a build-up board.

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7.13.3 Co-laminated structure example

Co-laminated HDI circuits also are likely to have taken inspiration from hybrid circuit manufacture for many of the same reasons; however, there are some significant differences as well. Co-laminated HDI substrates offer a two important advantages: (1) they do not require the plating of high aspect ratio holes, and (2) the layers can be individually tested and yielded before lamination. IBM, Tessera, and CTS Corporation have all described such methods. An example of one such process is provided in Fig. 7.35.

7.13.4 Sequential laminated structure example

This approach to manufacture has been employed by at least two major Japanese companies, Matsushita and Toshiba. There are significant differences between the two approaches, but the final products are comparable. Toshiba uses an insulation-piercing conductive bump to make connection between layers of copper foil at predetermined points during lamination. In contrast, Matsushita prepunches or predrills the insulation layer and fills the holes with conductive paste before laminating on the copper foils. Packard-Hughes of Irvine, California, has described in a patent a concept similar to that used by Toshiba, but they use integrally plated copper bumps to pierce the insulating layer during lamination. Flow diagrams for these processes can be seen in Fig. 7.36.

7.14 Inspection, Evaluation, and Test of Printed Circuits

Regardless of the type of printed circuit that is designed, manufactured, and used, it is inevitable that, at the end of the manufacturing process, some man-

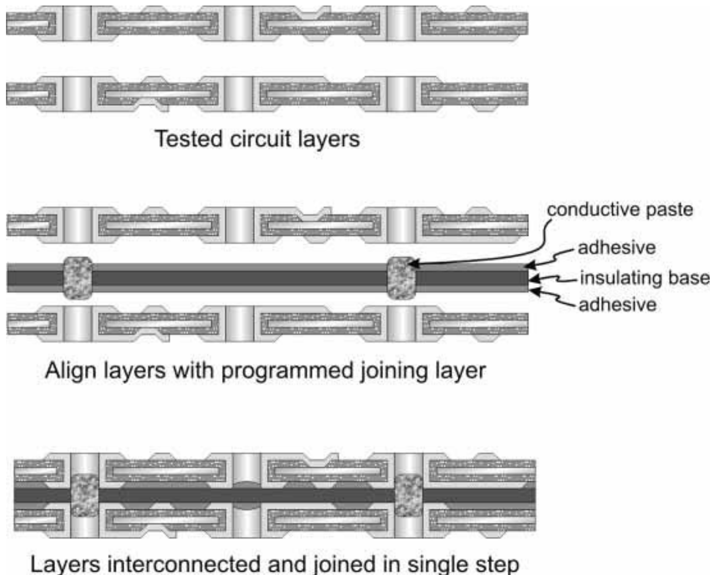

Figure 7.35 Simplified example of a co-laminated HDI structure.

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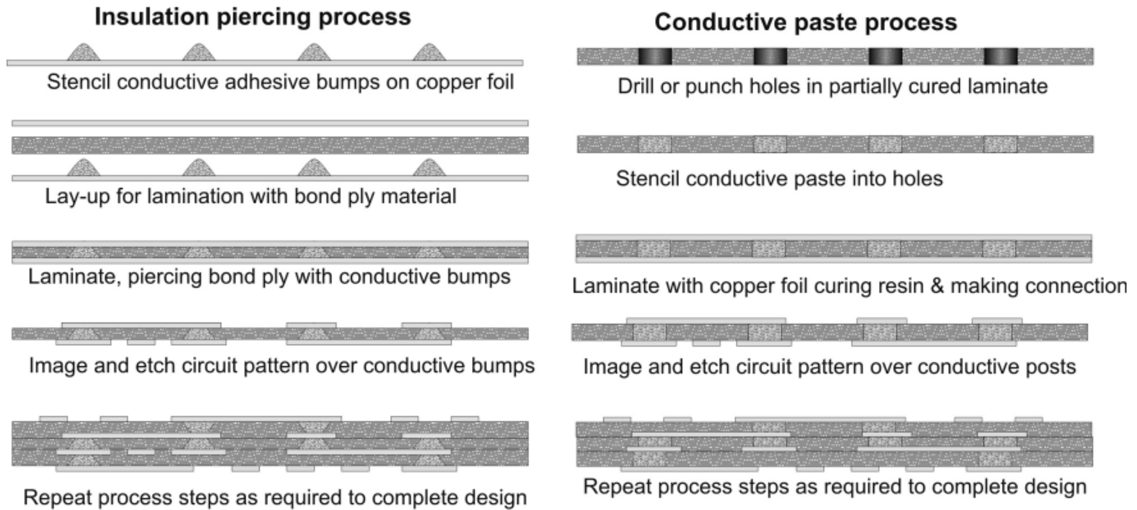

Figure 7.36 Several different methods exist for manufacturing sequentially co-laminated structures.

ner of inspection and test of the printed circuits will be performed. These processes are arguably the most important steps in the process. The reasons are quite simple, and one quick example will help to illustrate. The fact is that, although a printed circuit may be an expensive component in and of itself, the cost of the components that are to be mounted on the PCB are often much higher in total. This simple fact raises the importance of ensuring the integrity of the assembly function and quality to a high level. Thus, what to look for and what to test are important questions to be addressed.

7.14.1 Inspection points for printed circuits

In evaluating the quality and functionality of PCBs, we duplicate many of the tests that were performed on the raw material by the laminate manufacturer to qualify their product. The logic of this redundant testing is that it provides a measure of assurance that the manufacturing processes used in creating the PCB have not in some way degraded the material beyond acceptable limits. As with the raw materials, testing requirements have been established in several key areas to ascertain that the product is acceptable for its intended purpose. Major categories for testing and evaluating PCBs include the following

- Visual criteria such as plating quality, solder mask coverage, and workmanship
- Dimensional measurements of the body of the circuit and its design features (e.g., circuit lines and minimum spacing and hole diameters)
- Construction integrity, including such matters as an examination of plated-through hole quality
- Electrical properties such as dielectric withstand voltage and characteristic impedance measurements, if specified.

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- Cleanliness (usually measured in equivalent micrograms of NaCl per square centimeter), a measure that is generally indicative of the potential for latent failures caused by ionic conductive filament growth in moist environments
- Solderability, a measure of the wetting ability of the finish of the circuit
- Environmental properties

Testing requirements for each of the above-mentioned categories are reviewed here in a brief fashion. IPC specifications IPC-6011 and IPC-6012, which are qualification and performance specification for rigid printed boards (superseding the older IPC-RB-276 document), IPC-6013, "Specification for Single- and Double-Sided Flexible Printed Wiring" (superseding the IPC-FC-250A document), and IPC-A-600 are valuable documents that provide precise methods. These are available and are recommended if more detail is sought. Figure 7.37 provides examples of some of the types of defects that might be encountered.

7.14.2 Cross-section evaluation

Inspection of a cross section of a finished plated-through hole on the PCB is normally desired to ensure that the applied metal platings are all within prescribed ranges. It is also possible to get a sense of the quality of the processing using this method. Figure 7.37 gives examples of the types of defects than might be encountered in examining a plated-through hole as received and post solder stress testing.

7.14.3 Electrical testing

Electrical testing is thus recommended for highly complex boards and for boards that are designed to accept and interconnect large numbers of compo-

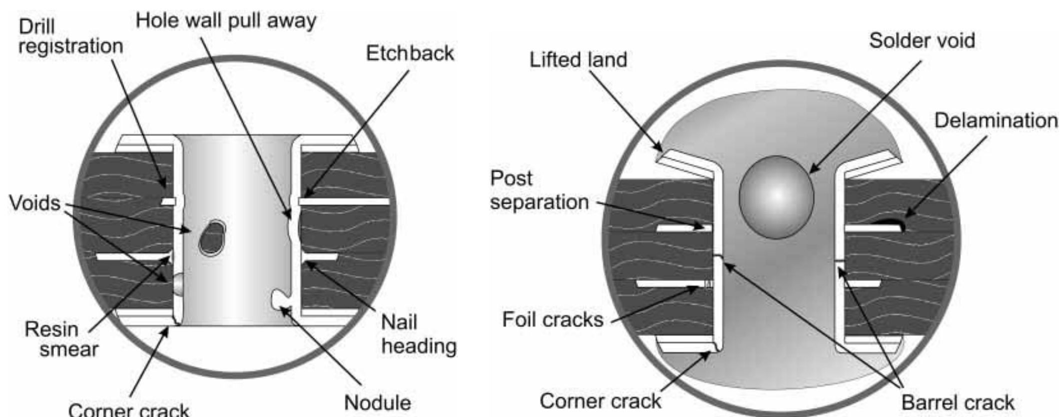

Figure 7.37 Examples of potential copper plating defects that might be encountered in the examination of plated-through hole cross sections. On the left is a hole before solder stress testing, and on the right is an example of a through hole after solder stress testing. Not all defects are cause for rejection; some are simply cause for concern as indicators of possible process control problems.

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nents. Test fixtures (or test programs, in the case of flying-probe-type testers) are not free, but the savings the might be afforded by preventing bad boards from entering the component population assembly operation can be significant. The data for test can be relatively easily extracted from CAD data. Figure 7.38 shows an example of a test fixture.

7.15 Future Directions

The future of printed circuit manufacture is indefinite, except for the fact that one can state with reasonable confidence that there will always be a need for electronic interconnection substrates of some sort. New schemes for manufacturing printed circuits presently in development could radically alter the traditional approaches to manufacture. For example, one company in England (TDAO, Ltd.) is known to be working on a technology that would allow for the direct imaging and plating of flexible circuits in a continuous fashion. This concept would bring the industry closer to realizing the dream of making circuits directly from a computer without the need for film or resist. Another example is a concept for creating metal-core laminates with predrilled and metallized holes that can serve as the raw materials for structures such as represented by the circuits shown in Fig. 7.36.

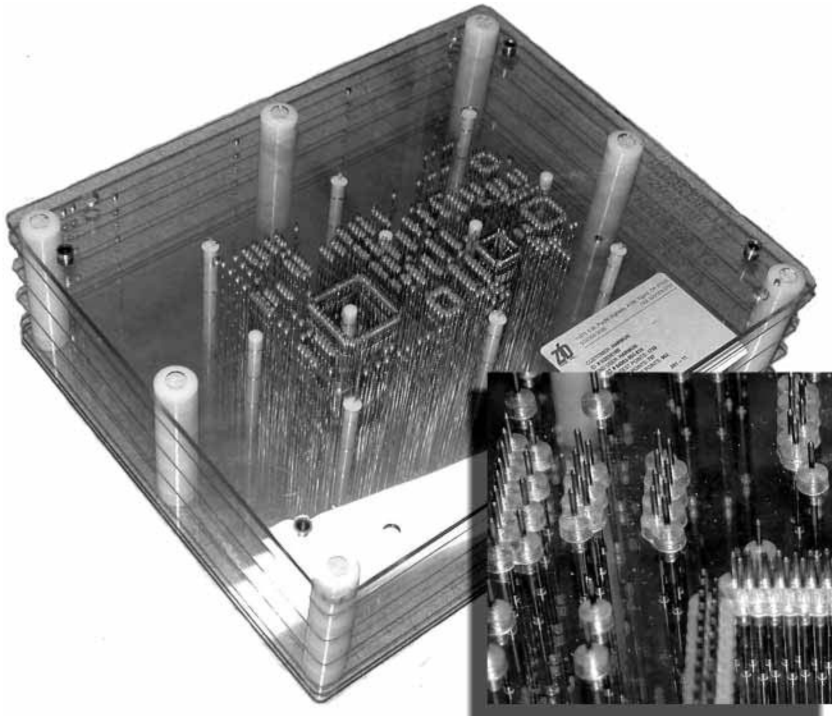

Figure 7.38 Example of a dedicated bed-of-nails test fixture. The insert shows a close-up view. *(Photo courtesy of Zero Defects, Santa Clara, California.)*

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Printed Circuit Board Fabrication

While no one can predict the future with absolute certainty, one thing that seems relatively certain in printed circuit manufacture is that the circuit traces and spaces, and the holes that connect them, will continue to get smaller with time. Of these two trends, the one that is likely to be most important is making smaller holes. Small holes are the key to improving circuit routing.

7.16 Summary

Printed circuits have had a long and colorful history, and they remain among the most important elements of electronic manufacture. There are numerous types of printed circuits and numerous approaches to their manufacture. With the ever expanding electronics market and the myriad of products that are being manufactured, there will likely be continuing increase in the number of different types of electronic interconnection substrates and printed circuits in the years to come.

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