Chapter

10

Thermal Management Materials and Systems

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10.1 Introduction

Heat is an unavoidable by-product of every electronic device and circuit,[1] and it needs to be minimized to improve reliability and maximize electrical performance. Managing this heat, commonly referred to as *thermal management,* requires an understanding of thermodynamics and an in-depth knowledge of the materials.

This chapter, which provides both an introduction into thermal management of electronic packaging and descriptions of the various materials used, is intended not only for thermal management experts but also for those in related fields who have a need to model and optimize their physical designs.

The trend in electronic packaging has been to reduce size and increase performance. This can be seen in the higher levels of integration in semiconductors and the increased usage of hybrids and multichip modules (MCMs). Intel's first microprocessor, the 4004, had 2,300 transistors. The latest microprocessor, the Pentium 4*, has 42 million transistors.[2] Placing more functions in a smaller package has resulted in higher heat densities, which mandate that thermal management be given a high priority in design so as to maintain system performance and reliability. As clock rates increase every year, the power dissipated in the semiconductors during switching is increasing at a linear rate, proportional to frequency as shown by the following equation:

* Pentium is a registered trademark of Intel Corporation.

$$P = \frac{CV^2}{2} f \tag{10.1}$$

where C = input capacitance in farads
V = peak-to-peak voltage swing of signal in volts
f = switching frequency in hertz

If the values of input capacitance and voltage swing had remained the same while the clock frequency increased, the amount of power dissipated would have grown at an exponential rate and would be unmanageable. Luckily, the thermal designer has been aided with reduced input capacitance for each new generation of integrated circuits. In addition, voltage swings, which are directly tied to logic power supply voltages, have been undergoing reduction from the classic 5.0 V to a forecast <1 V.[3]

The initial sections of this chapter review basic heat flow theory as applied to electronic packaging. Next, the various packaging methods and their materials are investigated. Finally, the factors that determine thermal resistance are evaluated.

10.1.1 Temperature effects on circuit operation

Increasing the temperature of an active device typically changes its electrical parameters such as gain, leakage, offset, threshold voltage, and forward drop. These parameter variations over temperature are well documented and incorporated into most circuit simulations. Most circuit designers are aware that leakage currents in active silicon devices approximately double every 10°C. Minimizing the temperature of these devices thus reduces the effect of the leakage currents. If the temperature of an active device increases too much, it will exceed the manufacturer's specifications and usually will fail.

Changing the temperature of passive devices typically changes their values. For example, film resistors have temperature coefficients that range from several to several hundred parts per million per degree Celsius (ppm/°C). Ceramic capacitors, depending on the dielectric material, have temperature variations from 30 ppm/°C to 60 percent over the military or extended temperature range (–55 to +125°C). These changes in electrical parameters are typically not desired. If the temperature increase is high enough, the active or passive device being heated may permanently degrade or even totally fail. Such failures include thermal runaway, junction failure, metallization failure, corrosion, resistor drift and electromigration diffusion. Therefore, the electrical designer needs to minimize any temperature increases. While the designer may not have control over environmental changes, he does have control over the device's self-heating. For analog circuits, he can make the circuits as efficient as possible. For digital circuits, he can select devices that produce the lowest amount of heat for the required clock rates.

In some hybrid and MCM circuits, certain component pairs or groups are designed to track over temperature to achieve the required circuit performance. Typically, resistors, transistors and diodes are components that fall

into this category. For example, in an operational amplifier circuit, as shown in Fig. 10.1, resistors R_1 and R_2 must track to achieve constant gain over temperature. If R_1 were physically located in a cool location on the substrate and separated from R_2, located next to a power transistor whose power level and thus temperature were varying, then the output of the operational amplifier V_{out} would modulate as a function of temperature and power in the transistor. One solution would be to relocate R_2 adjacent to R_1 and isolate it from the power transistor. An alternative solution would be to lower the temperature of the power transistor so that it would have less heating effect on R_2. Techniques to achieve this latter solution include using a larger power transistor, a better thermal die attach, a heat spreader, or a better substrate-to-package attach.

Therefore, to meet both the electrical and thermal performance of a circuit, the designer must thermally and electrically model each device and iterate the design to achieve the required performance. If any devices that must closely track are found to have significant differences, then the physical designer must either select alternate materials or incorporate additional cooling schemes.

10.1.2 Temperature effects on physical construction

With few exceptions, materials expand when their temperature is raised and contract when cooled. The *temperature coefficient of expansion* (TCE) is a parameter found in the literature for each material. Another name for this parameter is the *coefficient of thermal expansion* (CTE). The CTEs and thermal conductivities for various materials used in microelectronic assemblies are detailed in subsequent tables.

Thermal stresses occur when a material is constrained during expansion or contraction. An example of this is a copper heat sink soldered to a metallized ceramic substrate as shown in Fig. 10.2. The ceramic has a CTE of 6.4 ppm/°C, whereas the copper has a CTE of 16.8 ppm/°C. During temperature cycling, in which there are a number of periods of heating followed by cooling periods, the copper expands and then contracts at a higher rate than the ceramic but is

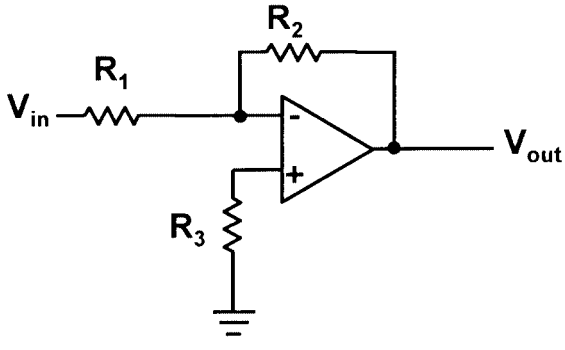


Figure 10.1 Gain tracking of resistors R_1 and R_2.

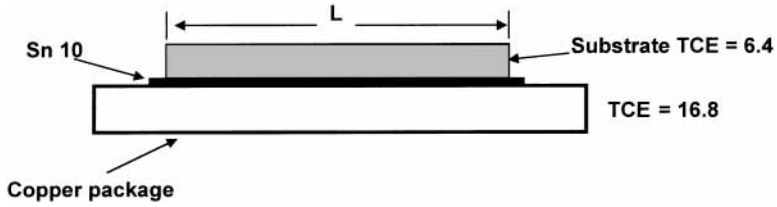


Figure 10.2 Stress example.

constrained. This constraining could result, after time and repeated temperature cycles, in the heat sink bending, the solder joint failing, the ceramic warping, or the ceramic completely failing and cracking.[3] To reduce or eliminate the thermal stresses requires both a selection of the correct materials and a minimization of the temperature changes caused by self-heating.

10.2 Understanding of Thermal Management

10.2.1 Second law of thermodynamics

The second law of thermodynamics states that heat always flows spontaneously from a hotter region to a cooler region as shown in Fig. 10.3. All active and passive devices are sources of heat. These devices are always hotter than the average temperature of their immediate surroundings.

10.2.2 Heat transfer mechanisms

There are three mechanisms for heat transfer: conduction, convection, and radiation, as depicted in Fig. 10.4. These mechanisms and the temperature distribution from the heat source to the surroundings will be discussed in the following sections.

10.2.2.1 Conduction. Thermal conduction is a process in which heat flows through a solid, liquid, or gas or between two media that are in intimate contact. Conduction, the dominant mechanism for heat transfer within solids, involves the transfer of kinetic thermal energy from one electron to another, causing no visible motion of the particles of the body. Conduction through dielectric solids is almost entirely a result of lattice vibrations, whereas conduction through metallic solids has the added energy transport by free electrons. This thermal energy transfer via electrons is similar to that of an electrical

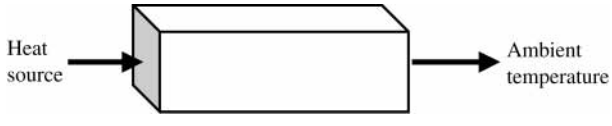


Figure 10.3 Second law of thermodynamics.

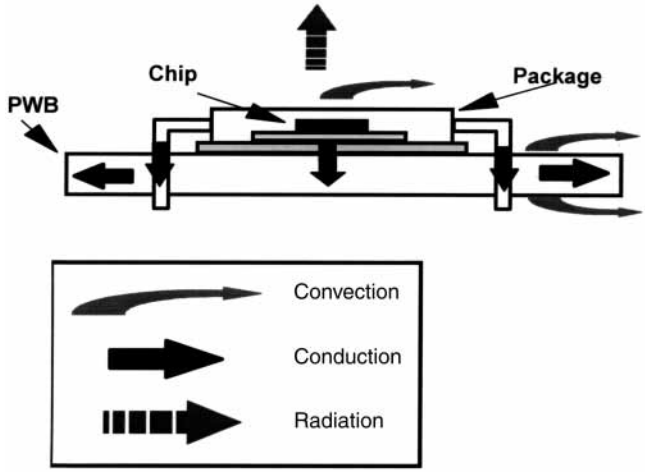


Figure 10.4 Mechanisms of heat transfer.

charge. It is not surprising to find that good electrical conductors such as copper and silver are good thermal conductors.

Fourier's law . Fourier's law of heat conduction, named after the French mathematician, Jean Fourier, states that the rate of heat flow equals the product of the area normal to the heat flow path, the temperature gradient along the path, and the thermal conductivity of the medium. Mathematically, Fourier's law can be expressed as

$$\frac{dq}{dt} = -KA\frac{dT}{dX} \tag{10.2}$$

where K = thermal conductivity of medium, W/m-K or W/in-°C
A = cross-sectional area of medium normal to the heat flow path, in^2 or cm^2
T = temperature of medium, °C
X = position along the medium, in or cm
t = time, sec
q = heat generated per unit volume, joules/cm^3
Q = heat flow in watts normal to the cross-sectional area of heat transfer

$$\frac{dQ}{dt} = \text{power in W or cal/sec} \tag{10.3}$$

$$\frac{dt}{dX} = \text{temperature gradient in °C/in or °C/cm} \tag{10.4}$$

The temperature gradient and the cross-sectional area are defined at the same point X as shown in Fig. 10.5. Heat flow is considered positive when the

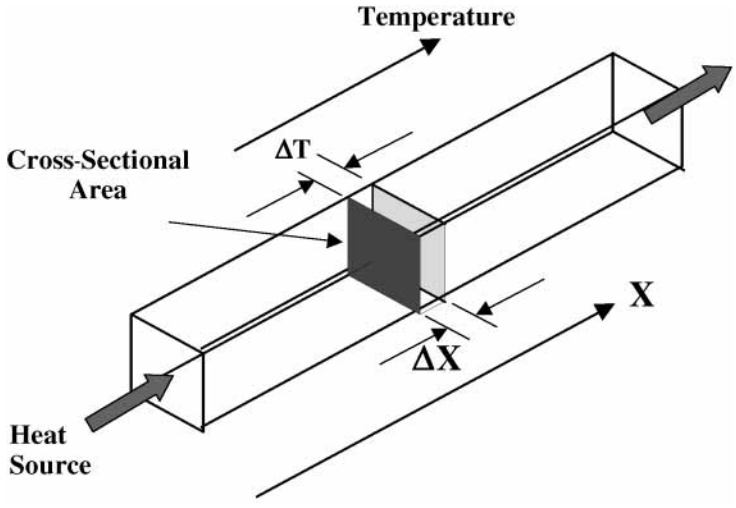


Figure 10.5 Fourier's law of heat conduction.

temperature is decreasing. The thermal conductivity of many materials varies with temperature and will be discussed in subsequent sections. In most cases, this variation with temperature can be considered a second-order effect and contributes only a minor source of error.

Substituting Eq. (10.3) into Eq. (10.2) and rearranging gives the expressions

$$P\,dX = KA\,dT \tag{10.5}$$

$$P\int_{0}^{X} dX = KA\int_{T_2}^{T_1} dT \tag{10.6}$$

Integrating the above over the length from 0 to X, and from the corresponding temperatures T_2 to T_1, the equation reduces to

$$PX = KA\,\Delta T \tag{10.7}$$

Rewriting Eq. (10.7) produces an expression for temperature difference,

$$\Delta T = \frac{PX}{KA} \tag{10.8}$$

The Greek letter theta (θ) is usually used to symbolize thermal resistance and can be mathematically defined using Eq. (10.9).

$$\theta = \frac{X}{KA} \tag{10.9}$$

Combining Eqs. (10.8) and (10.9) gives a relationship between thermal resistance, power, and temperature rise.

$$P\theta = \Delta T \tag{10.10}$$

10.2.2.2 Convection. Convection is the transfer of thermal energy between two surfaces as a consequence of a relative velocity between them.[4] It occurs only in fluids wherein the transfer mechanism is the mixing of the fluids. Although each of the surfaces may be a fluid, the most practical application is where one is a solid surface and the other is a fluid.

The heat loss due to Newtonian cooling (named after Sir Isaac Newton) or convection cooling is proportional to the temperature difference between them. In mathematical terms, this can be written as

$$Q_c = h_c A_s (T_s - T_A) = h_c A_s \Delta T \tag{10.11}$$

where Q_c = heat transferred from a surface to ambient by convection in watts
A_s = surface area in cm^3 or in^3
T_s = surface temperature in °C
T_A = ambient temperature in °C (temperature to which the heat is being transferred)
h_c = convection heat transfer coefficient in W/cm^3-°C or W/in^3-°C

Because h_c is both position and temperature dependent, convection heat transfer solutions are more complex than conduction solutions. Many analysts use a simplifying approximation in which the average surface temperature is used in conjunction with an average heat transfer coefficient, h_c.

Equation (10.11) can be rewritten as:

$$\Delta T = \frac{1}{h_c A_s} Q_c \tag{10.12}$$

The term θ_S can be defined as the convective surface thermal resistance.

$$\theta_S = \frac{1}{h_c A_s} \tag{10.13}$$

It should be noted that Eq. (10.13) is not a law of heat transfer as seen in Fourier's law but is a definition of the heat transfer coefficient. This definition simply states the quantity of heat transferred through a temperature difference. This temperature coefficient actually depends on the surface and surrounding temperatures, fluid velocity (for forced convection), fluid viscosity, fluid density, and surface geometry.

There are two types of convection cooling: natural (or free) and forced. In natural convection cooling, heat flows by conduction or contact from the surface to the fluid particles in intimate contact with the surface. The fluid parti-

cles increase in internal energy, causing the density of the nearby fluid to decrease. Buoyant forces then cause the particles to move to a region lower in temperature where further energy transfer takes place by conduction. There is a resulting boundary layer of hot air immediately adjacent to the surface. Natural convection is caused entirely by differences in density within the fluids resulting from different temperatures and does not use externally forced air movement.

In forced convection, the thermal energy is transferred from the solid to the adjacent fluid particles in the same manner as in natural convection. However, the subsequent fluid action occurs through artificially induced fluid motion generated by fans, pumps, or blowers. There are three types of air-moving devices: centrifugal, propeller, and axial flow. Centrifugal fans are designed to move small volumes of air at high velocities and are capable of working against a high resistance. Propeller types are designed to move large volumes of air at low velocities. Axial flow fans are an intermediate type of air mover between the centrifugal and propeller types.

Forced convection can be divided into laminar flow and turbulent flow. For air, the transition from laminar to turbulent flow usually occurs at a velocity of 180 linear feet per minute (LFM). The heat is transferred by molecular conduction in the fluid and by the solid–fluid interface. Turbulent flow, characterized by the irregular motion of fluid particles, has eddies in the fluid in which the particles are continuously mixed and rearranged. The heat is transferred from the eddies back and forth across the streamlines. The greater heat transfer occurs for turbulent flow.

For forced convection, the convection heat transfer coefficient is calculated from

$$h = B\frac{V^{0.75}}{L^{0.25}} \tag{10.14}$$

where B = constant of air properties and surface configuration
V = linear velocity of air in cm/sec or in/sec
L = characteristic length of surface in direction of flow in cm or inch

As can be seen in Eq. (10.14), the linear velocity of the air current as it passes the dissipating element is the key factor to the amount of heat that can be removed.

For natural or free convection, the convection heat transfer coefficient is calculated by

$$h = DE\frac{\Delta T^{0.25}}{L^{0.25}} \tag{10.15}$$

where D = constant for air properties (see Fig. 10.6)
E = constant for surface configuration ($E = 1.9 \times 10^{-4}$ for a flat plate)

L = characteristic length in centimeters or inches of dissipator surface with area factor
ΔT = temperature difference in °C between dissipator and ambient air

10.2.2.2.1 Natural convection cooling example. A flat plate with a characteristic length of 2.0 in (assumed value for this example), shown in Fig. 10.6c, can be considered to be a model for a flat heat sink. The plate size is 2.0 × 2.0 in. The plate bottom is at 125°C, and the ambient air is 25°C. The value of D for this configuration is 0.26 (from Fig. 10.6c). Calculating the value of the convective transfer heat coefficient h_c, from Eq. (10.15),

$$h_c = DE\frac{\Delta T^{0.25}}{L70.25} = 0.26 \times 1.9 \times 10^{-4}\frac{(125-25)^{0.25}}{2.0^{0.25}} = 1.31 \times 10^{-2}$$

The convection surface thermal resistance is

$$\theta_s = \frac{1}{h_c A_s} = \frac{1}{1.31 \times 10^{-2} \times 4} = 1.9°\text{C/W} \tag{10.16}$$

10.2.2.2.2 Forced convection example. Air with a velocity, V, of 500 ft/min is blown across a plate with a characteristic length L of 2.0 in. The surface area A is 4.0 in^2, and the air property/surface configuration constant B is 1.0×10^{-3}. From Eq. (10.14),

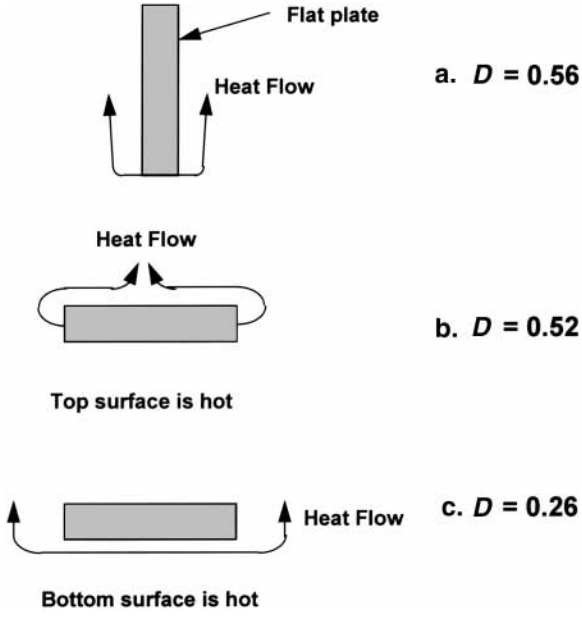


Figure 10.6 Value of D in Eq. (10.15).

$$h = B\frac{V^{0.75}}{L^{0.25}} = 1.0 \times 10^{-3}\frac{(500 \times 12)^{0.75}}{2^{0.25}} = 0.482 \text{ W/in}^2\text{-°C} \tag{10.17}$$

The thermal resistance is

$$\theta_s = \frac{1}{hA_S} = \frac{1}{0.482 \times 4} = 0.518\text{°C/W} \tag{10.18}$$

The above discussion of convection cooling points out that this heat removal method is wholly dependent on the movement of the fluid surrounding the heat-dissipating element. A brief review of the thermal conductivities of the various gases present in packaging will be presented. Because this chapter delves only into thermal management materials, there will be no further discussion of convection cooling.

10.2.2.3 Radiation cooling. All objects with a temperature above 0 kelvins emit thermal radiation. Radiation cooling is the transfer of heat by electromagnetic emission, primarily in the infrared wavelengths (0.1 to 100 μm). Because radiation cooling does not require a transport medium, it is the only means of cooling in a complete vacuum. Specifically, radiation cooling is maximized when there is no intervening material.

Radiation from solid objects may be considered to be a totally surface-related phenomenon that is electromagnetic in character.

Temperature radiators can be broken into two classes: *black bodies* and *non-black bodies*. Non-black bodies can be further broken down into gray bodies and selective radiators. A visibly black surface absorbs all visible light that falls upon it. Its thermal analogy is called a black body and is defined as a surface that absorbs the entire thermal radiation incident upon it, neither reflecting nor transmitting any of the incident radiation. The emissive power of a black body or surface is defined as E_b. Good absorbing materials are also good emitting materials. The black body, at any given temperature, radiates more energy, both in the total spectrum and for each wavelength interval, than any other temperature radiator and more than any non-black body at the same temperature.[6]

Real surfaces do not radiate precisely as described by black-body equations, because no surface is ideally black. Lampblack and some finely divided metals approach a black body in certain parts of the spectrum. The actual monochromatic emissive power of a real surface is always less than E_b. The emissivity of a body or surface (ε) is defined as the ratio of the radiated flux (E) emitted by a body to that (E_b) emitted by a black body at the same temperature.

$$\varepsilon = \frac{E}{E_b} \tag{10.19}$$

A black body or perfect emitter would have an ε of 1.0. A perfect reflector would have an ε of 0. Listed in Table 10.1[5] are the emissivities for various ma-

TABLE 10.1 Emissivities of Surfaces at 80°F

Surface type	Finish	Emissivity, ε
Paint	Black (flat lacquer)	0.96–0.90
Paint	Gray	0.84–9.91
Paint	White	0.80–0.91
Paint	White epoxy	0.91–0.95
Paint	Aluminum silicone	0.020
Metal	Nickel	0.21
Metal	Aluminum	0.14
Metal	Silver	0.10
Metal	Gold	0.04–0.23
	Specialty surfaces	
Metal	Aluminum (sandblasted)	0.41
Metal	Aluminum (black anodized)	0.86
Metal	Nickel (electrolysis)	0.06–0.17
Metal	Aluminum (machine polished)	0.03–0.06
Metal	Gold (electrodeposited or polished)	0.02
Ceramic	Cermet (ceramic containing sintered metal)	0.58
Metal	Brass (highly polished)	0.58
Metal	Copper (polished)	0.018
Metal	Nickel (polished)	0.070
Metal	Silver (polished)	0.02–0.03
Glass	Smooth	0.9–0.95
Metal	Alodine* on aluminum	0.15

*Registered trademark of Achem Products, Inc.

terials used in microelectronic applications. Aluminum, a low-cost material with a high thermal conductivity, has a low emissivity of 0.04 in a polished state. After black anodization, aluminum's emissivity is significantly increased to 0.80.

A *gray body* is defined as a radiator that has the same spectral emissivity for all wavelengths. A *selective radiator* is one in which the emissivity varies with wavelength.

The rate of emission of radiant energy from the surface of a body, R, can be expressed by the Stefan-Boltzmann law shown in Eq. (10.20).

$$R = \varepsilon\sigma T^4 \tag{10.20}$$

with R defined as

$$R = \frac{Q}{A} \text{ W/m}^2 \tag{10.21}$$

where ε = surface emissivity in joules/sec-cm^2

σ = Stefan-Boltzmann constant (3.65×10^{-11} watts/ in^2-K^4)

Q = heat transferred in watts
A = radiating surface area in meter^2
T = temperature of surface in kelvins

Combining Eqs. (10.20) and (10.21),

$$Q = \varepsilon\sigma A T^4 \tag{10.22}$$

The heat transferred via radiation between two black body surfaces ($\varepsilon = 1$) in which one body is completely enclosed by the other (and the internal body cannot see any part of itself) may be calculated by

$$Q = A\sigma(T_1^4 - T_2^4) \tag{10.23}$$

where T_1 = temperature of "hot" body in K
T_2 = temperature of "cold" body in K (air molecules or other absorbing body)

For non-black body surfaces, the heat transferred via radiation is

$$Q = SA\varepsilon\sigma(T_1^4 - T_2^4) \tag{10.24}$$

where S = shielding factor or view factor

The shielding factor (or view factor), S, whose value ranges from 0 to 1, is a measure of how well the emitter sees the absorber. Typical values of shielding factors are shown in Table 10.2.

TABLE 10.2 Shielding Factors for Various Configurations[3]

Configuration	Shielding factor
Infinite parallel plates or planes	1.0
Body completely enclosed by another body, internal body cannot see any part of itself	1.0
Two squares in perpendicular planes with a common side	0.20
Two equal, parallel squares separated by a distance equal to the side	0.19
Two equal, parallel circular disks separated by a distance equal to the diameter	0.18

The above discussion on radiation cooling points out that this heat removal method is dependent on the temperature difference between objects, their emissivity, and the shielding factor. From a materials standpoint, the physical designer can optimize the thermal design with the emissivity parameter.

10.2.2.3.1 Radiation example (non-black body). The bottom of a heat sink is at 150°C while the ambient air is at 25°C. The heat sink is nickel plated with a surface area of 4.0 in^2. The shielding factor is 1.0. The amount of heat transferred by radiation is calculated from Eq. (10.24).

$$Q = P = SA\varepsilon\sigma(T_1^4 - T_2^4)$$

$$= (1)(4)(0.11)(3.65 \times 10^{-11})[(150 + 273)^4 - (25 + 273)^4] = 0.388 \text{ W} \quad (10.25)$$

If the heat sink bottom temperature is changed to 125°C, then

$$T_2 = 125°\text{C}, \qquad Q = 0.111 \text{ W}$$

10.3 Unit Conversions

Comparisons of the thermal properties of materials is often made difficult by the fact the values use different units. To aid the reader, conversion factors between metric and English units for various physical parameters are listed in Table 10.3.

10.4 Packaging Overview

Before looking at the various materials used in electronic packaging from a thermal management standpoint, it is necessary to take a global look at the various packaging technologies and how they fit together. This chapter will look at first-level of packaging—the chip(s) in a package—and the second level of packaging—the circuit card.

Semiconductors are packaged for four basic reasons.

1. The package provides mechanical support to the semiconductor.
2. The package provides interconnections of the semiconductor(s) to the next level of packaging.
3. The package provides environmental protection of the semiconductor(s).
4. The package provides a method of removing the heat dissipated by the semiconductor(s).

10.4.1 Single-chip package

The lowest level of packaging is the single-chip package (SCP). In this package, the chip is mounted to the package base with a die attach material, interconnected, and sealed either hermetically or via encapsulation. An example of the SCP is shown in Fig. 10.7, which depicts a custom ASIC in a ball grid array package. This process is varied for flip-chips wherein the balls on the die are mass reflowed to the package and then sealed.

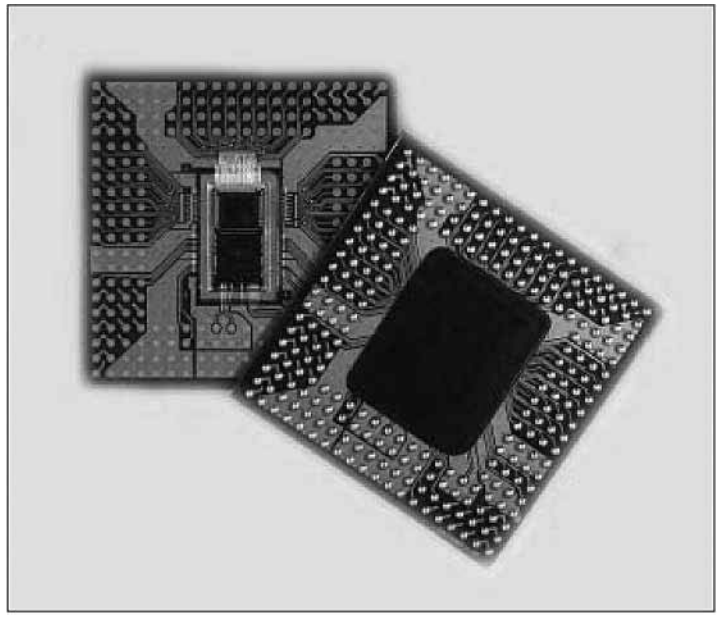


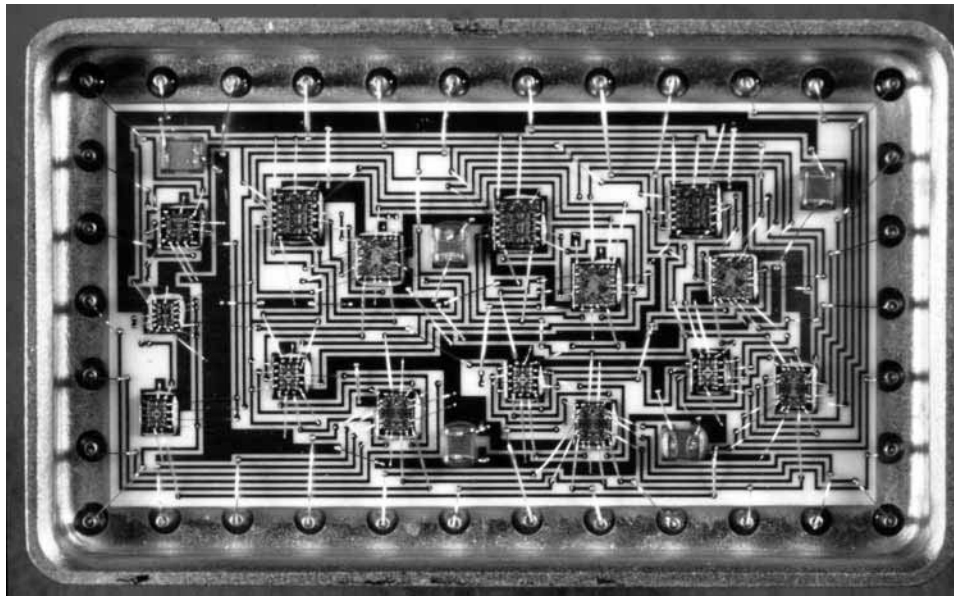
Figure 10.7 Single-chip package.

10.4.2 Multichip package

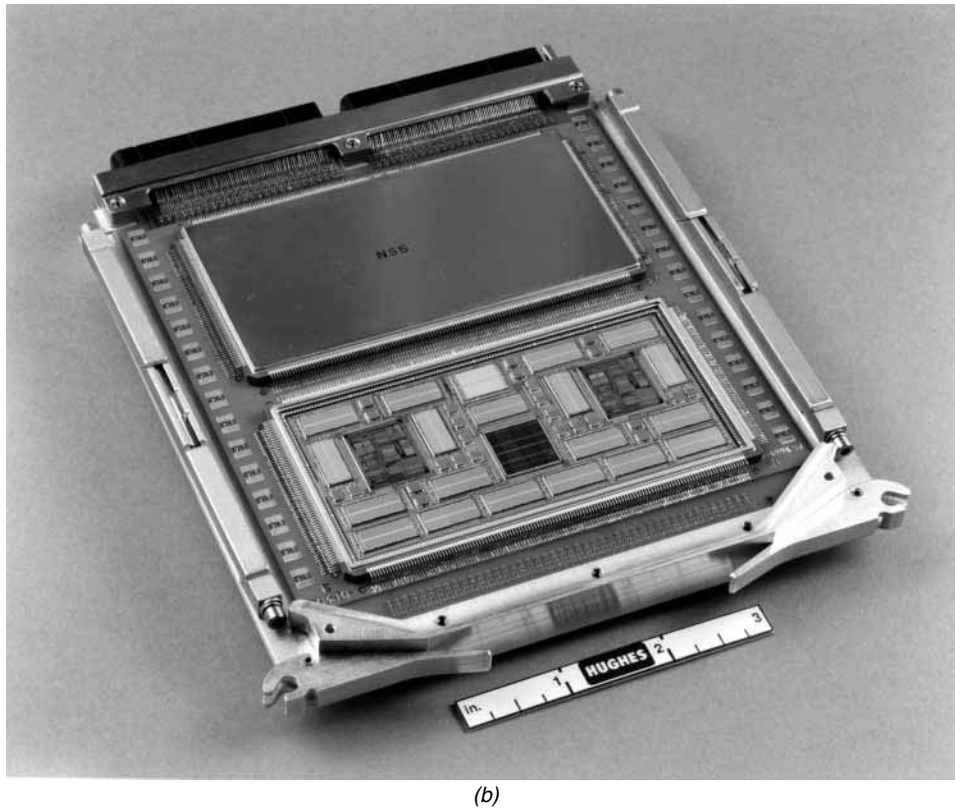
Multichip packaging has been used by the electronics industry since the mid 1960s. First known as hybrids, they placed several semiconductors and passive devices on a substrate housed in one package. The typical package used for the first hybrids was the TO-5. A more recent hybrid is shown in Fig. 10.8a. Over the years, multichip packaging technology has evolved in size, number of I/Os, and complexity to a point at which complete subsystems have been placed in a single package. The highest density of multichip packaging has been named the multichip module (MCM). An example of an MCM with 442 I/Os is shown in Fig. 10.8b. Another name for high-density multichip packaging is *system-in-package* (SiP). A variant of multichip packaging is the *few chip package* (FCP).

10.4.3 Board level

Once the semiconductors are packaged, they need to be attached to the next level of assembly—the circuit card. The electrical interconnections are typically made with a low-temperature solder. For many package types, this electrical connection also acts as the mechanical connection. However, for large devices, additional mechanical attachment is necessary. This may be in the form of adhesives or actual clamping to the circuit card. The additional attachment materials may also aid in removing the heat from the device. Even if the lead attachment is sufficient for holding the package on the circuit card, ther-



(a)



(b)

Figure 10.8 *(a)* Hybrid microcircuit and *(b)* multichip modules assembled on SEM-E frame.

TABLE 10.3 Units and Conversion Factors

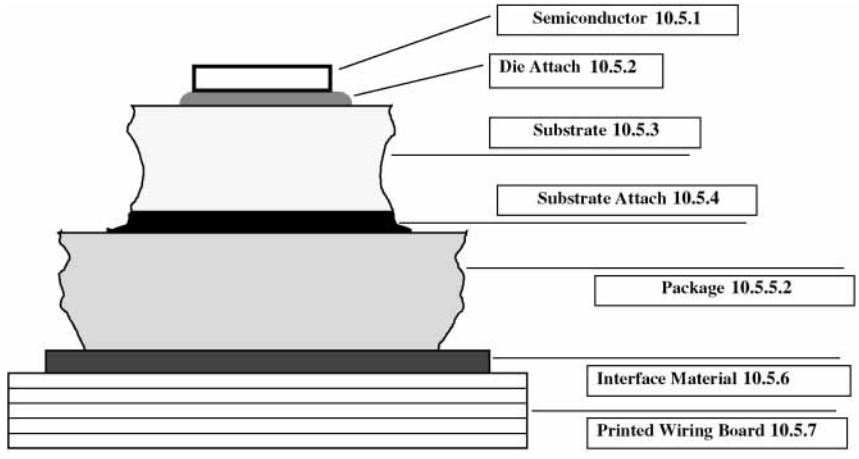
Length, area, and volume
1 in = 25.4 mm = 0.0254 m
1 in = 2.54 cm
1 in = 25400 μm (microns)
12 in = 1 ft
1 ft = 305 mm = 0.305 m
$1\ in^2 = 645\ mm^2 = 0.6452 \times 10^{-3}\ m^2$
$1\ ft^2 = 92{,}880\ mm^2 = 0.0929\ m^2$
$1\ in^3 = 16{,}380\ mm^3 = 16.38 \times 10^{-6}\ m^3$
$1\ ft^3 = 0.0283\ m^3$
Mass
1 lb (mass) = 0.45359 kg = 453.59 g
1 oz = 28.35 g
Density
$1\ lb/in^3 = 27680\ kg/m^3$
$1\ lb/in^3 = 27.68\ g/m^3$
$1\ lb/ft^3 = 16.0185\ kg/m^3$
Pressure
$1\ lb/in^2$ (psi) = 6,894.76 N/in^2
$1\ lb/ft^2$ (psf) = 47.9 N/in^2 = 0.0069 psi
$1\ MPa = 10^6\ N/m^2 = 1\ N/mm^2$
1 atm = 101325 Pa
$1\ dyne/cm^2 = 0.1$ Pa
$1\ kg/cm^2 = 14.22$ psi
Force
1 lb (force) = 4.448 N
1 gm (force) = 980.665 dyne
$1\ dyne = 10^{-5}$ N
$1\ dyne = 2.248 \times 10^{-6}$ lb

Work
1 in-lb (force) = 0.113 J = 0.113 Nm
1 ft-lb = 1.365 J
1 BTU = 778 ft-lb = 252 calories = 1,055 J
Energy
1 calorie (cal) = 4.186 J
$1\ erg = 10^7$ J
1 electron volt (eV) = 1.60×10^{19} joule
1 W-sec = 1J
Power
1 BTU/hr = 0.293 W
1 cal/sec = 4.18 W
1 ft-lb/sec = 1.356 W
1 ft-lb/mm = 0.0226 W
Thermal conductivity
1 BTU/hr-ft-°F = 1.7303 W/m-K
1 BTU/hr-in-°F = 0.1442 W/m-K
1 W/in-K = 39.3 W/m-K
1 cal/sec-cm-K = 418.4 W/m-K
Specific heat
1 cal/g-°C = 4.17 W-sec/g-°C
1 BTU/lb-°F = 4.1867 W-sec/g-°C
Temperature
1°C = 33.8°F
0°C = 273.15 K

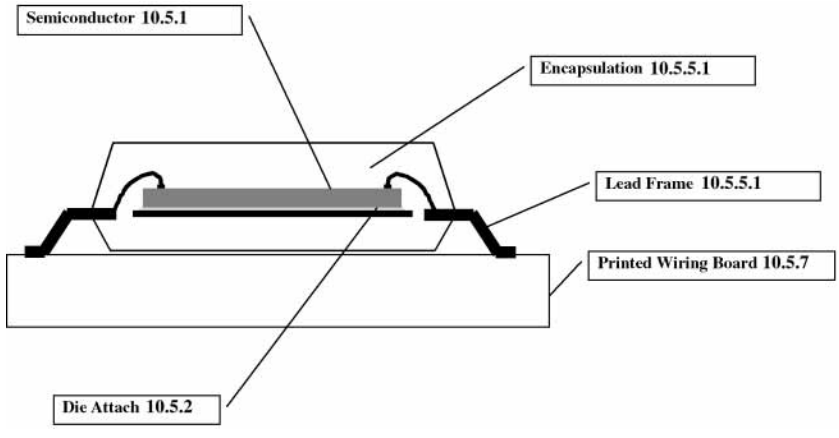
mal interface material may be required between the package and the board. A discussion of these materials can be found in Sec. 10.5.6.

10.5 Packaging Materials

Figure 10.9 shows cross-sectional views of the various types of electronic packaging. The constituent materials used in each type of packaging are referenced to the applicable section of this chapter.



(a)



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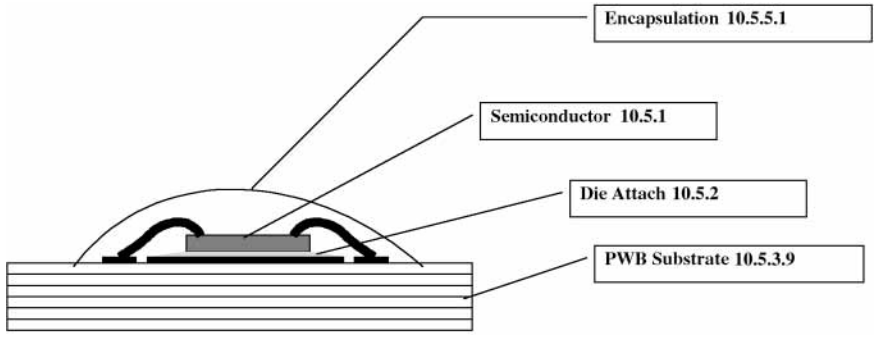

(c)

Figure 10.9 Cross-sectional views of various package types: *(a)* hybrid microcircuit, *(b)* PEM, and *(c)* COB.

10.5.1 Semiconductors

10.5.1.1 Silicon and germanium. The first transistors were fabricated with germanium (Ge) semiconductor material, which has a reasonably good thermal conductivity of 77 W/m-K. However, germanium suffers from an inherent leakage problem that limits the maximum operating temperature to the range of 90 to 120°C. Silicon transistors, invented at Texas Instruments in 1954, have maximum operating junction temperatures in the range of 150 to 200°C.[9,10] Forty years later, over 90 percent of all semiconductors are fabricated from silicon, which has a thermal conductivity of 150 W/m-K at 25°C.[11]

Table 10.4 lists the thermal conductivities of various semiconductor materials at 25°C. The variation of the thermal conductivity at temperature for several of these materials is shown in Fig. 10.10.

TABLE 10.4 Thermal Conductivities of Semiconductor Materials[3,13,23]

Material	Thermal conductivity @ 25°C (W/m-K)
Silicon	150
Silicon germanium	150
Silicon carbide	155
Gallium arsenide	45
Indium phosphide	97
Germanium	77
Gallium phosphide	133
Gallium antimony	33
Gallium nitride	16–33
Indium arsenide	35
Indium antimony	19

10.5.1.2 Compound semiconductors. To obtain higher performance than silicon in either frequency or temperature range, compound semiconductors were developed using materials such as gallium arsenide, indium phosphide, indium arsenide, indium antimony, gallium phosphide, gallium antimony, and silicon carbide.

For high-frequency applications, typically starting at 1 GHz, gallium arsenide (GaAs) is used as the semiconductor material because of its higher mobility. Because of its high-frequency performance, gallium arsenide has found its way into a variety of applications ranging from cellular telephones to military radars. Other materials used for high-frequency operation include indium phosphide, indium arsenide, indium antimony, gallium phosphide, and gallium antimony.

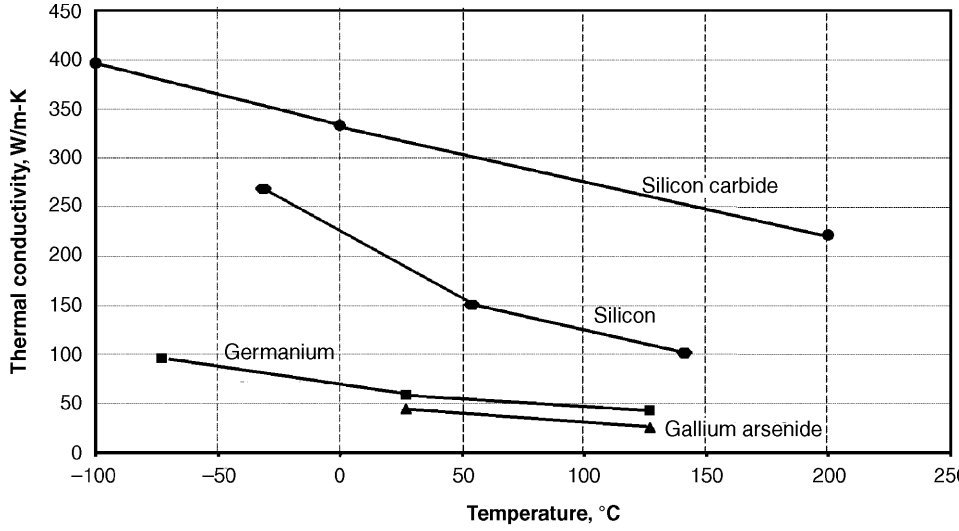

Figure 10.10 Variation of the thermal conductivity of various semiconductor materials at temperature.

To achieve maximum high-frequency performance from gallium arsenide, circuit geometries are made extremely small. This increased power density, coupled with the lower thermal conductivity (35 W/m-K), makes the packaging of gallium arsenide a significant challenge to the physical designer. One technique commonly used with gallium arsenide to lower the thermal resistance is to thin down the wafers. Gallium arsenide chips are also thinned so as to reduce the impedance of through-hole vias from the top to the bottom of the chip. Typical thicknesses of gallium arsenide used in the microelectronic assemblies are 0.006 and 0.002 in.

A new compound semiconductor material, silicon-germanium (SiGe), is fabricated by selectively introducing germanium as a dopant into the base region of the transistor. The processing of silicon-germanium wafers is done using the same equipment as standard silicon. The resulting silicon-germanium material produces a semiconductor that offers comparable high-frequency performance to gallium arsenide at a significantly lower cost. An example of the high-frequency capability of the silicon-germanium process is IBM's recently demonstrated 210-GHz silicon-germanium transistor. The amount of germanium in silicon-germanium is small. Therefore, the thermal conductivity can be considered to equal that of silicon.[15–17]

Silicon carbide (SiC) is a compound semiconductor material that is finding its way into a variety of applications. With a wide band gap of 3.1 eV (versus 1.1 eV for silicon), heat does not readily disrupt the performance of silicon carbide semiconductors. In addition to the wide band gap, silicon carbide has a high thermal conductivity: 333 W/m-K at 25°C and 221 W/m-K at 200°C. As a result, silicon carbide semiconductors are being used in a variety of high-temperature applications. Silicon carbide has a high maximum electron velocity, which allows devices to operate at high frequencies.[14,18,19]

Indium phosphide is a new compound semiconductor material being used for high-frequency electronic and optoelectronic devices with the potential of integrating both on a single chip. Indium phosphide's relatively high thermal conductivity of 97 W/m-K allows it to be used in high-power-density applications.[20,21]

Gallium nitride (GaN) is a developing semiconductor material with a wide bandgap that can effectively handle large amounts of power and operate at frequencies up to 40 GHz. While the thermal conductivity of gallium nitride is a low 16 to 32 W/m-K, it has a power density that is many times that of gallium arsenide and indium phosphide. Gallium nitride is finding applications such as power amplifiers in base stations.[22,23]

10.5.2 Die attach materials

Except for flip-chip-attached devices, all die are bonded to the next assembly (the substrate or package) active area facing up with a die-bond adhesive. It is the die bond that absorbs the thermal mismatch between the die and the package or substrate. Thus, the die bond is susceptible to fatigue fracture. The adhesives fall into two categories, soft and hard. Soft adhesives include organics, polymers, and lead-based solders. Hard adhesives include gold-based eutectics (gold-silicon, gold-germanium, and gold-tin), silver-based solder (Sn 96), and silver-glass.

10.5.2.1 Gold-silicon eutectic. Eutectic die attachment is based on the gold-silicon eutectic point at 370°C. In this process, the die is mechanically scrubbed with a gold-silicon perform on a substrate or a ceramic package at temperatures between 390 and 450°C under a nitrogen shroud. On semiconductors with no backside metallization, the scrubbing breaks down the thin layer of silicon on the back of the chip and combines it with another metal, usually gold. For gold-backed semiconductors, the gold-silicon perform is reflowed and attaches the die to the underlying metallization. The resulting gold-silicon eutectic structure is approximately 0.001-in thick and has a thermal conductivity of 27 W/m-K.[13]

10.5.2.2 Solders. For semiconductors metallized with non-gold metals such as titanium-nickel-silver, other eutectic solders are used. These include gold-tin, with a eutectic temperature of 280°C; gold-germanium, with a eutectic temperature of 361°C; and Sn 96, with a eutectic temperature of 221°C. (Note that gold-tin, gold-germanium, and Sn 96 can be used with both gold-backed and non-gold-backed die.) Other solders used for die attach include a variety of lead-tin and indium-lead solders. The thermal conductivities of the various solders used as die attach adhesives are listed in Table 10.5.[38] Preforms of gold-tin, gold-germanium, and Sn 96 come in various thicknesses, starting at 0.001 in. Solder pastes, a mixture of solder particles and flux, are available for a number of solder alloys for use in dispensing, screen printing, and stencil-

TABLE 10.5 Thermal Properties of Solders[38]

Solder	Composition	Thermal conductivity @25°C (W/m-K)	CTE, (ppm/°C)
Gold-silicon	96.85 Au, 3.15 Si	27	12.3
Gold-tin	80 Au, 20 Sn	57	15.9
Gold-germanium	88 Au, 12 Ge	44	13.4
Sn 10	90 Pb, 10 Sn	36	27.9
Sn 96	3.5 Ag, 96.5 Sn	33	30.2
Sn 62	2 Ag, 36 Pb, 62 Sn	42	27
Sn 63	37 Pb, 63 Sn	51	25
Sn 60	40 Pb, 60 Sn	29	27
Indium-lead	30 Pb, 70 In	38	28
Indium-silver	3 Ag, 97 In	73	22

ing. When solder pastes are used, there is a possibility of creating voids in the die attach as a result of flux entrapment. This is discussed in Sec. 10.6.2.

The lack of plastic flow in hard adhesives leads to high stresses in the silicon chip as a result of the CTE mismatch between the substrate/package and the die.[24]

10.5.2.3 Silver-glass. As semiconductors grew in complexity from medium scale integration (MSI) to large scale integration (LSI), and in size past 0.2 inches square with power densities exceeding 32 W/in^2 (5 W/cm^2), the eutectic die attach process became inadequate. Assembly houses could not provide high enough void-free attachment in volume to meet the thermal resistance requirements. In addition, the CTE mismatch between silicon at 3.6 ppm/°C and 92 percent alumina packages at 7.2 ppm/°C was introducing significant reliability-decreasing stresses.[13]

Silver-glass die attach materials were developed to provide void-free die attach with low thermal resistance. Composed of approximately 60 percent silver flake, 20 percent glass, and 20 percent organic binders that are burned off completely during the processing, silver-glass has a thermal conductivity ranging from 60 to 80 W/m-K, depending on the manufacturing formulation. This is an order of magnitude higher than epoxies. See Table 10.6 for details. Silver-glass is applied to the semiconductor package or to the substrate with dispensing equipment to provide an after-firing bond line of 0.002 in minimum.[28] Typical processing temperatures for silver-glass die attach are 400 to 420°C.[26] Owens has reported that there was no cracking of die when attached with silver-glass.[28] The same die, when attached eutectically, was exhibiting cracking. The thermal properties of several silver-glass compositions are listed in Table 10.6.

TABLE 10.6 Thermal Properties of Silver-Glass[25–27]

Material	Thermal conductivity @25°C (W/m-K)	CTE (ppm/°C)
QMI3555R	>80	16
QMI2419MA	>60	21
DM-3030	70	19.7
JM4720	78.3	17

10.5.2.4 Organic adhesives. Polyimides, cyanate esters, and epoxies filled with precious metals are widely used for die attach in all types of packaging. Their ease of application and low processing temperatures have made them the die attach material of choice in many applications. These organic adhesives are typically filled with a metal to provide the required electrical and thermal conductivity. Silver is the most common fill material. In selected applications, gold and copper are used as the fill material. To improve the thermal conductivity of organic adhesives, some manufacturers add electrically insulating materials such as boron nitride, aluminum nitride, alumina, and CVD diamond as fillers.

For single-chip packaging, dispensing and stamping are the preferred methods of application of organic adhesives. In multichip applications, the adhesives are typically screen printed or dispensed. With the proper dispensing pattern, void-free die attach can easily be achieved.

Many polymers come as a preform in which a carrier is impregnated with epoxy. Typical carrier materials are fiberglass and Kapton.* These preforms provide an extremely uniform material thickness. Preforms with thicknesses as thin as 0.0015 in are available for use in die attach. Thicker preforms, up to 0.006 in thick and unfilled, are typically used for substrate attachment in multichip applications. These are discussed in Sec. 10.5.4.

Polymers are grouped into two categories—thermoplastics and thermosets. Thermoplastics, made from ground cured resins and mixed with fillers and a solvent, are capable of softening or melting when heated and return to a solid when cooled. Because of the presence of the cured resins, thermoplastics do not require any subsequent curing. Thermosets, typically referred to as *epoxies,* are uncured or partially cured. They do not have the reversible phase-change behavior of thermoplastics. The thermal conductivity of both thermoplastics and thermosets is a first-order function of the type and amount of filler material. When used for die attach, the typical filler material is silver. Because thermoplastics do not require a cure, the bond line they form is dense and void-free, with a resulting higher thermal conductivity. Thermosets, which require a cure, have small voids caused by shrinkage during curing that result in a lower-density bond line and thus a lower thermal conductivity.[31,32]

* Kapton is a registered trademark of DuPont.

Polyimide and cyanate ester adhesives, both metal-filled and unfilled, are more thermally stable than epoxy adhesives and are used for higher-temperature applications such as furnace sealing. Epoxies have a maximum temperature range of 175°C to 250°C, depending on their composition. Polyimides, stable to 400°C to 500°C, have thermal conductivities close to 0.16 W/m-K.[19] Silver-filled cyanate esters, stable to over 400°C have thermal conductivities of approximately 1 W/m-K.[33] The thermal conductivities of polyimide and cyanate ester die attach adhesives are extremely low. However, because their thickness is on the order of 0.001 inch or less, the resultant thermal resistance of the die attach, while not low, is acceptable for low to medium power densities.

Thermoplastic and thermoset adhesives come in both a paste and a preform. The critical thermal parameters for both materials are the thickness of the die attach and its uniformity. The screen printing and dispensing processes can provide uniform bond lines. By definition, the preform provides a uniform thickness. Table 10.7 lists the thermal conductivities of various organic adhesives used for die attach.

10.5.3 Substrates and metallizations

In all multichip applications and selected single-chip applications, the dice are attached to a substrate that provides interconnection as well as electrical isolation from the package. This substrate material can be a ceramic, a metal with insulating dielectric, or an organic. Ceramic substrate materials include alumina, beryllium oxide, low-temperature cofired ceramic (LTCC), and aluminum nitride. Table 10.8 lists the thermal properties of inorganic substrates. In multilayer substrates, the dielectric material has a very large effect on the overall thermal resistance and is discussed below in detail.

Table 10.9 lists the thermal conductivities of various thick film substrate dielectric materials. Metal substrates include steel, copper, and aluminum with subsequent dielectric layers. Whereas the physical parameters that set the thermal resistance for a substrate are primarily the thermal conductivity of the base material and the dielectric material, the conductor material has a very important effect on the thermal resistance. The conductors, composed of various metals, when used as a plane or planes, serve to spread the heat and thus lower the thermal resistance. Therefore, in the subsequent discussion on substrate materials, the methods of metallizing will be presented with a focus on thermal conductivity.

Inorganic substrates, used for low-cost applications, are discussed in Sec. 10.5.7, Printed Wiring Boards.

10.5.3.1 Alumina. The most commonly used ceramic material in electronic packaging is alumina, Al_2O_3, or aluminum oxide. It is used both as a body of a hermetic package and as a substrate. The CTE of the 96 percent alumina, 6.3 ppm/°C (25 to 400°C),[13] closely matches that of silicon and several metal packaging alloys (Kovar and Alloy 42). This close match prevents differential stresses that can lead to mechanical failure.

TABLE 10.7 Thermal Properties of Organic Adhesives[27,29,30,45,86]

Manufacturer	Material	Material type	Thermal conductivity @25°C (W/m-K)	Comments
Ablestik	84-1LMISR4	Thermoset-conductive	2.5	
Ablestik	84-1LMIT	Thermoset-conductive	5.9	
Ablestik	ECF561	Thermoset- conductive	1.6	
Emerson & Cuming	5025E	Thermoset-conductive	3.5	
Emerson & Cuming	ECF561	Thermoset-conductive	1.6	
AI Technology	TC8750	Thermoset-conductive	6.5	
Epoxy Technology	T6116	Thermoset-conductive	1.5	
Epoxy Technology	H20E	Thermoset-conductive	2.0	
DIEMAT	6030HK	Thermoset-conductive	60	
Hysol	KO120	Thermoset-conductive	2.8	
Ablestik	84-3J	Thermoset-nonconductive	0.8	
Emerson & Cuming	561K	Thermoset-nonconductive	0.9	
Emerson & Cuming	506	Thermoset-nonconductive	0.9	
Emerson & Cuming	5020K	Thermoset-nonconductive	0.7	
AI Technology	TK78759	Thermoset-nonconductive	11.6	Diamond filled
AI Technology	TP8260	Thermoplastic-conductive	6.5	
AI Technology	TP7155	Thermoplastic-conductive	1.6	
DIEMAT	4030LD	Thermoplastic-conductive	15	
Ablestik	2600K	Thermoplastic/thermoset blend	20.0	
AI Technology	TP7095	Thermoplastic-nonconducting	1.6	
AI Technology	TP7755	Thermoplastic-nonconducting	1.8	
AI Technology	TP7459	Thermoplastic-nonconducting	11.5	Diamond filled
Ablestik	71-1	Polyimide	2.1	
Ablestik	JM2000LB	Cyanate Ester	1.8	@ 121°C
Ablestik	JM2500	Cyanate Ester	1.1	@ 121°C

The thermal conductivity of alumina ranges from 12 to 35 W/m-K, depending on the purity. The highest purity available, 99.6 percent alumina, is typically used for thin film applications and has a thermal conductivity of 34.7 W/m-K at 25°C. Ninety-six percent alumina, typically used with thick-film metallization, has a thermal conductivity of 21 W/m-K at 25°C. Figure 10.11 shows the measured thermal conductivity for various percentages of alumina. In addition to thermal conductivity varying with the percentage of alumina, it also varies with temperature variation as shown in Fig. 10.12.[13,39]

TABLE 10.8 Thermal Properties of Inorganic Substrates[13,34]

Material name	Thermal conductivity @25°C (W/m-K)	CTE (ppm/°C)
Alumina 92%	17	7.2
Alumina 96%	21	6.3
Alumina 99.9%	30	7.4 (25–400°C)
Beryllium oxide 99.5%	248	6.4
Aluminum nitride	170	4.2
LTCC	2.0–4.4	4.5–8.0
CVD diamond	1300–2000	2.0

TABLE 10.9 Thermal Properties of Thick Film Dielectrics[35–37]

Material name	Application	Thermal conductivity @25°C (W/m-K)
DuPont dielectrics	Thick film glass	3.0
41010-25C	Tape on substrate	2.5–3.0
GPA98-047	Steel substrates	4.3

Alumina can be metallized with refractory metallizations (e.g., tungsten or moly-manganese), thin films, thick films, direct copper plating, and direct bond copper. The use of ground or power planes in either substrate or package metallization can aid in spreading the heat.

Multilayer thick films usually use screen-printed glass as the dielectric layers as depicted in the cross section shown in Fig. 10.13. This glass is both an electrical and a thermal insulator. The typical thermal conductivity of thick-film glass is identical to that of LTCC, which is 3.0 W/m-K.[40] To improve the effective thermal conductivity of multilayer thick-films, the physical designer makes use of thermal vias. As shown in Fig. 10.14, thermal vias are a series of filled vias stacked upon each other in an array. The bottom of the stack is attached either to the ceramic substrate or to a plane. Thick-film conductor inks, whether they are gold, silver, or an alloy, are not pure metals. The inks consist of a functional material of metal, a solvent, a temporary binder, and a permanent binder. This permanent binder is used to tailor the CTE to that of the substrate and to aid in the adhesion to either the dielectric or the ceramic substrate. During firing, the solvent and temporary binders are burned out, leaving a conductor whose properties are no longer that of the pure metal functional material. In addition to altering the CTE, the permanent binder reduces both the electrical and thermal conductivity of the conductor. Typical fired thick-film conductors are 8 μm thick. If this conductor were pure gold, it

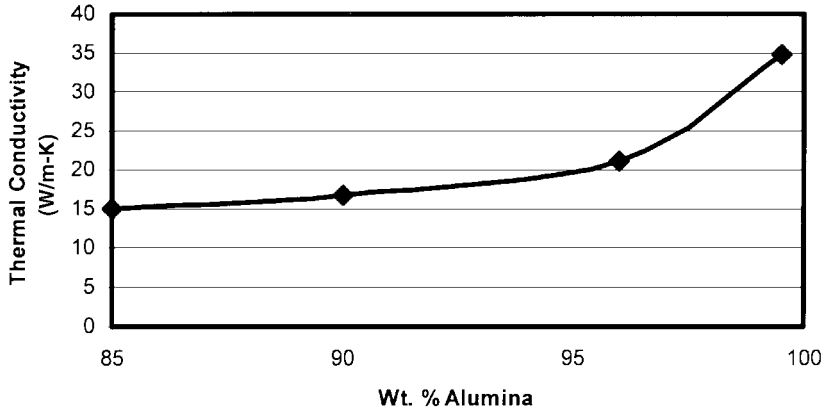

Figure 10.11 Effect of weight percent of Al_2O_3 on thermal conductivity.

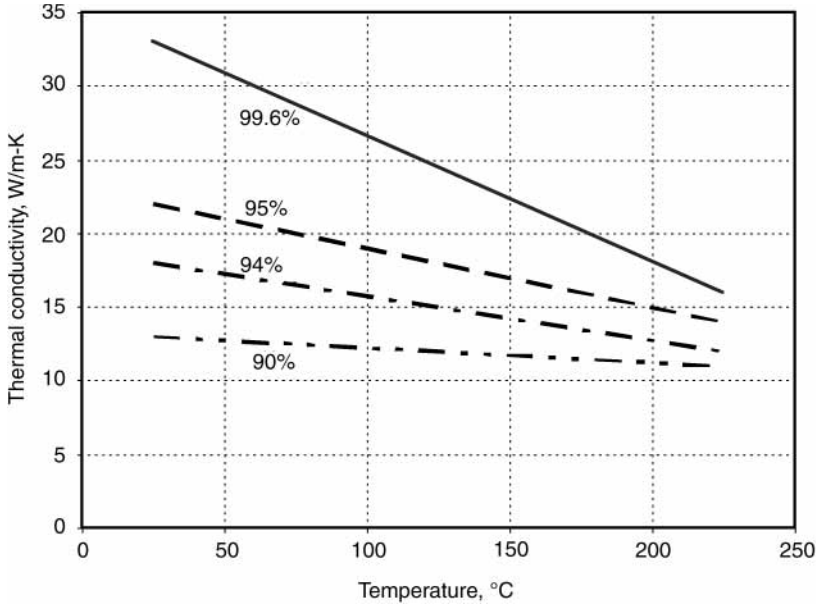

Figure 10.12 Variation of thermal conductivity of alumina at temperature.

would have a sheet resistivity of 3 mΩ/❑. The 5715 thick-film gold conductor material from DuPont Electronics specifies a sheet resistivity of less than 5 mΩ/❑ for the same fired thickness.[35] The composition of via fill inks is slightly different from that of conductors. This allows the via fill to closely match the CTE of the dielectrics and, in the process, changes both the thermal and electrical conductivities. The sheet resistivity of DuPont Electronics' 5727 gold via fill material is 15 mΩ/❑. This is five times that of pure gold. There is also a drastic difference in the thermal conductivity of thick-film gold in comparison with pure gold. Thick-film gold via fill has a measured thermal con-

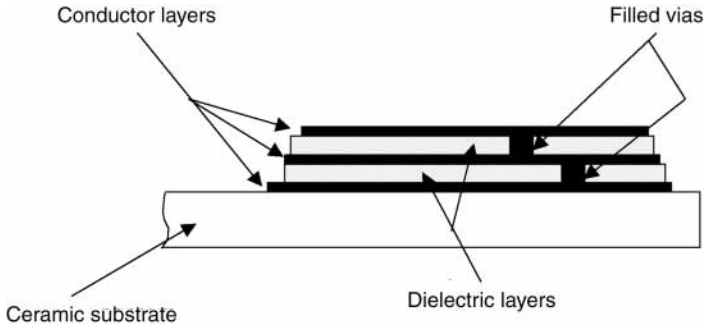

Figure 10.13 Multilayer thick film dielectric cross section.

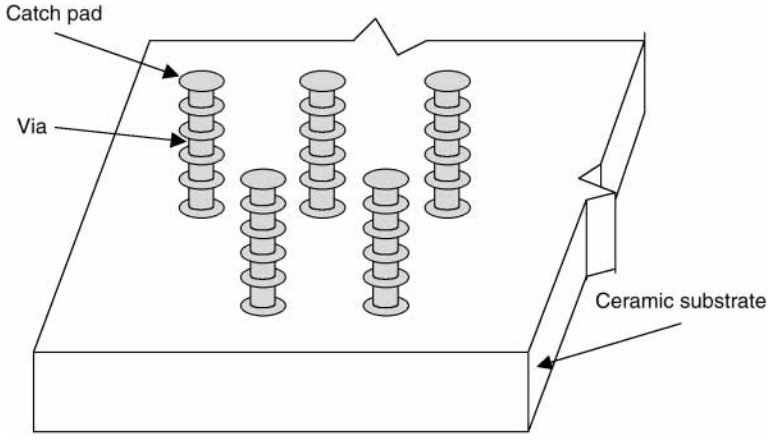

Figure 10.14 Portion of a thermal via array in multilayer thick film dielectric.

ductivity of 20.1 W/m-K (see Ref. 41), whereas pure gold has a thermal conductivity of 297 W/m-K.[24]

There are two key parameters in the design of thermal vias in thick films. The diameter of the via is determined by the filling process. If the diameter is too large, it will be difficult to fill with just one or two screen printings. The design of the spacing or pitch of the vias is a trade-off. Obtaining the maximum thermal conduction requires a high pitch or high density of vias. But a high pitch has two problems. First, it restricts routing of the signals. Even though via fill materials are designed to match the CTE of the dielectric, placing too many per unit area increases the effective CTE and puts the dielectric material into stress, which can result in cracking.[8]

Direct bond copper (DBC) is a patented[42] process, originally developed at General Electric, in which copper is eutectically attached to oxygen-bearing ceramics such as alumina and beryllium oxide. As shown in the copper-oxygen phase diagram in Fig. 10.15, copper and oxygen have a eutectic point at 1065°C. At this point on the phase diagram, there is 0.39 percent oxygen. When copper is placed on the ceramic between 1065 and 1083°C (the melting

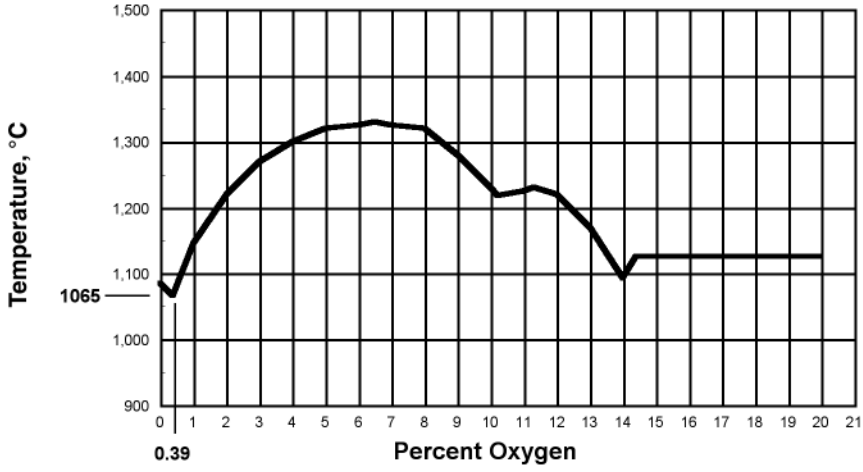

Figure 10.15 Copper-oxygen phase diagram.

point of copper), the copper fuses with the ceramic. A cross section of direct bond copper is shown in Fig. 10.16. There is a thin layer of Cu-O between the copper and the ceramic. In microelectronics applications, the thickness of the copper foil can range from 0.001 to 0.020 in. Because copper has a CTE of 16.12 ppm/°C,[43] which is many parts per million higher than that of the ceramic, it can place the ceramic in tension and either warp it or cause it to crack. To prevent this, manufacturers of direct bond copper typically place equal amounts of copper on both sides of the ceramic. A curve for the equivalent CTE versus copper thickness for an alumina substrate with equal amounts of copper on each side is shown in Fig. 10.17.[44] Most DBC manufacturers recommend limiting the thickness of the copper on each side of the substrate as a percentage of the ceramic thickness to prevent warping and cracking of the ceramic.[45]

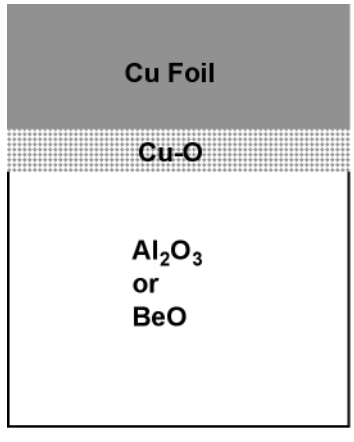

Figure 10.16 Cross section of direct bond copper on alumina and beryllia.

Most applications of direct bond copper require it for its high electrical conductivity. Typical values of sheet resistivity are significantly less than 1 mΩ/❑. An added benefit of DBC is its high thermal conductivity as a result of the excellent spreading capability of the copper. Nguyen has developed an equation for the equivalent thermal conductivity of direct bond copper substrates.[47]

$$K_e = \frac{\sum_{i=1}^{n} K_i t_i}{\sum_{i=1}^{n} t_i} \tag{10.26}$$

where K_e = equivalent thermal conductivity
K_i = thermal conductivity of each material
T_i = thickness of each material
n = number of materials

Example Find the equivalent thermal conductivity of a direct bond copper substrate consisting of 0.010-in thick copper on each side of a 0.025-in thick beryllium oxide substrate.

- K_{Cu} = 401 W/m-K
- K_{BeO} = 248 W/m-K
- t_{Cu} = 0.010 in
- t_{BeO} = 0.025 in

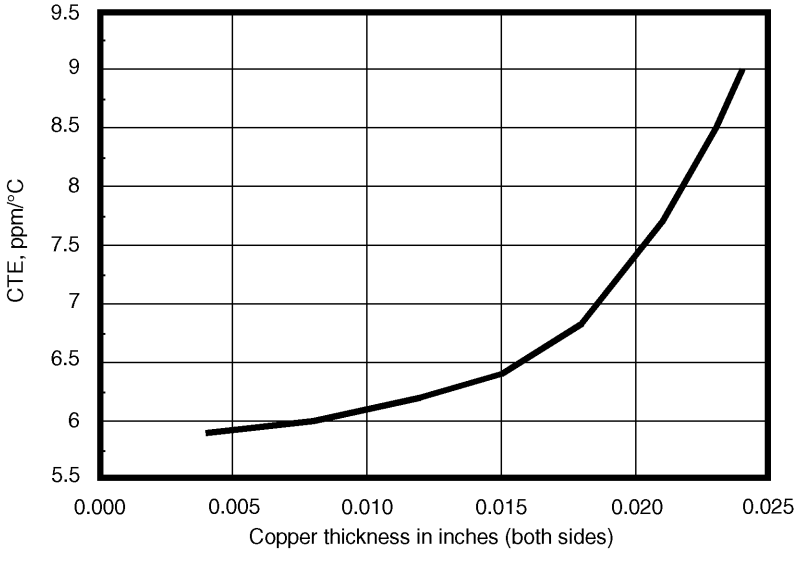

Figure 10.17 Equivalent TCE vs. copper thickness for a 0.025-in alumina substrate with equal amounts of copper on each side.

The thicknesses of the copper and beryllium oxide are first converted to metric units.

- $t_{Cu} = 0.010 \text{ in} \times 0.0254 \text{ m/in} = 2.54 \times 10^{-4} \text{ m}$
- $t_{BeO} = 0.025 \text{ in} \times 0.0254 \text{ m/in} = 6.35 \times 10^{-4} \text{ m}$

Using Eq. (10.26), the equivalent thermal conductivity K_e is calculated.

$$K_e = \frac{2.54 \times 401 \times 6.35 \times 10^{-4} \times 248 + 2.54 \times 10^{-4} \times 401}{(2.54 + 6.35 + 2.54) \times 10^{-4}} = 8.03 \text{ W/m-K} \quad (10.27)$$

An alternative material used for dielectrics in thick film multilayer circuits is *tape transfer dielectric*. The tape dielectric process is a patented process[48] in which layers of glass-ceramic tape are applied to a fired, dimensionally stable substrate in lieu of screen printing the dielectric. This process has several trade names—TTRAN, Tape-on-Substrate, and DITRAN. The purpose of using tape dielectric in lieu of screen-printed dielectric is to provide an extremely flat surface for screen printing fine lines (as narrow as 0.002 in). The thermal conductivity of the 41010-25C tape dielectric material from Electro Scientific Laboratories is 2.5 to 3.0 W/m-K.[49]

10.5.3.2 Beryllium oxide. Beryllium oxide, BeO, or *beryllia,* is often used when a high-thermal-conductivity substrate is required. At 25°C, beryllia has a thermal conductivity of 248 W/m-K,[13] a value ten times that of alumina. The thermal conductivity of BeO decreases with increasing temperature as shown in Fig. 10.18.[19]

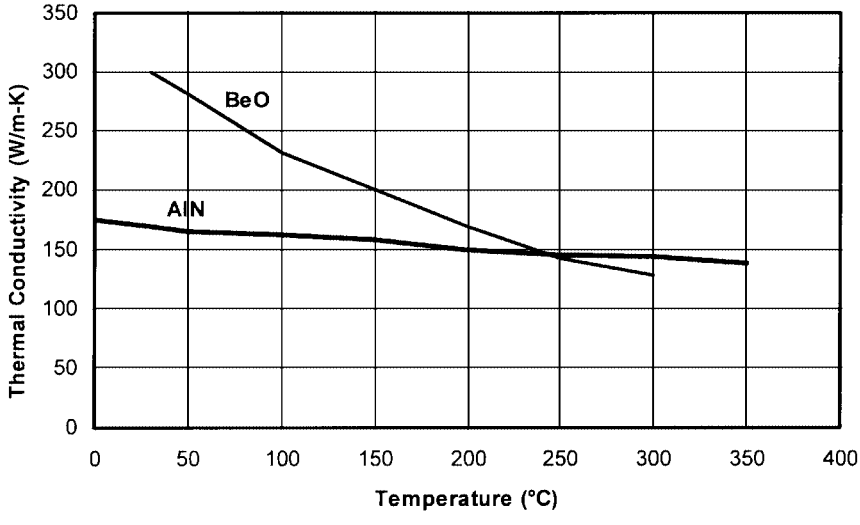

Figure 10.18 Thermal conductivity variation of AlN (170 W/m-K) and BeO.

All beryllium compounds, including beryllium oxide, are toxic in powder form. However, in their solid form, they do not pose any health hazards. Therefore, operations such as grinding, cutting, laser trimming, and certain furnace operations need to be performed so that airborne beryllium oxide particles are not generated.

The dust of beryllium compounds causes *chronic beryllium disease* (CBD). It is also known as *berylliosis*, a disease whose symptoms include scarring and damage of lung tissue, shortness of breath, wheezing, and/or coughing.[50] The incidence of CBD requires three factors:

1. The individual must be allergic to beryllium. It is estimated that approximately 1 percent of the population is allergic to beryllium. Because those who are susceptible cannot be identified, 100 percent of the population must be protected.
2. The individual must be exposed to beryllium of a respirable size—less than 10 μm. The only significant hazard associated with beryllium is inhalation. Airborne particles in excess of 10 μm in size cannot penetrate the upper respiratory tract and enter the alveolar area of the lung.
3. The individual must be exposed to a sufficiently large concentration of airborne beryllium. There is no exact dividing line between safe and unsafe amounts. The recommended levels, which include guard bands, are 2 $\mu g/m^3$ average or 25 μg peak.[51]

Because of the toxicity of beryllium oxide, several countries and some individual companies have banned its use.[52] Where beryllia is used, it must be clearly identified on the component and its shipping container.

Beryllia is commonly metallized with refractory metallization such as tungsten and moly-manganese, nickel, and gold plating. Other metallization methods include thin and thick films as well as direct bond copper. When multilayer thick films are used with beryllium, the thermal resistance must be broken down into two main parts—the ceramic and the glass/metal combination of the multilayers.

The CTE of 99.5 percent beryllia at 20°C is 6.4 ppm/°C, which is very close to that of alumina.[13] The variation of linear expansion of beryllia over the temperature range is shown in Fig. 10.19. This is a key parameter in mounting devices to the BeO or mounting the BeO to the next assembly.[51]

10.5.3.3 Aluminum nitride. A high-thermal-conductivity alternative to beryllium oxide is aluminum nitride, AlN. Having a nominal thermal conductivity of 170 W/m-K at 25°C,[13,55] it is approximately seven times more thermally conductive than alumina. Aluminum nitride, with a room temperature CTE of 4.7 ppm/°C, is more closely matched to silicon (2.5 ppm/°C over the 20 to 100°C range)[13] than beryllium oxide or alumina. For many high-power applications, aluminum nitride is the substrate material of choice, as it is nontoxic. The thermal conductivity of aluminum nitride can have significant variation if the

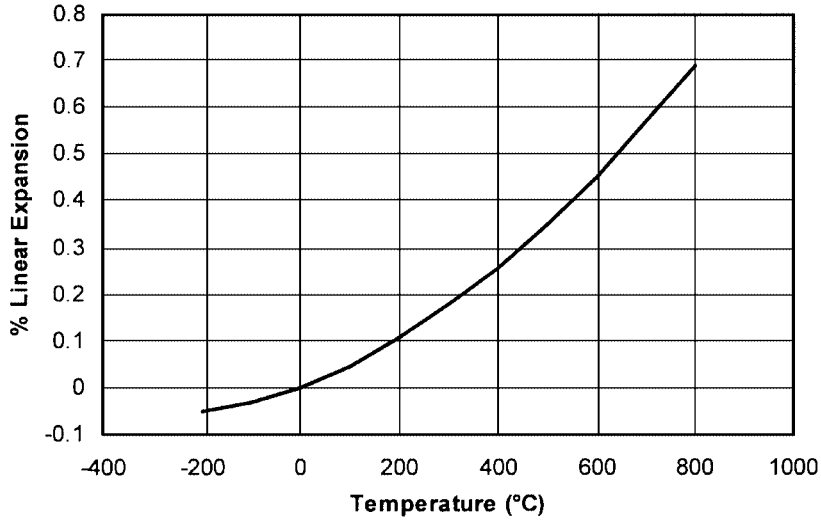

Figure 10.19 TCE variation of beryllium oxide vs. temperature.

oxygen content varies. As shown in Fig. 10.20, a 0.2 percent change in oxygen content can have a 12.5 percent variation in thermal conductivity.

Both beryllium oxide and aluminum nitride have thermal conductivity degradation as the temperature increases. As shown in Fig. 10.18, the thermal conductivity of aluminum nitride becomes greater than that of beryllium oxide at temperatures greater than 240°C. Therefore, for operation at temperatures in excess of 240°C, aluminum nitride is the ceramic material of choice when high thermal conductivity is the selection criteria.[19]

Aluminum nitride can be metallized a number of ways. Single-layer thin film is a reliable metallization. Starting with a sputtered or evaporated adhe-

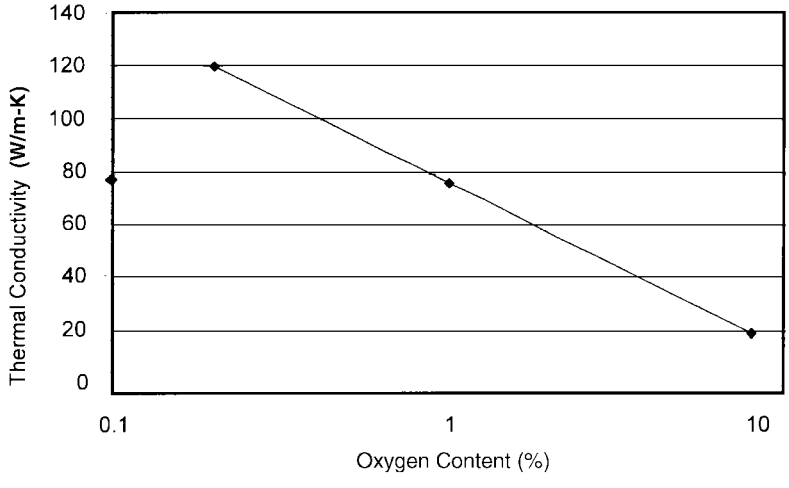

Figure 10.20 Copper-oxygen phase diagram.

sion layer, it can be plated with nickel and gold. Refractory metallization can also be used.

Aluminum nitride can be metallized using the classic thick film printing process using specially formulated inks. The oxide glasses in inks formulated for alumina are not chemically compatible with aluminum nitride. The CTE of glasses for dielectrics need to match those of the substrate. Because standard thick film inks are formulated for 96 percent alumina with a CTE of 6.3 ppm/°C, they do not match the CTE of AlN at 4.2 ppm/°C.[13] In addition, the reactive bonding compounds in standard thick film inks in alumina are not effective in promoting adhesion to aluminum nitride substrates.[56] Several thick film ink manufacturers have developed inks that are compatible with aluminum nitride.[57,58]

Aluminum nitride can also be metallized using active metal brazing, a process that relies on an "active" (i.e., chemically reactive) constituent, usually titanium, to produce a wettable compound at the brazing interface.[59]

Aluminum nitride can be metallized with direct bond copper. However, the process used for oxide-bearing ceramics (alumina and beryllium oxide) must be modified to first grow an oxide of Al-O on the aluminum nitride. This oxygen layer thickness is on the order of angstroms. The copper oxide then fuses with this Al-O oxide. A cross section of direct bond copper on aluminum nitride is shown in Fig. 10.21. The effect of adding copper to both sides of aluminum nitride can be modeled in the same manner as described in Eq. (10.26).

One shortcoming of aluminum nitride is its decomposition to amorphous aluminum hydroxide when in contact with water at elevated temperatures. Aluminum nitride also reacts with cleaning solutions containing ammonia. The ammonia will etch the substrate and produce a porous surface finish that will lead to poor adhesion between metallization and the substrate.[60]

10.5.3.4 Low-temperature cofired ceramic. Low-temperature cofired ceramic (LTCC) is a thick film process technology commercialized by DuPont in 1985 and used for multilayer substrates and integral substrate-packages. The

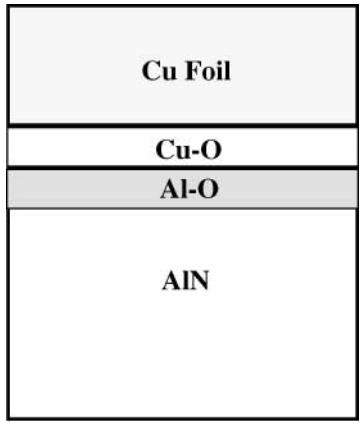

Figure 10.21 Cross section of direct bond copper on aluminum nitride.

LTCC process starts off with "green" (unfired) ceramic tape that is a combination of glass and ceramic. It has a high glass content, allowing it to be fired at temperatures in the range of 850 to 950°C. This low firing temperature allows the LTCC to be metallized with low-resistivity gold, silver, and copper conductors. Vias, cavities, and registration holes are produced in the tape by mechanical drilling, punching, or laser ablation. Next, the individual layers are metallized using the classic screen-printing process. Vias are then filled. The individual layers are then collated, aligned, laminated, and fired in an air-fired furnace. During firing, the LTCC shrinks nominally 12.27 percent. The completed substrate is cut to size using either a mechanical or laser process.[8,35]

The thermal conductivity of LTCC ranges from 2.0 to 4.4 W/m-K, depending on the manufacturer and the particular formulation of the tape. See Table 10.10 for details. For all formulations of LTCC, the thermal conductivities are extremely low as a result of the high glass content (approximately 50 percent). To minimize the effect of the low thermal conductivity, physical designers can use cavities under high-power-density components, arrays of thermal vias, or a combination of both.[36,40,61–63]

TABLE 10.10 Thermal Properties of LTCC[36,40,61–63]

Material	Manufacturer	Thermal conductivity, (W/m-K)	CTE (25–300°C), (ppm/°C)
951	DuPont	3.0	5.8
943	DuPont	4.4	4.5
41110-70C	ESL	2.5–3.0	6.4
41020-70C	ESL	2.5–3.0	7.4
A6M	Ferro	2.0	7.0
A6S	Ferro	2.0	8.0

The number of layers of tape constituting an LTCC substrate can range from as few as 5 to as many as 50. To minimize the thermal resistance, the designer can place the high-dissipating component in a cavity as shown in Fig. 10.22. In this figure, the bottom of the die is electrically isolated from the back of the substrate with two layers of tape. The actual number of layers of tape under the cavity is a function of the area of the cavity and the strength of the

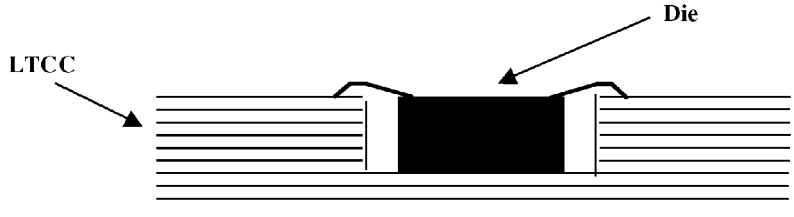

Figure 10.22 Isolated die in cavity under LTCC.

LTCC. For small devices (i.e., less than 0.1 in sq.), there can be only one or two layers of tape. For large devices, such as complex ASICS, there must be at least five layers of tape. When the back side of the die does not need to be electrically isolated and can sit on the package base or heat sink, the cavity can go through the entire LTCC substrate as shown in Fig. 10.23.

The use of thermal vias in LTCC is a standard method of improving the effective thermal conductivity. There can be an array of stacked vias going to the bottom of the substrate, as shown in Fig. 10.24, or to one layer above, as shown in Fig. 10.25. In the former case, the back side of the die does not need to be isolated from the bottom of the substrate. In the latter case, the bottom layer of the substrate provides the electrical insulation. Thermal vias can be used in conjunction with the die cavities discussed above. A cross section of a substrate with a die cavity and thermal vias is shown in Fig. 10.26.

The density of the thermal vias and their diameter are typically set by the individual manufacturer of LTCC substrates with recommendations from the tape manufacturer. The via diameter is a function of the method used to fill the vias and the differential shrinkage of the via fill material and the LTCC material. An industry standard for via diameter is 0.006 in.[8] The density, or pitch, of the thermal vias is a function of the CTE of the via fill with respect to the CTE of the LTCC tape. The relative dimensions of a typical thermal via array are shown in Fig. 10.27.[40,61] For the industry standard 0.006-in diameter via, the spacing of the vias should be 0.018 in.

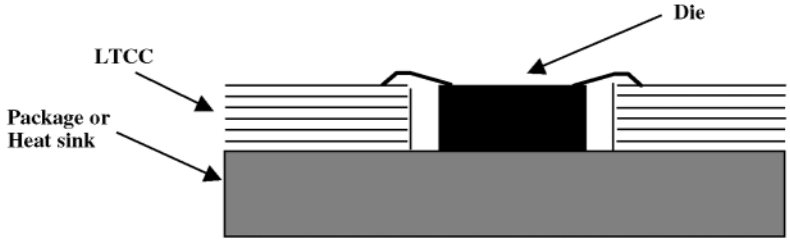

Figure 10.23 Cavity in LTCC with die directly attached to package or heat sink.

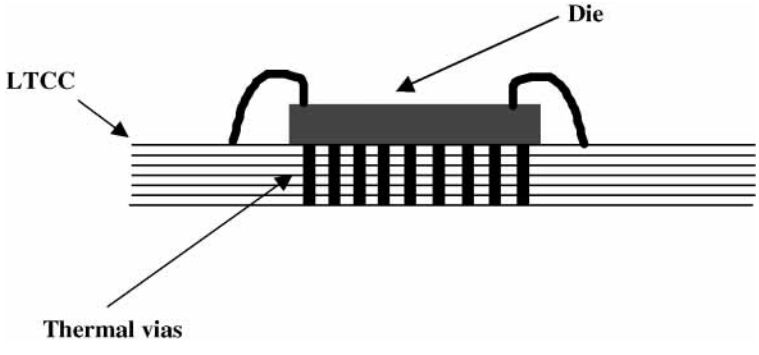

Figure 10.24 Thermal vias in LTCC.

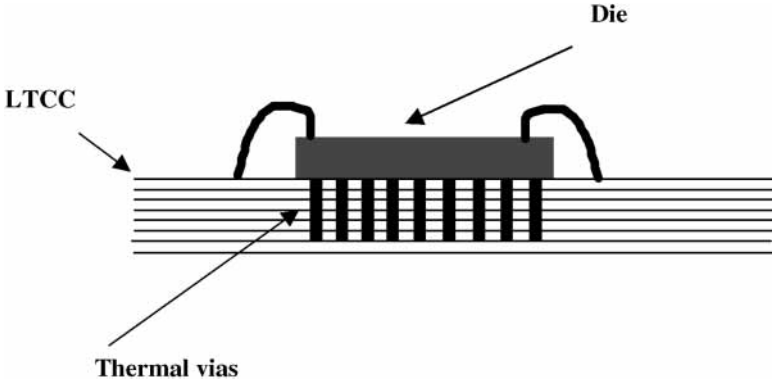

Figure 10.25 Thermal vias in LTCC with electrically isolated die.

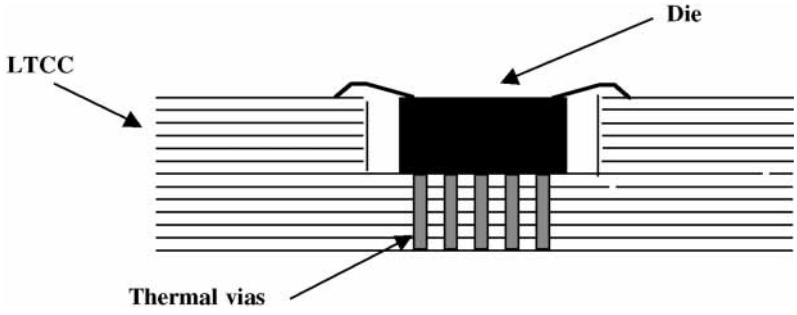

Figure 10.26 Cavity in LTCC with thermal vias.

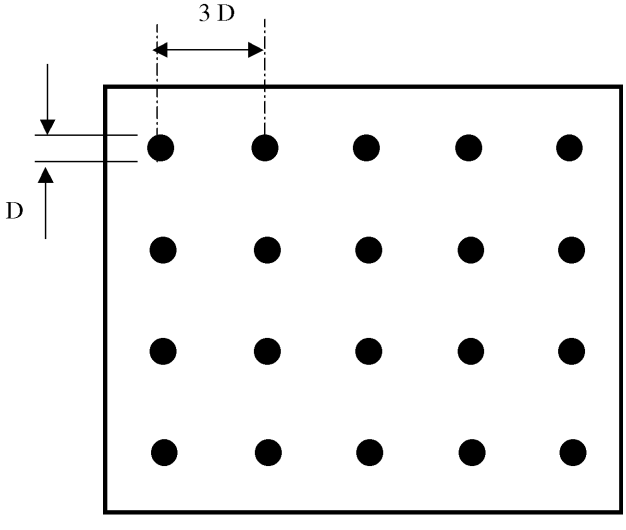

Figure 10.27 Via dimensions in LTCC.

The LTCC manufacturer has a choice of gold, silver, or palladium silver inks for use as via fill materials. The silver inks are both electrically and thermally more conductive than the gold inks. DuPont[35] publishes electrical resistivity data for its via fill inks but does not give any thermal conductivity data. Licari[8] has data on average thermal resistance for very large (0.020-in dia.) gold and silver thermal vias that shows silver being 8 to 15 percent lower. Actual measured data are very limited. The measurements by Harshbarger[64] were used to calculate the thermal conductivity of 5718 gold via fill at 24.4 W/m-K.[41]

10.5.3.5 Thin film multilayer substrates. Thin film multilayer substrates are used to fabricate MCM-Ds (MCM-deposited). Many materials (alumina, silicon, aluminum nitride, and aluminum) are used as the supporting substrate and have been previously described. The difference is in the metallization and the insulating dielectric material. A cross-sectional view of a typical MCM-D substrate is shown in Fig. 10.28. Most MCM-D manufacturers use polyimide or other polymers as the dielectric in their thin film multilayer substrates. Internal metallization traces can be copper, gold, or aluminum. External (or top) metallization can be either aluminum or gold.[8]

The total thermal resistance of the thin film multilayer substrate consists of two resistances in series—the multilayer portion and the supporting material. The thermal conductivity of the thin film multilayer portion of the substrate is primarily determined by the low thermal conductivity of the polyimide. Typical values for the polyimide are in the range of 0.2 to 0.3 W/m-K (see Table 10.11).[8,66]

TABLE 10.11 Thermal Properties of Thin Film Dielectrics

Material	Thermal conductivity (W/m-K)
Polyimide	0.2–0.3
Silicon dioxide	0.5–2.0

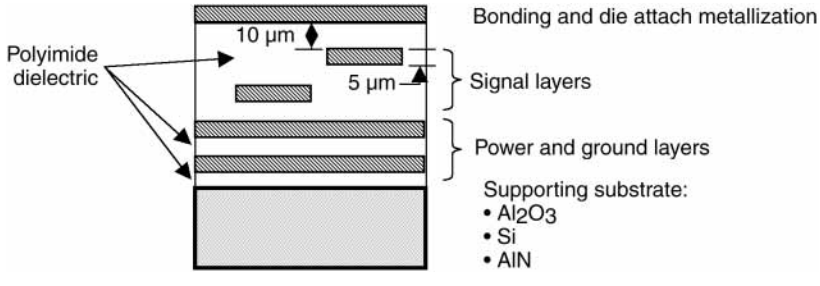

Figure 10.28 MCM-D substrate cross section with polyimide dielectric.

Some MCM-D manufacturers use silicon dioxide as the dielectric layer. A cross-sectional view of an MCM-D substrate with silicon dioxide dielectric is shown in Fig. 10.29. Silicon dioxide's thermal conductivity of 0.5 to 2.0 W/m-K is extremely low.[3]

To improve the effective thermal conductivity in thin film multilayer substrates, the physical designer can use arrays of thermal vias. The materials used for these vias are the same as the internal metallization of the substrates—gold, copper, or aluminum. The thermal conductivity of these metallizations is listed in Table 10.12. Deposited as a thin film using evaporation or

TABLE 10.12 Thermal Conductivity of Thin Film Metallizations[65]

Material	Thermal conductivity (W/m-K)
Gold	319
Aluminum	237
Copper	401
Nickel	94

sputtering, these thermal vias are composed of pure metals and have the same thermal conductivity as the pure metals. The dimensions of a thermal via array with a polyimide dielectric are shown in Fig. 10.30. When thermal vias are used, and their area equals 50 percent of the die area, the effective thermal conductivity of a polyimide based dielectric improves to 1.2 W/m-K. For a thermal via pattern that is 75 percent of the die area, the effective thermal conductivity is 2.4 W/m-K.

10.5.3.6 Steel substrates. Ceramic substrates, as described above, are difficult to attach to heat sinks with screws because of their low tensile strength. Polymeric attachment adds thermal resistance to the thermal path. Steel substrates do not have these shortcomings because of the strength of the steel.

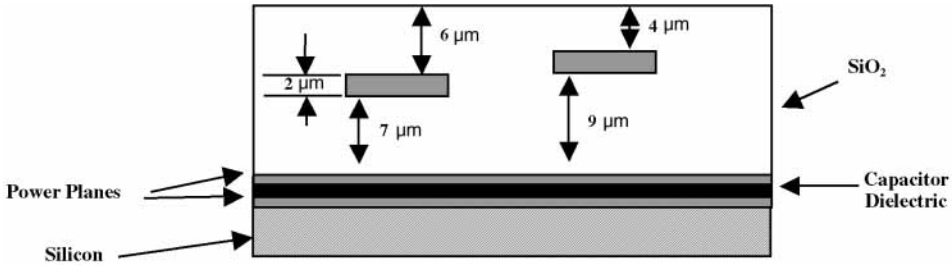

Figure 10.29 MCM-D substrate cross section with silicon dioxide dielectric.

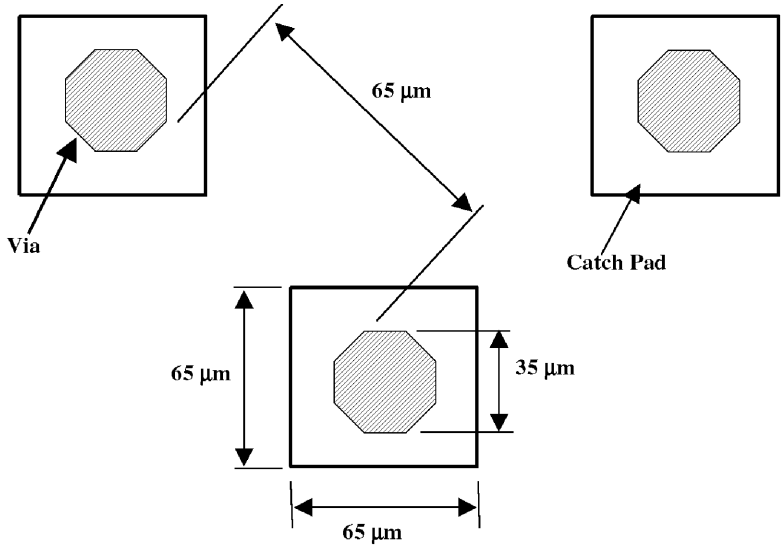

Figure 10.30 Dimensions for thermal vias in MCM-D substrates.

However, steel is an electrical conductor and needs to be insulated before being used as a substrate. The Cermalloy Division of Heraeus Incorporated has developed a system of thick film inks for use with Type 430 stainless steel substrates.[37] This system of inks is known as Dielectric on Steel (DOS). The process starts out with the printing of dielectric material on the steel with subsequent drying and firing. Multiple layers of dielectric are typically used to prevent pinholes that can lead to shorts between layers. The recommended fired thickness of dielectric is 0.003 ± 0.0002 in. Conductors are added using the classic thick film processes. Additional dielectrics and conductors are added as required.

The thermal conductivity of the Cermalloy GPA98-047 is 4.3 W/m-K, whereas the thermal conductivity of Type 430 stainless steel is 26.1 W/m-K. The value of the dielectric thermal conductivity can be considered low.[13,37,68,69]

10.5.3.7 CVD diamond. Synthetic diamond or chemically vapor deposited (CVD) diamond is a very high (>1300 W/m-K) thermal conductivity material that can be used both as a substrate and as a heat spreader. An electrical insulator ($\rho > 10^8$ Ω-cm), CVD diamond has a temperature coefficient of expansion of 2.0 ppm/°C for temperatures in the range of 25 to 200°C. This can possibly cause stresses between semiconductor materials and the diamond spreader or substrate. The CVD diamond can be grown "free standing"—as a substrate or as a film deposited on another material. Figure 10.31 shows an alumina substrate with a layer of CVD diamond. Diamond substrates can be metallized with thin films such as titanium-platinum-gold (TiPtAu), titanium-palladium-gold (Ti/Pd/Au), nichrome-nickel-gold (NiCr/Ni/Au), titanium-tungsten-gold

Figure 10.31 CVD diamond layer on alumina substrate.

(Ti-W/Au), or chrome-gold (CrAu). Thick film metallization of diamond has not been developed.

With its extremely high thermal conductivity, CVD diamond can serve as an excellent heat spreader. One of the earliest applications of the material was as a heat spreader under high-power-density gallium arsenide devices.

Compared to ceramics such as alumina, beryllia, and aluminum nitride, CVD diamond is considered expensive. To minimize costs when using CVD diamond, the size needs to be minimized. Moravec et al. have found that the optimal thickness (t_{opt}) of a diamond heat spreader should be 0.5 to 1.0 times the radius of the heat source as shown in Fig. 10.32. The optimal radius (R_{opt}) of the heat spreader should be three times that of the heat source. This analysis can be approximated for rectangular heat sources by substituting half the device's length in Eq. (10.29) for the radius as described above.[70]

$$t_{opt} = 0.5 \text{ to } 1.0 \times \text{radius of heat source} \tag{10.28}$$

$$R_{opt} = \frac{a_2}{a_1} \tag{10.29}$$

The thermal properties of CVD diamond are tabulated in Table 10.8.[34,71]

10.5.3.8 Insulated metal substrates. Insulated metal substrates (IMS) are used as both substrates and circuit cards. As shown in Fig. 10.33, they are com-

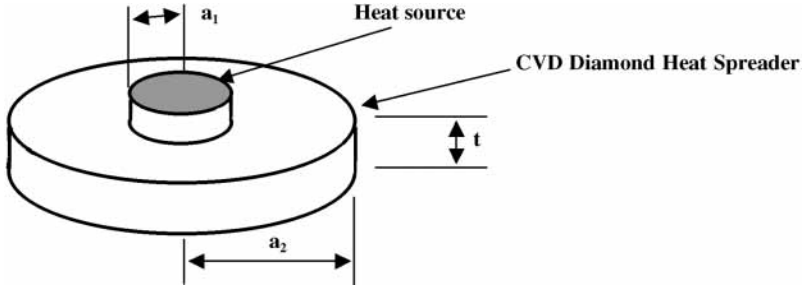

Figure 10.32 Optimal size of CVD diamond heat spreader.

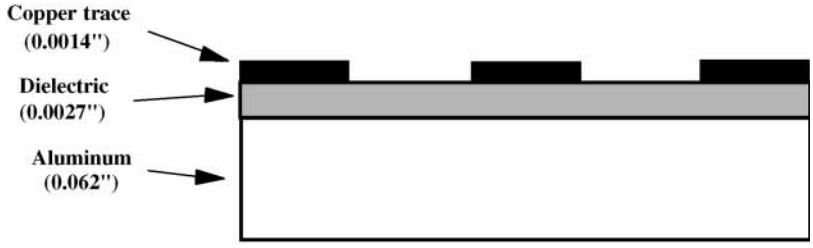

Figure 10.33 Single-layer insulated metal substrate cross section.

posed of a single-sided metal-clad board material with several layers of metallization. Fabricated in arrays on panels as large as 18 x 24 in, insulated metal substrates offer a low-cost, high-thermal-conductivity alternative to FR-4 printed circuit cards. The backing plate, typically aluminum, can also be copper, copper-Invar-copper, copper-molybdenum-copper, or steel and serves as a heat sink. The dielectric material is a polymer material whose thickness is a trade-off between voltage breakdown and thermal resistance. To have the highest voltage breakdown requires the thickest layer of dielectric. However, the dielectric is a poor thermal conductor, and its thickness needs to be minimized so that the thermal resistance can be minimized. The thermal conductivity of the dielectric material for Berquist's IMS is 1.3 W/m-K.[72] To improve the thermal conductivity of the polymer dielectric layer, the IMS manufacturer typically loads the material with alumina or boron nitride. The voltage breakdown of this standard Berquist material is 6 kV.

Improved dielectric materials for insulated metal substrates are available with a higher thermal conductivity of 2.0 W/m-K.[72] These materials also have a higher dielectric breakdown voltage of 9 kV.

On IMS substrates, the conductor traces are copper with thicknesses that range from 1-oz copper (0.0014 in) to 4-oz copper (0.0056 in). The effect of thick copper metallization not only aids in minimizing voltage drop, it helps spread the heat.

The equivalent CTE of IMS substrates is very close to that of the backing plate. For example, for the Berquist IMS material with an aluminum base, the CTE is 20 ppm/°C.

Insulated metal substrates can be made with two conductor layers as shown in Fig. 10.34. The thermal conductivity of the dielectric remains the same as

Figure 10.34 Two-layer insulated metal substrate cross section.

in the single layer, 1.3 W/m-K. However, in the multilayer IMS, thermal vias can be incorporated to reduce the thermal resistance. Table 10.13 summarizes the thermal properties of insulated metal substrates.

TABLE 10.13 Thermal Properties of Insulated Metal Substrates[13,72]

Base material	Dielectric	Thermal conductivity @25°C (W/m-K)	CTE (ppm/°C)
Copper C11000 alloy		388	17.0
Aluminum 6061		180	23.6
Cold-rolled steel		65.2	12.6
Copper-Invar-copper (1:3:1)		174 x & y 24.8 z	6.5
Copper-moly-copper (1:6:1)		233	6.4
	Thermal Clad®*	1.3	†
	Thermal Clad HTV®*	2.0	†

*Thermal Clad and Thermal Clad HTV are registered trademarks of the Berquist Company.
†CTE of dielectric on base material is approximately equal to that of the base material.

Insulated metal substrates are used with both bare die and packaged devices. When used with bare die, the thermal path from the die to the heat sink is minimal as shown in Fig. 10.35. The heat goes from the die, through the die attach, through the IMS dielectric, and into the metal base plate, where it spreads.

10.5.3.9 Printed wiring board substrates. In MCM-L (laminated) applications, the multilayer substrate is fabricated from organic materials such as FR-4 and polyimide. Another name for the MCM-L is chip-on-board (COB), which is discussed in Sec. 10.5.5.1.

A complete discussion of printed wiring boards can be found in Sec. 10.5.7. The key differentiator in printed wiring boards used for MCM-L applications

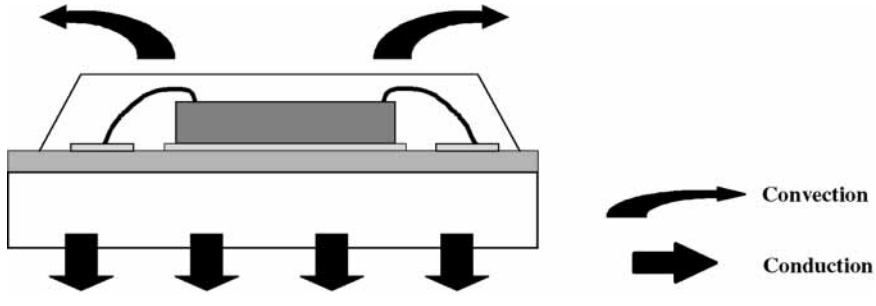

Figure 10.35 Thermal path for bare die on IMS.

is the requirement for wire bonding. Special attention needs to be given to the plating and cleaning of the boards to allow for high yields in wire bonding. The thermal conductivities of various printed circuit card dielectrics are listed in Table 10.14.

TABLE 10.14 Thermal Conductivity of Printed Circuit Card Dielectrics.[3,19,38,73–76*]

Material	Thermal conductivity @25°C (W/m-K)	CTE (below T_g) (ppm/°C)	Comments
FR-4	0.8 x & y 0.3 z	16–20 x & y 50–70 z	
G-10	0.294	14	
Bismaleimide/triazine (BT)	0.17–0.21	13–15 x & y 40–50 z	
Polyimide	0.11	23–56	
S-2 glass	0.9	2.8	
Aramid (Kevlar)	0.20	7–8 x & y 115 z	
Quartz	1.1	1.0	
GML 2032	0.289	28–30 x & y 80 z	99°C
GML 1000	0.228	30–32 x & y	120°C
Rogers RO4003	0.64	11–14 x & y 46 z	100°C
Rogers RT/Duroid 6002	0.6	16 x & y 24 z	
Arlon	0.28–0.36	17–29 x & y 217 z	
Benzocyclobutene (BCB)	0.19	45–70	

*Unless otherwise noted, thermal conductivities are at 25°C.

10.5.4 Substrate attach

A substrate is usually utilized in multichip applications. Attaching the substrate to the next assembly (whether it is a package, a circuit card, or a heat sink) requires an attachment medium. Polymeric material is typically used. Unless grounding is required for the back side of the substrate, the polymeric material is typically electrically nonconducting. Some of the polymeric paste materials used for die attach are also used for substrate attach and are listed in Table 10.7. To maintain a uniform bond line and to speed the assembly operation, preforms of thermoset and thermoplastics are used for substrate at-

tach. The thermal conductivity of organic materials specifically designed for substrate attach are listed in Table 10.15. If the backside of the substrate has to be electrically connected to the next assembly, then the attachment material needs to be electrically conducting. For high-power-density applications, solder may be used for substrate attachment. Typically applied in either a paste or a preform, the solders used include Sn10, Sn62, Sn63, Sn96, and gold-tin. The thermal conductivities of these solders are listed in Table 10.5.

TABLE 10.15 Thermal Conductivity of Organic Adhesives for Substrate Attach[29,30,86]

Material	Manufacturer	Electrical characteristics	Thermal conductivity (W/m-K)
Ablefilm 550K	Ablestik Industries	Nonconductive	0.8
Ablefilm 506	Ablestik Industries	Nonconductive	0.9
Ablefilm 563K	Ablestik Industries	Nonconductive	1.1
ECF 5025E	Ablestik Industries	Conductive	3.5
TK7755	AI Technology	Nonconductive	1.8
TP7165	AI Technology	Nonconductive	1.8
TK7759	AI Technology	Nonconductive	11.6
TC8750	AI Technology	Conductive	6.5
T7109	Epoxy Technology	Nonconductive	3.0
H70-2	Epoxy Technology	Nonconductive	1.4
930	Epoxy Technology	Nonconductive	4.0
6081	Epoxy Technology	Nonconductive	2.5

10.5.5 Packages

Electronic packages provide three key functions.

- Mechanical support and environmental protection for the semiconductor
- Power and signal interconnections from the semiconductor(s) to the circuit card
- A means for dissipating the heat generated in the semiconductor(s)

These functions can be accomplished by both hermetic and nonhermetic packages. In the following sections, the construction of the packages will be analyzed with respect to the materials and thermal paths composing the package.

10.5.5.1 Nonhermetic packages. Almost all of the semiconductors used today are assembled into packages. For most applications, the microcircuits are assembled in molded plastic packages called plastic encapsulated microcircuits (PEMs). In this packaging technology, the microcircuit is typically attached with a polymeric material to a lead frame, wire bonded, and encapsulated in a plastic material as shown in Fig. 10.36. The exterior base of the package is also plastic.

The primary heat paths from a plastic encapsulated microcircuit, as shown in Fig. 10.37, are through the base of the package and through the leads to the circuit card assembly. A secondary heat path is from the die through the plastic to the air. To improve the thermal performance, some manufacturers have developed plastic packages using thermally enhanced mold compounds.

A variety of plastic encapsulated microcircuit package families are used for surface mount applications. They include SOIC, SOJ, PLCC, BQFP, TQFP, and TSOP. Two key differentiators for the package families are lead configuration and pitch. The heat paths for each package type are the same as the generic PEM as described above.

To achieve higher thermal conductivity, the mold compound manufacturers add materials such as aluminum nitride, alumina, and boron nitride to their resins. For example, by adding aluminum nitride to the mold compound, the equivalent thermal conductivity of the mold material increases to 3.8 W/m-K. However, adding materials with higher thermal conductivities may degrade other properties of the molding compound such as stress performance.

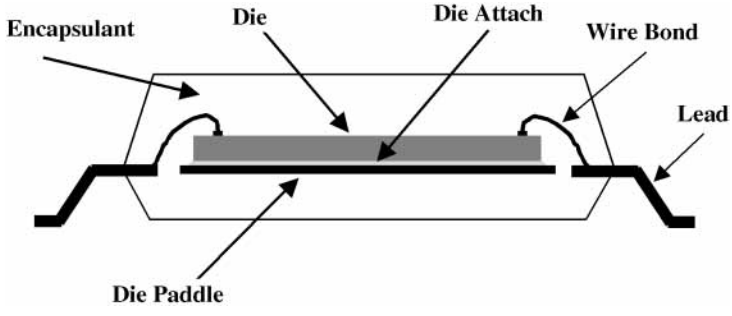

Figure 10.36 Plastic encapsulated microcircuit (PEM).

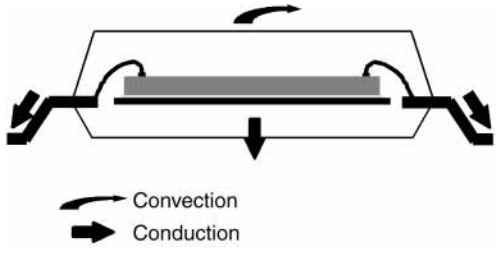

Figure 10.37 Heat paths from a PEM.

To further improve the thermal performance of PEMs, some manufacturers have developed plastic packages in which the bottom of the lead frame is exposed under the die. This type of package is known as an *exposed pad* or *exposed paddle*. An example is shown in Fig. 10.38. This exposed pad eliminates the low-thermal-conductivity plastic in the heat path. A variation of this technique is mounting the die on a low-cost heat spreader and then encapsulating it as shown in Fig. 10.39. Some semiconductor manufacturers are using packages with the exposed pad configuration and forming the leads so that the bottom of the die is directed away from the circuit card. In this configuration, the primary heat path is through convection cooling.[24,77–79]

The lead frame is the heart of the plastic encapsulated microcircuit. Fabricated from either a stamped or chemically etched piece of sheet metal, it acts as a holding fixture during the assembly process. After molding, it becomes an integral part of the package. Electrically, the lead frame provides the electrical connections from the chip to the circuit board. Thermally, the lead frame conducts heat from the chip to the circuit card.

The materials used for lead frames are nickel-iron alloys, clad or copper-based. Nickel-iron alloys are the most widely used metals for lead frames. A popular lead frame material is Alloy 42, a 42 percent nickel-58 percent iron alloy, which has a CTE of 4.5 ppm/°C that is reasonably close to silicon's 2.6 ppm/°C. Able to be heat treated to obtain optimal tensile strength and ductility, Alloy 42 has one significant drawback: a low thermal conductivity of 10.6 W/m-K.[12,80]

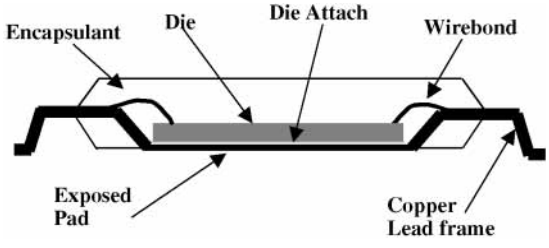

Figure 10.38 Exposed pad plastic package.

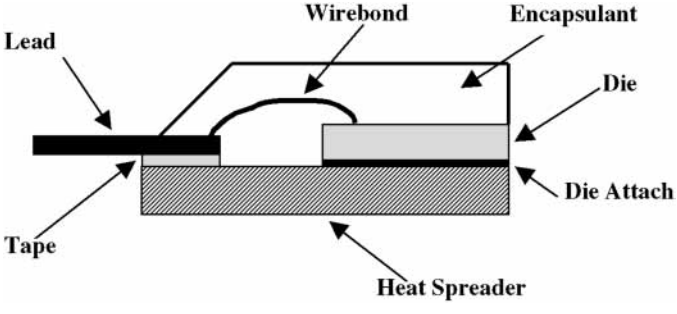

Figure 10.39 Die on heat spreader in plastic package.

To obtain improved thermal conductivity, manufacturers have gone to copper and copper-clad stainless steel lead frames. Copper-clad stainless steel is used for its thermal conductivity improvement over Alloy 42 without increasing the CTE.

Copper, with its high electrical and thermal conductivities, has been used for lead frames on PEMs. However, because of its high CTE, copper lead frames can introduce stresses in the die and die attach, leading to failures.[81]

The plastic materials used for encapsulation are modified epoxy resins with low thermal conductivities. The plastic encapsulation is typically loaded with fused silica and has an equivalent thermal conductivity of 0.5 to 1.0 W/m-K. Table 10.16 lists the thermal conductivities of various materials used for encapsulation.

TABLE 10.16 Thermal Properties of Encapsulation Materials[12,25,82]

Material	Manufacturer	Thermal conductivity @25°C (W/m-K)
Stycast XT5038-6/B 100	Emerson & Cuming	0.4
Stycast 2651-40/Cat 11	Emerson & Cuming	0.6
Stycast 2851 KT	Emerson & Cuming	2.8
Stycast XT5038-6/B 100	Emerson & Cuming	0.6
Hysol FP4450	Dexter*	0.63
Hysol FP4401	Dexter	0.67
Hysol EO1016	Dexter	0.39
Hysol FP4322	Dexter	1.0
HIPEC 648	Dow Corning	0.094
GE RTV6126	General Electric	0.19

*Dexter is now Loctite Corp.

The need to make a large number of interconnections (greater than 200) to a package in a small footprint has driven physical designers from their use of flat packs to ball grid arrays (BGAs). Although BGAs also provide ease of manufacture, low electrical parasitics, and a small footprint, they introduce unique cooling issues with respect to the heat paths and materials. There are three basic types of BGAs: tape (TBGA), plastic (PBGA), and ceramic (CBGA). Their construction and heat removal paths will be discussed in the subsequent sections.

Lau and Chen[83] have shown that the amount of heat removed through conduction from a plastic BGA with an integral heat sink is less than 50 percent. Approximately 40 percent is removed through convection. Although the actual percentages will vary by BGA construction, these percentages can be applied to all BGA types as a first approximation.

In the TBGA, as shown in Fig. 10.40, the die sits, cavity down, on the integral flat copper or aluminum heat sink. This allows the heat to spread from the die to the overall dimension of the heat sink. As shown in Fig. 10.41, there are two heat paths from this point—convection to the air and conduction through the BGA package and balls to the circuit card. To aid in convection cooling, a finned heat sink can be attached to the BGA heat sink. The heat path through the package is hindered by the high thermal resistance of the tape layer, although extremely thin (0.002 to 0.004 in), and is typically composed of a polyimide with a thermal conductivity of 0.27 W/m-K. From the tape layer to the circuit card are solder balls. For Sn 63 solder balls, the thermal conductivity is 51 W/m-K. The thermal conductivities of other solder compositions can be used and are listed in Table 10.5.

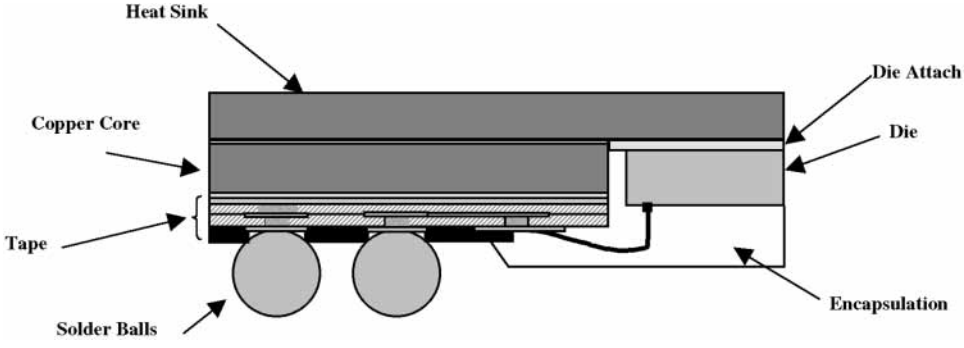

Figure 10.40 TBGA cross section.

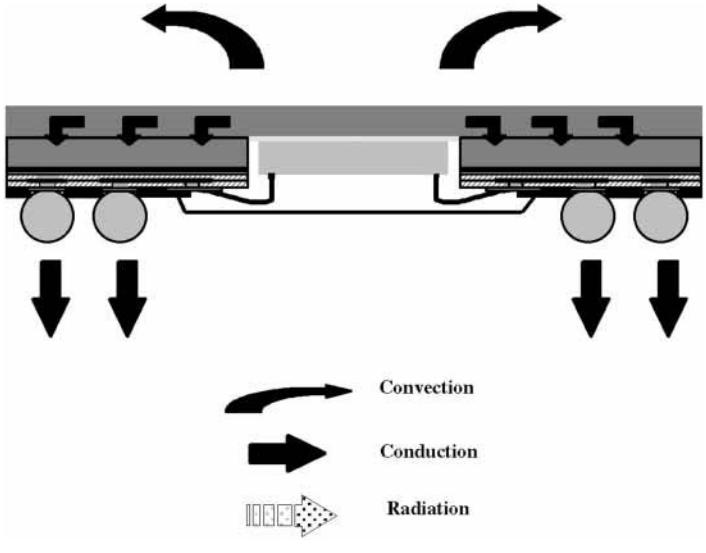

Figure 10.41 Heat paths in TBGA.

Without forced air and a finned heat sink, a 27-mm square TBGA with 256 balls and a die 6 mm square typically has a thermal resistance (junction-to-air) of 10 to 15°C/W.

The die is protected from the environment with a glob-top encapsulant. Typically, these potting materials have a thermal conductivity in the range of 0.1 to 2.8 W/m-K. See Table 10.16 for the thermal properties of encapsulants.

Having a substrate fabricated with printed circuit board materials (copper and polyimide), the TBGA has a CTE that matches most circuit cards and does not pose the problem of solder joint cracking.

In the PBGA, the die sits on a substrate fabricated from a circuit card material such as epoxy or bismaleimide/triazine (BT). There are two configurations of the PBGA as shown in Fig. 10.42: die-up and die-down. In the die-up configuration (Fig. 10.42b), there can be a full array of solder balls on the substrate. Not only does this configuration give the maximum number of interconnections, it provides a more direct thermal path from the die to the circuit card. A version of the die-up configuration shown in Fig. 10.42c, known as the thermally enhanced BGA, has a set of solder balls directly under the die that are used only for improving the thermal path. In the die-down configuration (Fig. 10.42a), a heat sink can be attached to the back of the BGA to enhance convection. The substrates used for plastic ball grid arrays have thermal conductivities in the range of 0.1 to 0.2 W/m-K. The heat paths in the plastic ball grid array are shown in Fig. 10.43.

Without forced air and a finned heat sink, a 27-mm square PBGA with 256 balls having a die size of 6 mm square typically has a thermal resistance (junction-to-air with natural convection) of 18 to 26°C/W. This high value of thermal resistance can be attributed to the low thermal conductivity of the FR-4 (0.35 W/m-K) or BCB (0.14 W/m-K) material composing the substrate or body of the package.

Having a substrate fabricated with printed circuit board materials, the PBGA has a CTE that matches most circuit cards and does not pose the problem of solder joint cracking. The die is protected from the environment with a glob-top encapsulant with thermal properties listed in Table 10.16.

The ceramic ball grid array as shown in Fig. 10.44 provides significantly improved thermal conductivity over the plastic ball grid array as a result of the significantly higher thermal conductivities of the alumina or aluminum nitride substrates. Alumina has a thermal conductivity of 21 W/m-K, whereas aluminum nitride has a thermal conductivity of 170 W/m-K. These conductivities are several orders of magnitude higher than those for plastic ball grid array substrates.

Like the PBGA, the CBGA has two configurations: die-up and die-down. The die-up configuration is shown in Fig. 10.44. The heat paths from a CBGA are shown in Fig. 10.45. In the die-down configuration, a heat sink can be attached to the back of the BGA to enhance convection.

Having a substrate fabricated with a low-CTE ceramic, the CBGA has a CTE that is significantly lower than that of printed circuit cards. During temperature cycling, the CTE mismatch between the CBGA and the circuit card can result in solder joint cracking at the balls. To minimize this problem, some

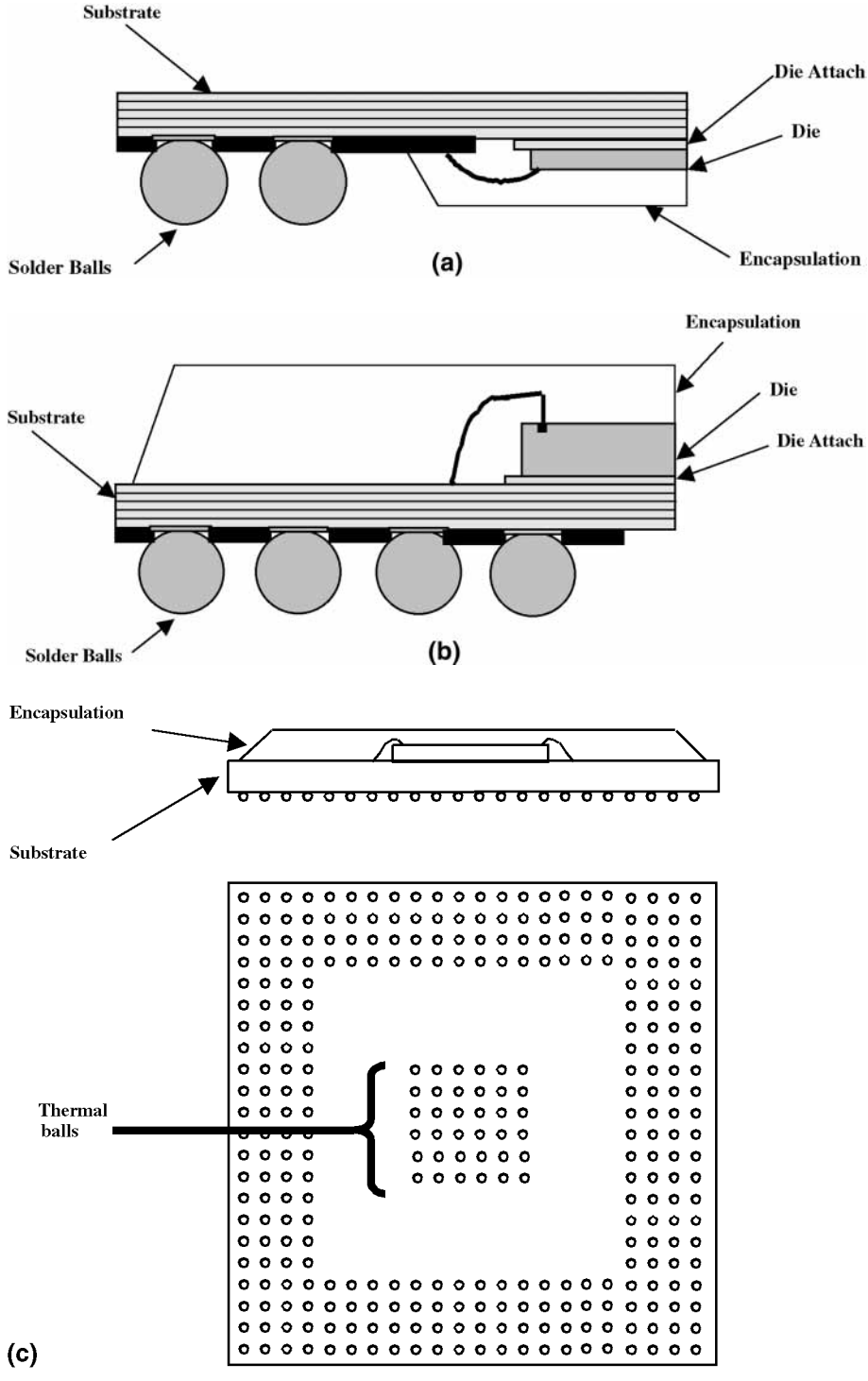

Figure 10.42 PBGA configurations: *(a)* die-down, *(b)* die-up, and *(c)* thermally enhanced.

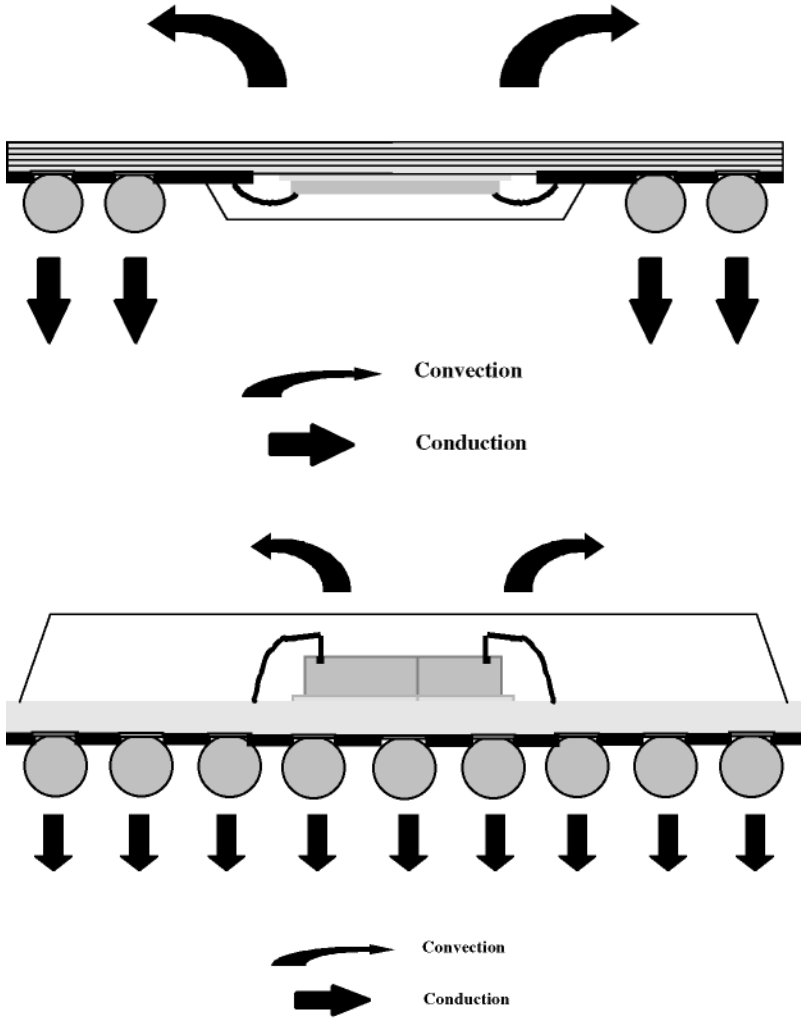

Figure 10.43 Heat paths in PBGA.

BGA manufacturers have gone to a column of solder in lieu of the ball to reduce the stresses. Some circuit card assemblers have gone to an underfill material between the BGA and the circuit card to help reduce the stresses. The die is protected from the environment by a glob-top encapsulant with the thermal properties listed in Table 10.16.

A chip-scale package (CSP) is defined as an IC package that has an area footprint equal to or less than 1.2× the footprint of the die.[84] In appearance, it looks like a miniature ball grid array. One manufacturer (Tessera) even calls its CSP a μBGA. A variety of configurations of CSPs are available as shown in the cross sections in Fig. 10.46. All of the chip-scale packages make use of solder balls with a pitch as fine as 0.5 mm in an area array for their interconnections.[85]

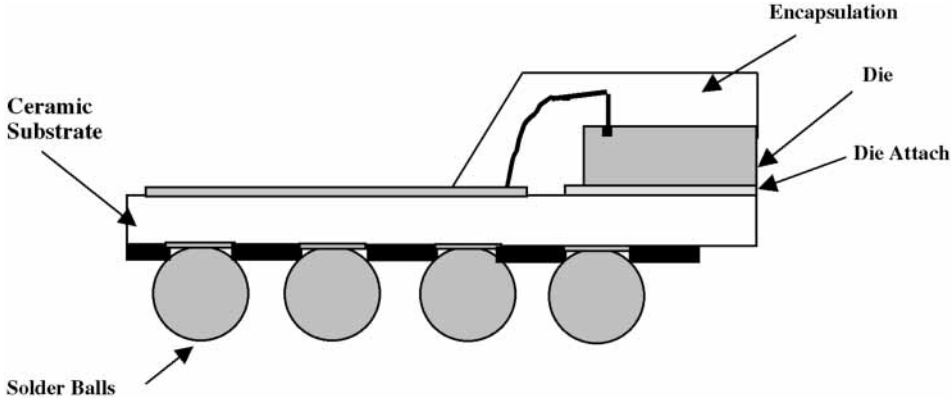

Figure 10.44 CBGA cross section.

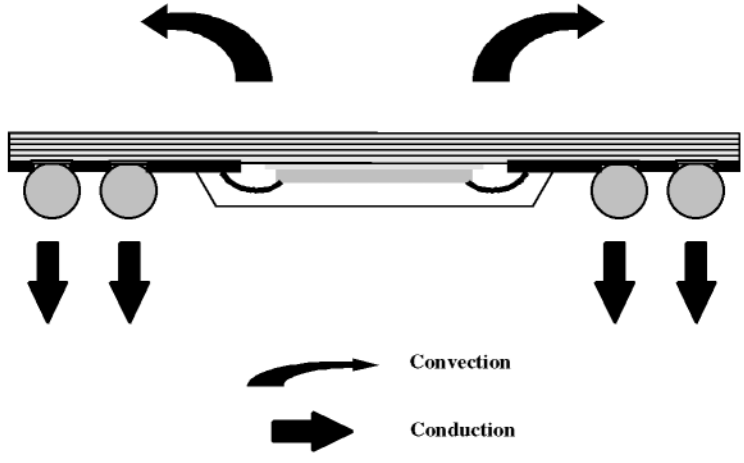

Figure 10.45 Heat paths in CBGA.

There are two heat paths for chip-scale packages: conduction through the balls to the circuit card and convection to the air as shown in Fig. 10.47. The conductive heat path is limited by the presence of a low-thermal-conductivity polyimide film and the limited cross-sectional area of the solder balls.

Some circuit card assemblers have gone to a underfill material between the CSP and the circuit card to help reduce the stresses.

For high-density packaging applications, some physical designers have eliminated the package and placed the chips directly on a board or substrate. To protect the chip from the elements and handling, the chips are encapsulated. This packaging technology is known as chip-on-board (COB). A cross section of a die in a COB application is shown in Fig. 10.48. The die is mounted with a polymeric material directly to the board, typically a printed circuit card, and then wire bonded. All of the semiconductors are then encapsulated with a potting material such as FP4401.

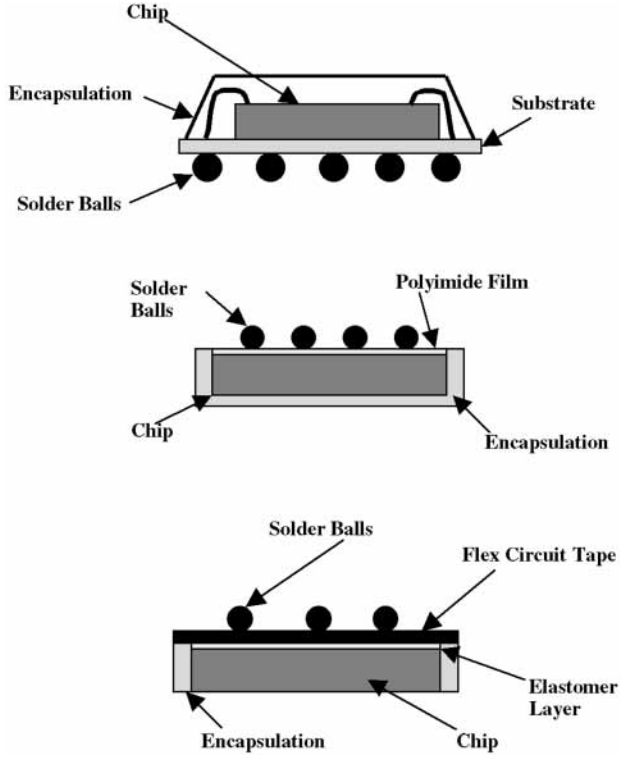

Figure 10.46 Chip-scale package (CSP) cross sections.

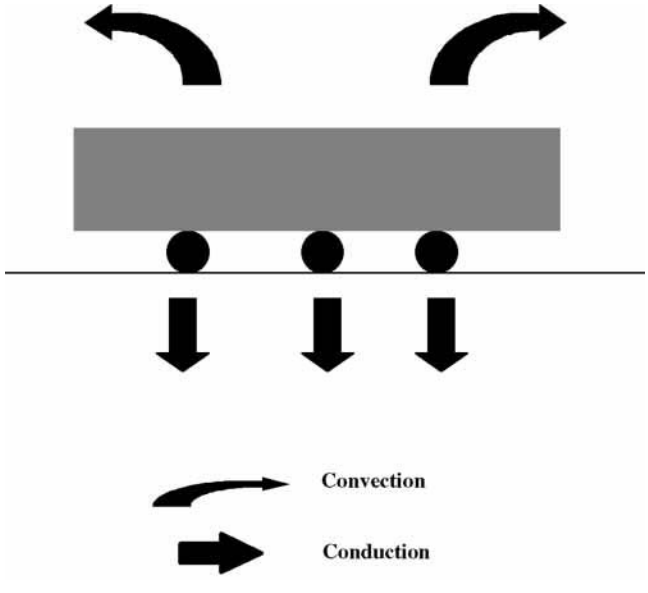

Figure 10.47 CSP heat paths.

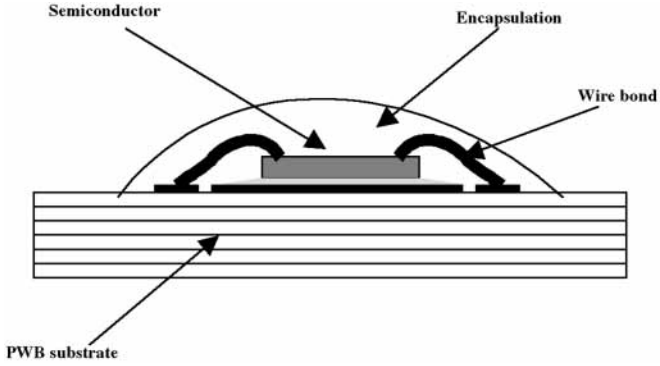

Figure 10.48 Chip-on-board (COB).

In COB, there are two heat paths from the semiconductor as shown in Fig. 10.49. The first and prime path is from the die to the circuit card through the die attach material. The second is from the die through the encapsulation material to the air. The potting materials, with thermal conductivities in the range of 0.4 to 1.0 W/m-K, have an insignificant effect on the heat transfer. By not using a package, there is one less thermal resistance in the heat path. However, the board or circuit card used as the substrate has a thermal conductivity in the range of 0.1 to 0.3 W/m-K, which is two orders of magnitude

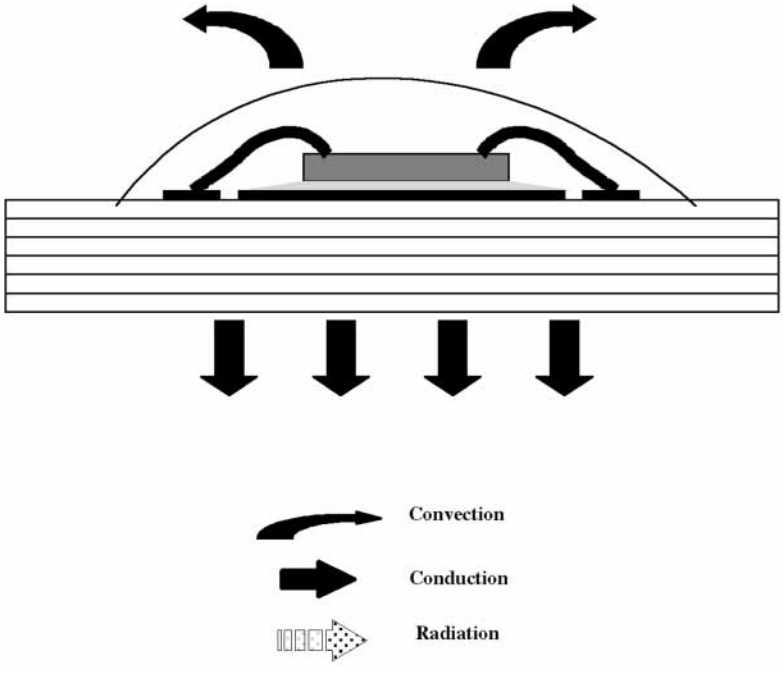

Figure 10.49 Heat paths in COB.

lower than the 21 W/m-K conductivity of 96 percent alumina. The resulting thermal resistance of the COB assembly may be higher, and techniques for reducing it may be required.

In one version of COB, chips are attached to a ceramic substrate and then encapsulated. This method has a significantly lower thermal resistance than the organic-based boards.

An alternative die attach method for COB is flip-chip. The heat path from die goes through the solder balls into the circuit card. The heat path through the potting material is also small for flip-chip attach.

10.5.5.2 Hermetic packages. For high-reliability and severe-environment applications, hermetic packages with either ceramic or metal bases are used. Cross-sectional views of various hermetic packages are shown in Fig. 10.50. The prime heat path in a hermetic package is conduction through the base. A secondary but very minor heat path is convection. The base in a hermetic package is the key material in determining the thermal resistance of the packaged semiconductor(s). The base material, which can be either ceramic or metal, is discussed below.

The most commonly used ceramic package material is cofired 92 percent alumina with a thermal conductivity of 17 W/m-K. The die is attached to the base of the package with a polymeric material, silver-glass, or some type of solder. To reduce the thermal resistance, the package designer can make use of filled thermal vias in the ceramic base. Equations for modeling the thermal resistance in substrates with vias can be found in Sec. 10.5.7, with the thermal conductivities of the board material changed to 17 W/m-K and the via fill material changed to 130 W/m-K for tungsten.[19]

In high-performance ceramic packages, the base may be a higher-thermal-conductivity material such as beryllium oxide or aluminum nitride with a metal ring frame made from a material such as Kovar.

The thermal properties of the various ceramic materials used for hermetic packages, the same as those for substrates, are listed in Tables 10.8 and 10.10.

To aid the heat spreading in an alumina package, the package designer can use a heat spreader such as copper-tungsten as shown in Fig. 10.51. Copper-tungsten is used because it has a high thermal conductivity (approximately 180 W/m-K, depending on composition) and a CTE in the 7 to 8 ppm/°C range that matches alumina. If the die needs to be electrical isolated, the heat spreader is brazed to the ceramic base. For applications wherein the die can be electrically connected to the package base, the die can sit on a copper-tungsten plug as shown in Fig. 10.52. This plug is brazed into a cavity in the package and offers improved thermal conductivity over the isolated heat spreader.

Low-temperature cofired ceramic (LTCC) can also be used as a hermetic package. The base of the package is fabricated in the manner described in Sec. 10.5.3.4 with a Kovar ring frame/seal ring attached with solder as shown in Fig. 10.53. The same thermal resistance improvement techniques discussed previously for LTCC substrates can be applied to the LTCC package.

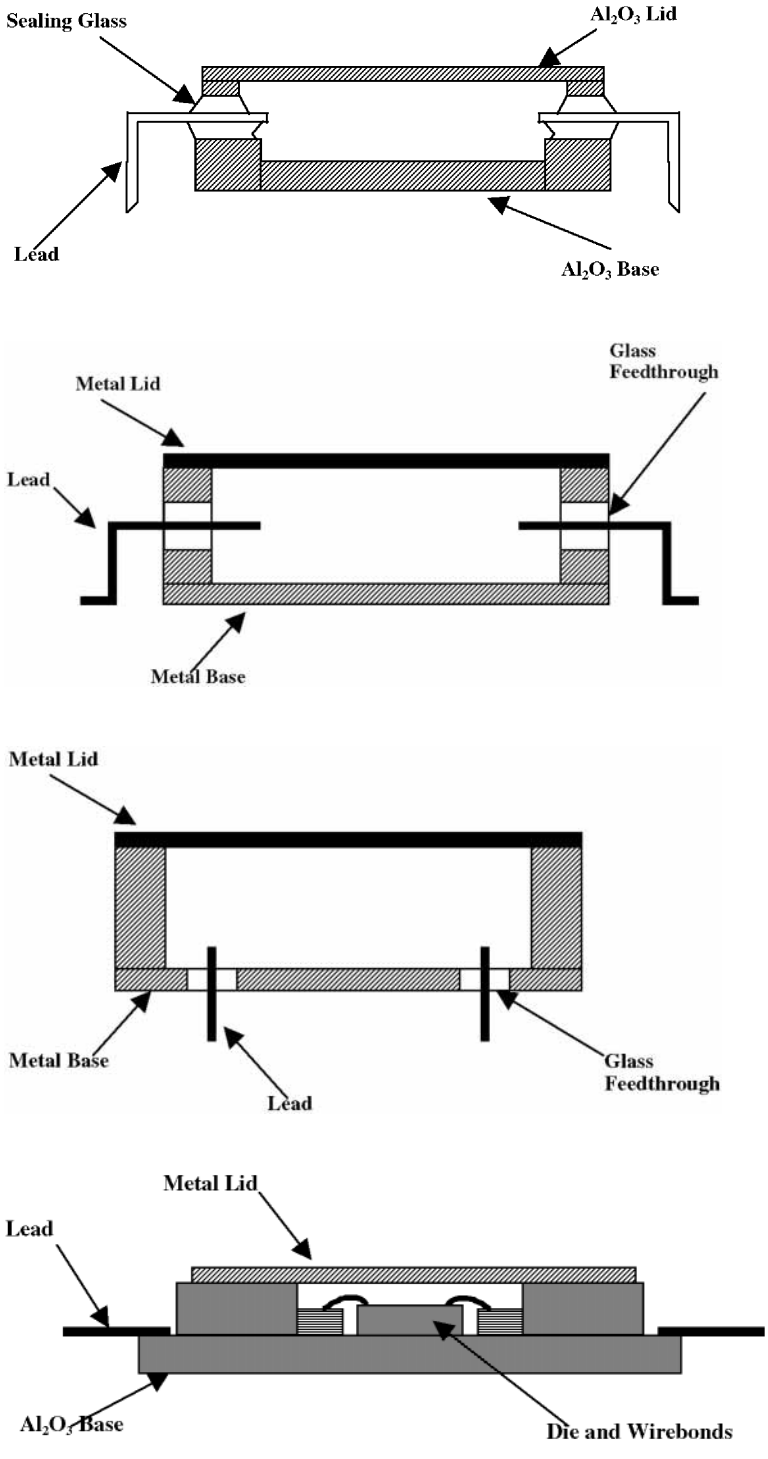

Figure 10.50 Cross-sectional views of hermetic packages.

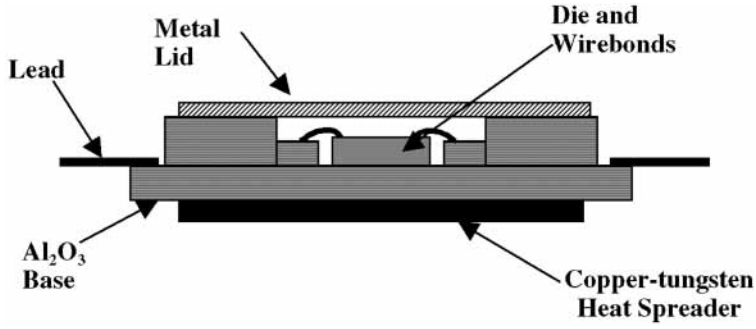

Figure 10.51 Ceramic package with copper-tungsten heat spreader.

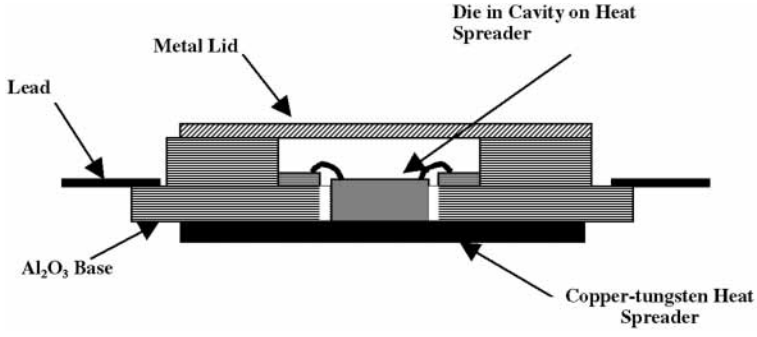

Figure 10.52 Direct chip attach to copper tungsten base of ceramic package.

Metal packages employing glass-to-metal feedthroughs are widely used for single-chip and multichip applications with low I/O counts. The density of glass-to-metal feedthroughs is typically limited to lead pitches of 0.050 in because of glass cracking. Kovar and steel packages are typically used for low-power applications. For high-power applications, materials such as copper, copper-tungsten, molybdenum, Silvar™, and aluminum-silicon carbide are used for the package base.

Kovar, an alloy of 54 percent iron, 29 percent nickel, and 17 percent cobalt,[80] has a CTE at 25°C of 5.5 ppm/°C that closely matches alumina, beryllia, and aluminum nitride.[12] It is also known as ASTM F-15 alloy and is used as a package base in single-chip and multichip (hybrid and MCM) applications in which there are low power densities. When used with certain types of glass as feedthroughs on packages, it forms a hermetic molecular bond. A plot of the CTE of Kovar over a wide temperature range is shown in Fig. 10.54.

The thermal conductivity of Kovar, 16.5 W/m-K at 30°C and 17.6 W/m-K at 100°C,[12] is considered low, so Kovar should be avoided as a package base in high-power-density applications.

The thermal properties of the various metals used for package bases are listed in Table 10.17. Table 10.18 lists the properties of metal composite materials used for package bases.

TABLE 10.17 Thermal Properties of Metals Used for Package Bases and Printed Circuit Card Cores[12,13]

Material	Thermal conductivity @25°C (W/m-K)	Thermal conductivity @100°C (W/m-K)	CTE @25°C (ppm/°C)
Kovar	16.5	17.6	5.5
OFHC copper	401	395	16.5
Glidcop	365		16.6
Alloy 52	14		10.0–10.5
Molybdenum	138		5.35
Aluminum	237	238	23.2

TABLE 10.18 Properties of Composite Materials[87–91]

Composite material	Composition	Thermal conductivity @25°C (W/m-K)	Thermal conductivity @100°C (W/m-K)	CTE (ppm/°C)	Vendor P/N
CuW	80 W, 20 Cu	185	197	8.3	
	82 W, 18 Cu	185		7.8	
	85 W, 15 Cu	180	183	7.2	
	87 W, 13 Cu	175		6.9	
	90 W, 10 Cu	170	176	6.5	
Silvar	61 Invar, 39 Ag	153		6.5	
	72 Kovar, 28 Ag	110		7.0	
AlSiC	30-70 SiC, balance Al	160–220		6.2–15	
Al-Be	62 Al, 38 Be	212	195	13.2	AlBeMet AM162
Al-graphite		230 x & y 120 z		3.0-5.0 x & y 24 + z	MMCC GA 4-230
		200 x & y 125 z		6.5–9.5 x & y 24 + z	MMCC GA 7-200
Cu-graphite		300 x & y 200z		7.4	
Cu-Mo	20 Cu, 80 Mo	170		8.0	
	15 Cu, 85 Mo	160		7.0	

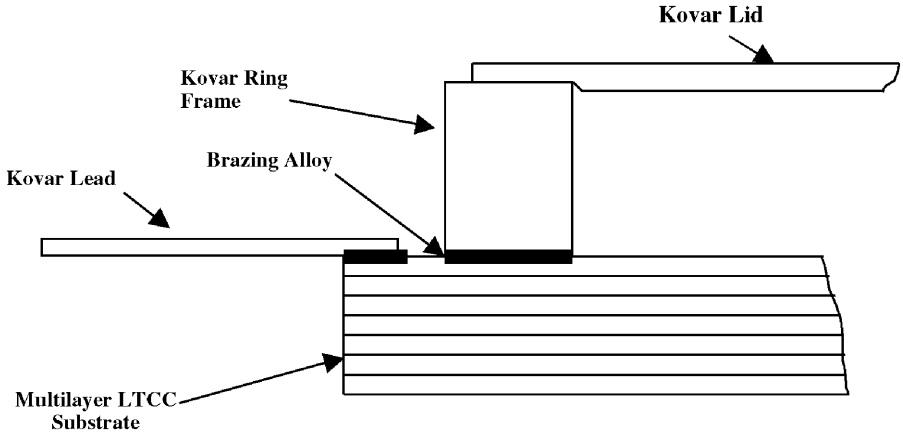

Figure 10.53 Hermetic LTCC package construction.

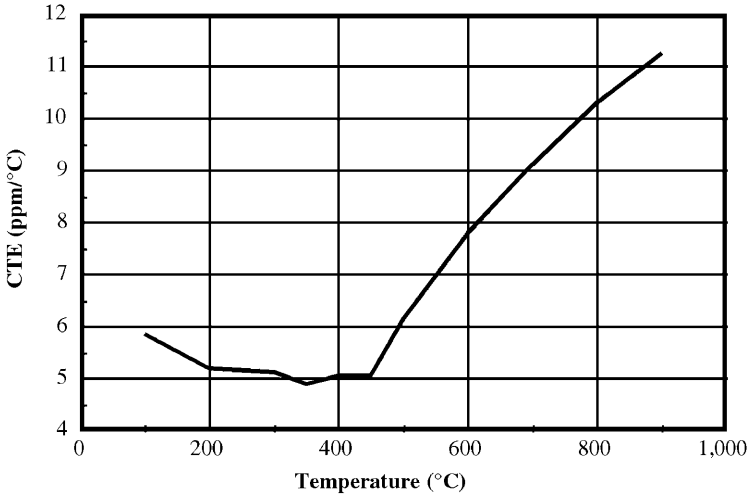

Figure 10.54 CTE of Kovar.

Pure or elemental copper, also known as oxygen-free high-conductivity copper (OFHC), having a thermal conductivity of 401 W/m-K, is ideal from a heat transfer standpoint for a package base. However, with its high CTE of 16.5 ppm/°C,[12] copper can introduce stresses into rigidly attached ceramic substrates. To reduce the stresses in ceramic substrates, the physical designer can partition the layout so that several smaller substrates are used instead of one large one. An example of a power hybrid with a copper package and multiple substrates is shown in Fig. 10.55. OFHC copper has the second-lowest resistivity of the elements, 1.72 μΩ-cm, second only to silver, at 1.59 μΩ-cm.[65]

Pure copper has a low annealing point as shown in Fig. 10.56. Package bases made from pure copper exhibit softening that can result in cracked die and/or substrates. To raise the annealing point of the copper, manufacturers

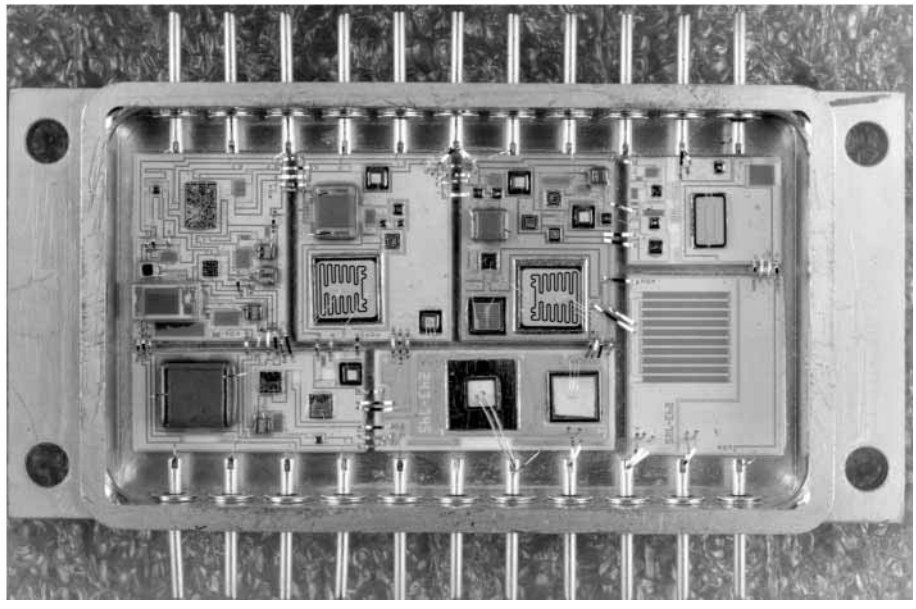

Figure 10.55 Multiple substrates in a copper package.

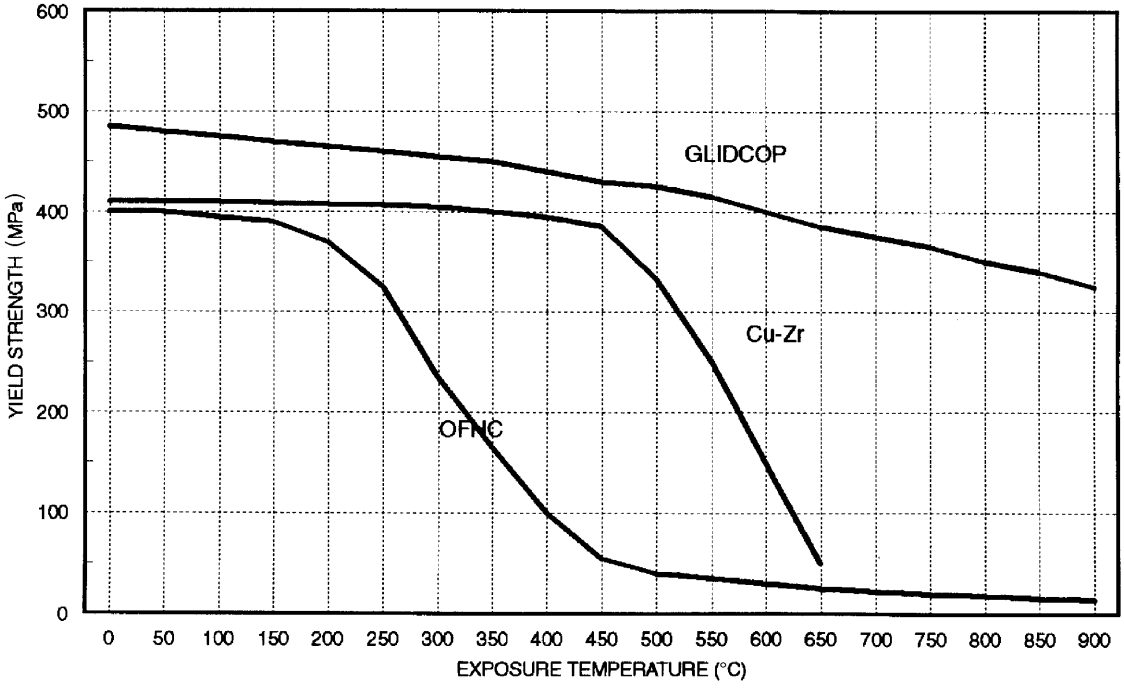

Figure 10.56 Yield strengths of OFHC copper, Glidcop, and zirconium copper.

typically incorporate a small amount of material such as alumina, zirconium, silver, or silicon in the melt. This material has the effect of raising the annealing point of OFHC copper from 320 to 400°C with only slight losses in thermal and electrical conductivity. One such material, Glidcop® * is composed of 99.7 percent copper and 0.3 percent alumina. With the addition of the alumina, the thermal conductivity is reduced to 365 W/m-K, and its electrical resistivity is increased to 1.85 mW-cm.[13] The yield strengths of Glidcop and zirconium-copper are shown in Fig. 10.56, along with OFHC copper.

Because of its ease of machinability, aluminum and its alloys are typically used as housings on microwave integrated circuits (MICs). Elemental aluminum has a high thermal conductivity of 237 W/m-K at 25°C. However, the CTE of aluminum is high, at 23.2 ppm/°C.[12] To alleviate this problem, physical designers typically use many small substrates in lieu of one large one in a manner similar to the hybrid shown in Fig. 10.9. The thermal properties of aluminum are listed in Table 10.17.

Stainless steel is used for hermetic packages wherein corrosion resistance is required. One such application is implantable medical electronics. To achieve hermetic leads in stainless steel, compression seals are used, because fused glass-to-metal seals cannot be formed. There are a variety of formulations for stainless steel. One formulation, designated 1010 steel, has a thermal conductivity of 49.8 W/m-K, approximately three times that of Kovar. The CTE of 12.6 ppm/°C poses a thermal mismatch with ceramics and semiconductors. Another stainless steel, Type 430, has a much lower thermal conductivity of 26.1 W/m-K.[19]

Molybdenum is used for bases on hermetic packages in conjunction with Kovar ring frames. Having a CTE of 5.35 ppm/°C, molybdenum closely matches the CTE of Kovar and alumina. Its thermal conductivity of 138 W/m-K is reasonably high and can be used for many medium and high-power-density applications.[13] One major drawback of molybdenum bases is that the best flatness available is 0.002 inch per inch. Another issue is the brittleness of the molybdenum after it has been recrystallized.

Composites are a combination of materials that are not alloyed and have properties that none of the constituent materials has by itself. The materials are selected for use in a composite to take advantage of one or more characteristic properties of the individual material. For example, copper has both high thermal conductivity and high CTE. The high thermal conductivity is the desired property, but a lower CTE would be welcomed. Combining 80 to 90 percent tungsten with copper produces a material with a CTE matching ceramics and Kovar.[92] In some applications, weight is the parameter that needs to be minimized. To achieve low weight in a package, the materials need to have low densities. Aluminum-silicon-carbide is a composite that offers low weight and a tailored CTE.

Many composite materials tend to be anisotropic; i.e., they have properties that differ according to the direction of measurement. The thermal conductivi-

* Glidcop is a registered trademark of SCM Metal Products.

ties of various composite materials used for package bases are listed in Table 10.18 with a notation for the thermal conductivity and expansion values in each of the planes.

Several composites, such as aluminum-silicon-carbide, copper-molybdenum, and copper-graphite, are used for bases in hermetic packages. These materials and others, such as aluminum-graphite and copper-Invar-copper, are also used as cores for circuit cards, as discussed in Sec. 10.5.7.

To alleviate the CTE mismatch between ceramic substrates and copper package bases, some package manufacturers are using a composite of copper and tungsten. An 85 percent tungsten, 15 percent copper composite has a CTE of 7.2 ppm/°C and a thermal conductivity of 180 W/m-K. Other combinations of copper and tungsten are available and are tabulated in Table 10.18. Copper-tungsten is used in a variety of ways in electronic packaging. It is used as a package base, as a heat sink, and also as a heat spreader. One major disadvantage of copper-tungsten is its high density, a result of the high percentage of tungsten. The 85-15 copper-tungsten material has a density of 16.1 gm/cm^3.[87]

Copper-tungsten is also used as a heat sink for substrates in nonhermetic applications. As discussed in Sec. 10.5.5.2.1, copper-tungsten is used as a base on hermetic ceramic packages or as a heat spreader.

Because of its high density, copper-tungsten provides excellent radiation shielding for total ionizing dose (TID) environments. If aluminum were used for a radiation shield, it would have to be 16 times as thick as a copper-tungsten to obtain the same amount of shielding.

Silvar* is a powder metallurgical composite of silver and an iron-based alloy. One version of Silvar uses 61 percent Invar 36† and 39 percent silver. Invar 36 is a low-expansion alloy of 63 percent iron, 39 percent nickel, and traces of carbon, manganese, and silicon. This isotropic controlled composite of silver and Invar has a CTE of 6.5 ppm/°C and a thermal conductivity of 153 W/m-K. Another version of Silvar is composed of 72 percent Kovar and 28 percent silver, which has a CTE of 7ppm/°C and a thermal conductivity of 110 W/m-K.[93,94]

Silvar is manufactured in a variety of methods, including liquid metal sintering, coblending, hot isostatic pressing, and liquid metal infiltration. It can be easily stamped, machined, or formed and is able to be brazed or soldered without the need for prior electroplating.

Aluminum-silicon-carbide (AlSiC) is a metal matrix composite (MMC) consisting of 30 to 70 percent silicon carbide and aluminum for the balance. It can be fabricated in a number of ways, including compocasting, high-pressure casting, pressureless infiltration, and powder metallurgy. The resulting AlSiC material consists of aluminum alloys with suspended silicon carbide particles. The CTE of AlSiC is tailorable, based on the percentages of the constituent materials. As shown in Fig. 10.57, increasing the silicon carbide content has the effect of lowering the CTE from elemental aluminum's high 23.2 ppm/°C.

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* Silvar is a trademark of Engineered Materials Solutions, Inc.

† Invar 36 is a registered trademark of Carpenter Technology Corp.

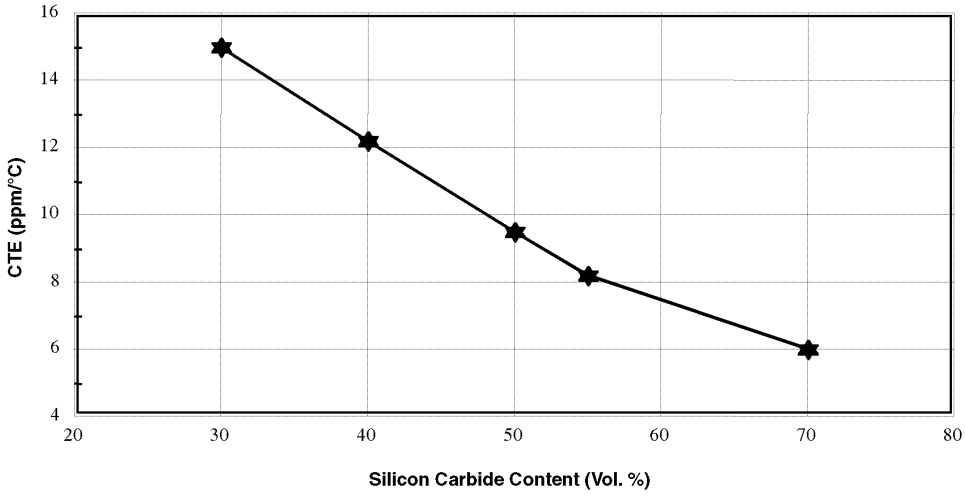


Figure 10.57 CTE of aluminum-silicon-carbide as a function of silicon carbide content.

Varying the silicon carbide content has minimal effect on tailoring the thermal conductivity, as silicon carbide has a thermal conductivity of 110 W/m-K whereas elemental aluminum has a value of 237 W/m-K. AlSiC, with 70 percent silicon carbide, has a thermal conductivity of 170 W/m-K.[3,12,13]

The weight of AlSiC is a result of the low densities of both aluminum and silicon carbide. Seventy percent silicon carbide AlSiC has a density of 2.79 g/cm^3.[95] AlSiC can be used as a base for a hermetic package or a heat sink, or as a heat spreader.

Mixing copper and molybdenum in a ratio of 15:85 produces a composite with a CTE of 6.7 ppm/°C and a thermal conductivity of 160 W/m-K. There is a slight difference in thermal conductivity in the x- and y-planes as compared to the z-plane. For the copper-molybdenum mixture with 20 percent copper thickness per side, the thermal conductivity is 150 W/m-K in the x- and y-planes and 194 W/m-K in the z-plane. The CTE is an excellent match with ceramics, and the thermal conductivity is relatively high. The tailored CTE of copper-molybdenum allows the use of a Kovar ring frame. The CTEs for ratios other than15:85 are listed in Table 10.18. Copper-molybdenum can be used as a base for a hermetic package or a heat sink, or as a heat spreader.

Carbon-fiber-reinforced copper is attractive for applications with high power densities, as the material offers higher thermal conductivities than tungsten or molybdenum, with CTEs that can be tailored to match any device type or substrate type. The thermal conductivity along the length of a carbon fiber is extremely high at 600 to 750 W/m-K. However, perpendicular to the length, the thermal conductivity is an order of magnitude lower at 51 to 59 W/m-K. The coefficient of expansion along the length of the fiber is –0.5 ppm/°C and 8 ppm/°C perpendicular to the length. When used as a package base or as a heat spreader, carbon fiber is not very efficient in moving the heat from the device to the next level. However, it is extremely efficient in spreading the heat.

Instead of using carbon fiber in a continuous form, discontinuous fiber (randomly oriented pieces of fiber, approximately 10 μm in length) provides a material with a thermal conductivity of 20 to 40 W/m-K in the y- and z-planes and 700 to 800 W/m-K in the x-plane. The CTE in the x-plane is –0.5 ppm/°C and 8 to 10 ppm/°C perpendicular to the length.[96]

All of the above specifications apply for graphite alone. Mixing 51 percent unidirectional graphite with copper produces a material with a thermal conductivity of 494 W/m-K in plane and 128 W/m-K perpendicular to it.

Aluminum-graphite is a metal matrix composite of graphite fiber and aluminum. There are several types of this composite available, as shown in Table 10.18. One such material, GA 4-230 from Metal Matrix Composites Corporation (MMCC), has a CTE of 3.0 to 5.0 ppm/°C from 20 to 300°C. Its thermal conductivity in the x- and y-planes is quite high at 230 W/m-K. In the z-plane, its thermal conductivity decreases to 120 W/m-K.

As a result of the low densities of its component materials, aluminum-graphite has an extremely low overall density. For the MMCC GA 4-230, the density is quite low at 2.40 grams/cm^3.[89]

Aluminum-beryllium (Al-Be) is by definition an alloy consisting of aluminum and beryllium. However, the industry treats it as a composite. Produced under the trade name of AlBeMet® by Brush Wellman, aluminum-beryllia is available as a sheet, plate, or bar with 20 to 75 weight percent beryllia in an aluminum matrix. At room temperature, a 62 percent beryllia/38 percent aluminum ratio produces a material with a CTE of 13.2 ppm/°C and a thermal conductivity of 212 W/m-K. Having a density of 2.07 g/cm^3, Al-Be is used for applications wherein low weight is required.

Because of its beryllium content, machining of Al-Be can cause health risks as described in Sec. 10.5.3.2. The cost of Al-Be is at least an order of magnitude higher than standard aluminum and its alloys because of material and machining costs. In addition to its use as a core for circuit cards, Al-Be is also used for chassis and housings.[90]

Clad materials are produced by high-pressure rolling of a foil onto a base metal and annealing the composite to form a solid-solution weld. By cladding high-CTE materials with lower-CTE materials, a composite with a tailorable CTE is achieved. In addition to the tailorable CTE, the thermal conductivities are changed. Using Eq. (10.26), the effective thermal conductivity of clad materials can be calculated. Two clad materials used in electronic packaging include copper-clad Invar and copper-clad molybdenum. The CTE and thermal conductivities of these materials are listed in Table 10.19.

TABLE 10.19 Thermal Properties of Clad Materials Used for Packages and PCB Cores[7]

Material	Composition	Thermal conductivity @25°C (W/m-K)	CTE @25°C (ppm/°C)
Copper-Invar-copper	1 Cu, 3 Invar, 1 Cu	174 x & y, 24.8 z	6.5
Copper-molybdenum-copper	1 Cu, 6 Mo, 1 Cu	233	6.4

When Invar is clad with foils of copper on each side in the ratio of 1 part copper, 3 parts Invar, and 1 part copper as shown in Fig. 10.58, the resulting material has a CTE of 6.5 ppm/°C. The CTE for other combinations of copper and Invar is shown in Fig. 10.59. The thermal conductivity in the x- and y-planes for this 1:3:1 clad material is a high 174 W/m-K because of the high thermal conductivity of the copper. However, in the z-plane, the thermal conductivity is only 24.8 W/m-K because of the low thermal conductivity of the Invar in the center of the clad combination. The variation of thermal conductivity of copper-clad Invar in the various planes for different percentages of copper is shown in Fig. 10.60.[19,80]

The principal usage of Invar has been as a core on printed circuit cards, in which it tailors the equivalent CTE to a value that reasonably matches that of

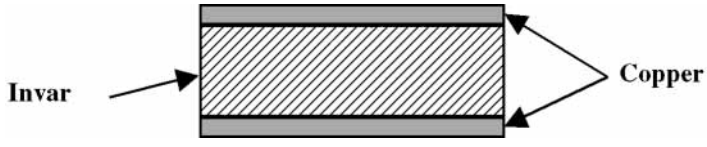


Figure 10.58 Copper-clad Invar construction.

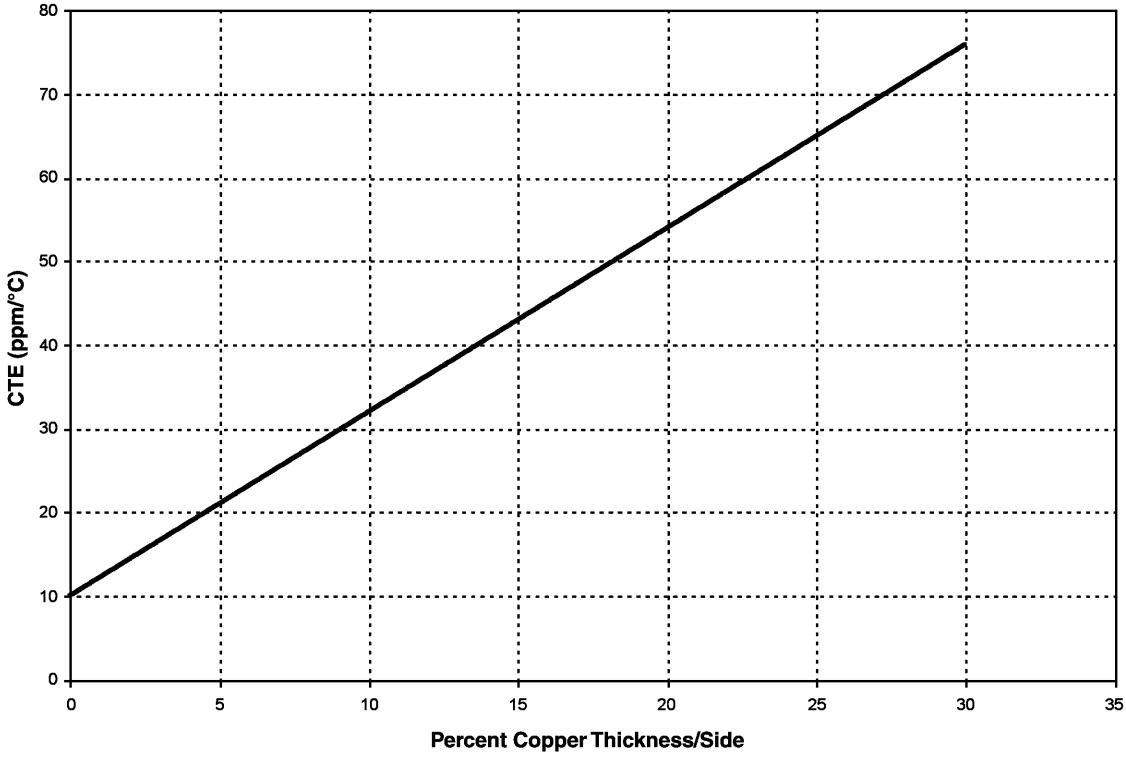


Figure 10.59 Copper-clad Invar CTE.

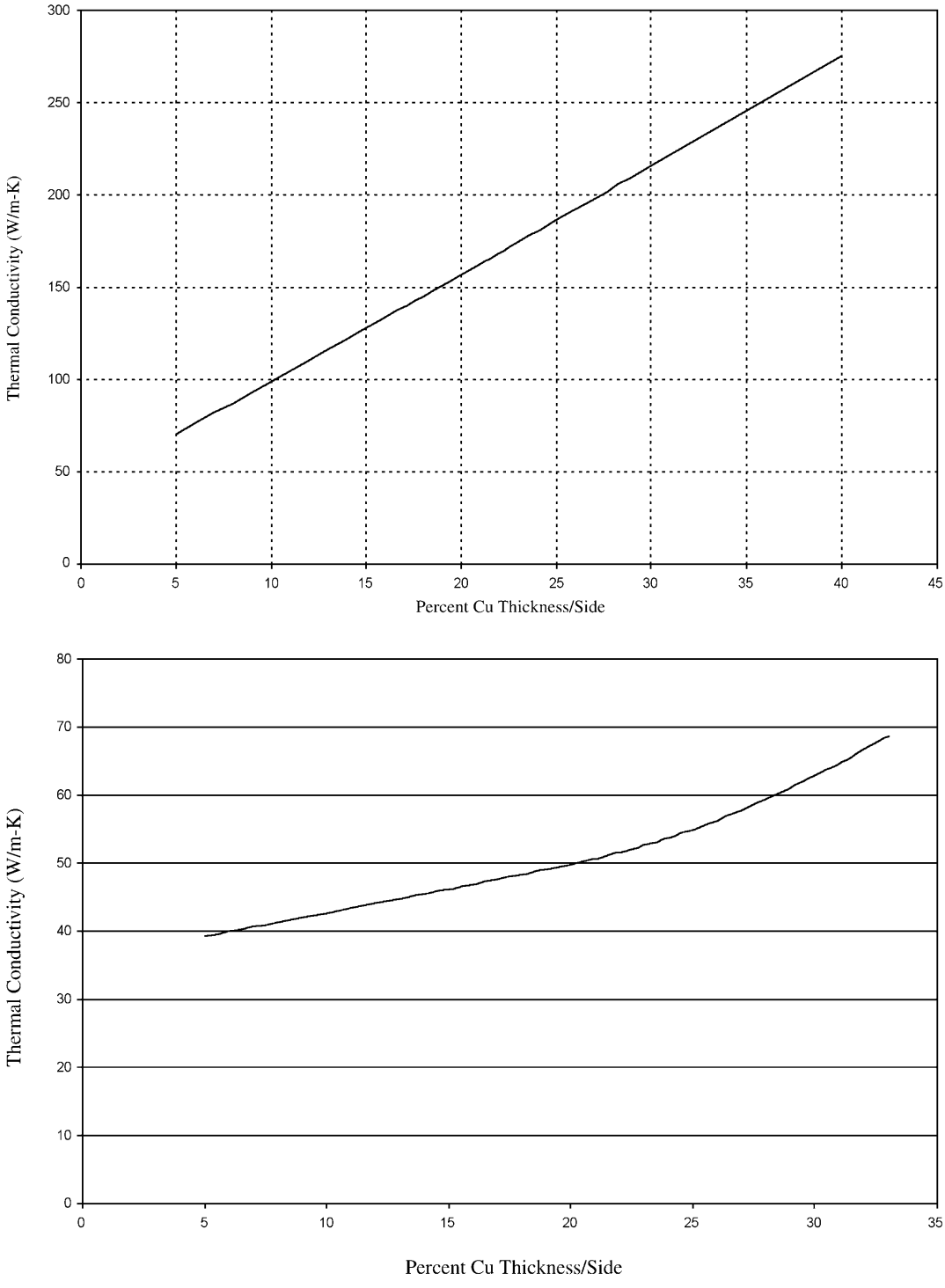


Figure 10.60 Copper-clad Invar thermal conductivity, (top) x- and y-planes and (bottom) z-plane.

ceramic packages. Copper-clad Invar can also be used as a base for hermetic packages.

By cladding molybdenum with copper in the ratio of 1:6:1 as shown in Fig. 10.61, the resulting laminate has a CTE of 6.4 ppm/°C, an excellent match with ceramics and with Kovar and alumina. The CTE for other combinations of copper and molybdenum is shown in Fig. 10.62. The effective thermal conductivity of the laminate is quite high at 233 W/m-K. The thermal conductivity of copper-clad molybdenum as a function of copper thickness is shown in Fig. 10.63. Package bases for hybrids and MCMs have been made with copper-clad molybdenum. Kovar ring frames can be attached reliably because of the close match in temperature coefficients. Copper-clad molybdenum suffers from the same shortcoming of pure molybdenum, i.e., minimum flatness of

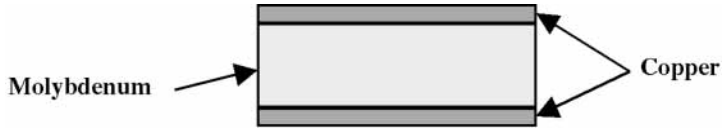


Figure 10.61 Copper-clad molybdenum construction.

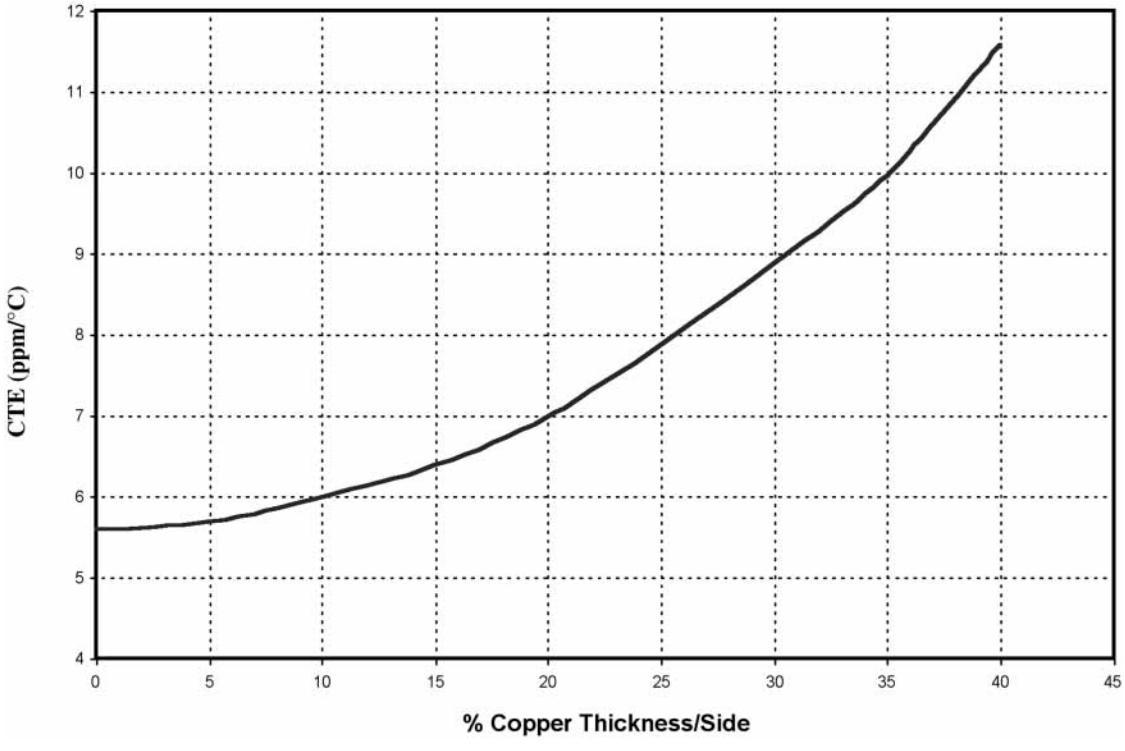
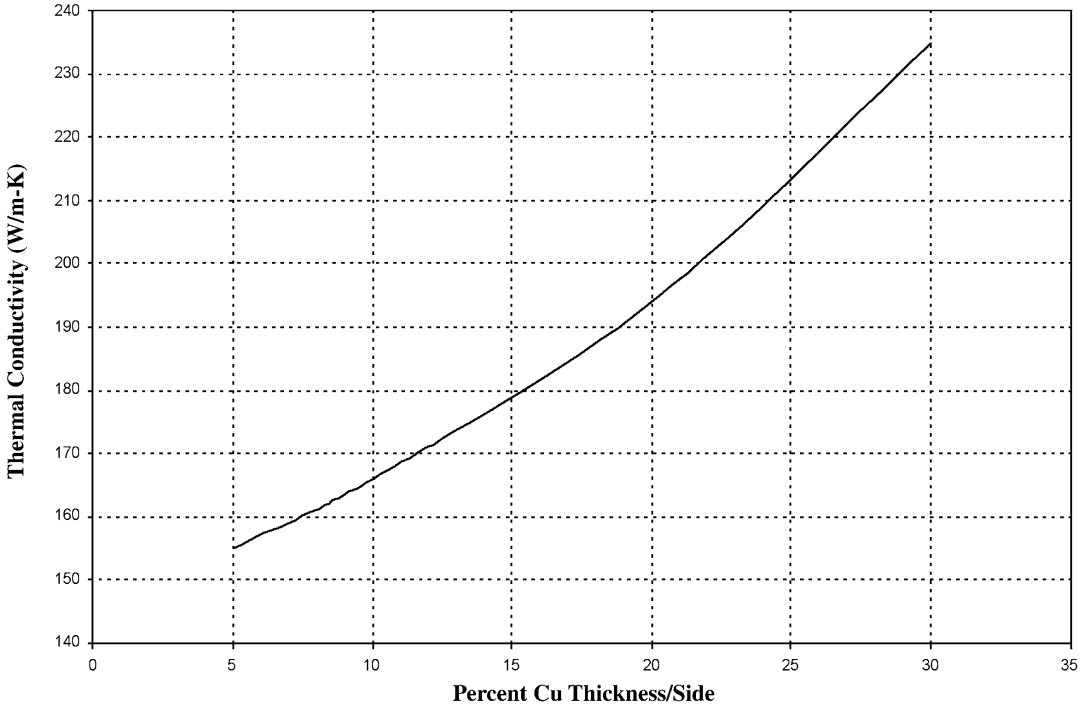


Figure 10.62 Copper-clad molybdenum CTE.



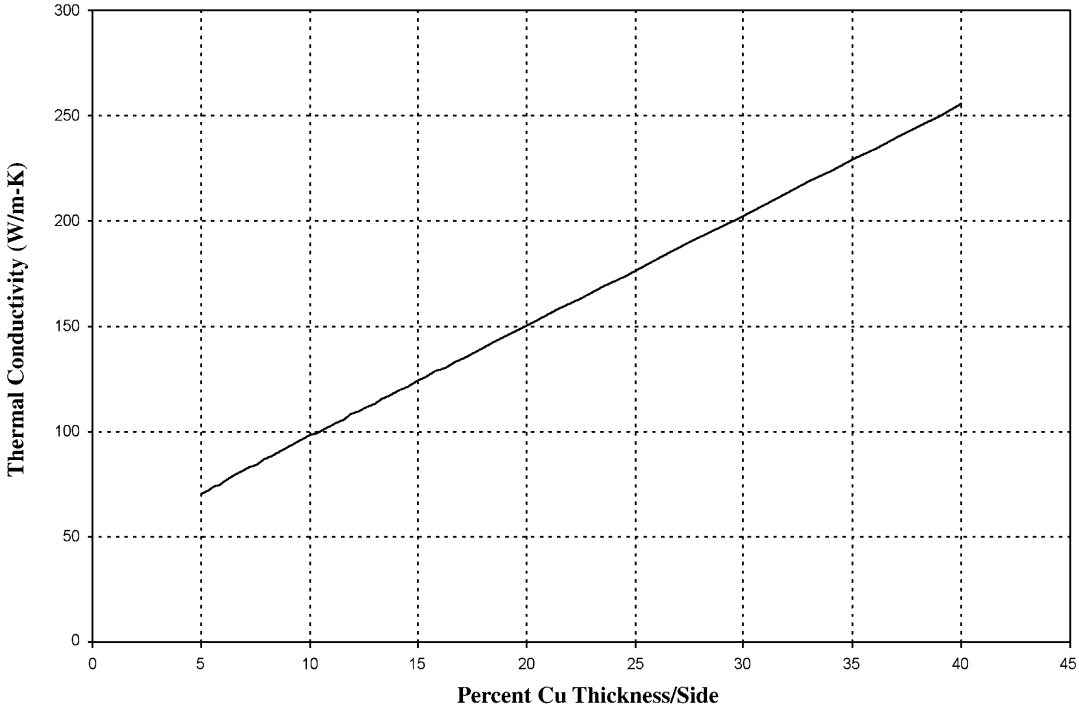


Figure 10.63 Copper-clad molybdenum thermal conductivity in x- and y-planes.

0.002 inch per inch. Copper-molybdenum-copper is also used as heat spreaders with various ceramic substrates and packages.

10.5.6 Thermal interface materials

Air, having a thermal conductivity of 0.026 W/m-K,[97] is a very poor thermal conductor and must be eliminated from the thermal path from junction to heat sink. Every package type, covering all materials, is neither perfectly flat nor perfectly smooth. The portion of a heat sink that interfaces with the electronic package is also not perfectly flat or smooth. At the microscopic level, the interface of the package to the heat sink consists of point-to-point contacts surrounding air pockets as shown in Fig. 10.64. DeSorgo[97] claims that as much as 99 percent of the surfaces between heat sinks and dissipating devices are separated by air. Because circuit card assemblies act as a heat sink to some extent, they will be considered as a heat sink in this discussion. To minimize the thermal resistance caused by the nonsmooth surfaces and the resulting air pockets, several techniques are available. One technique is to apply mechanical pressure to smooth out the interface. This works to some degree when soft metals are used. However, the pressure required to produce an acceptable thermal condition may exceed the materials' strength and produce a degradation or failure.

Another technique of eliminating the gaps is to fill them with a material with high thermal conductivity. Materials used for gap filling include solder, thermal grease, elastomeric pads, conductive adhesives, polyimide films, phase change materials, mica pads, adhesive tapes, polyimide films, and ceramic wafers. Their properties of the various interface materials used are summarized in Table 10.20.

10.5.6.1 Solder. Solder can be used in two different manners to fill the air gaps in the heat sink attachment interface. In the first, solder is reflowed be-

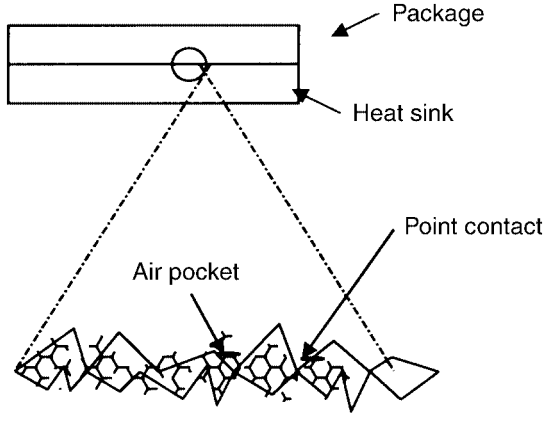


Figure 10.64 Microscopic view of package-to-heat-sink interface.

TABLE 10.20 Thermal Properties of Interface Materials[5,25,29,82,98–100]

Material	Typical thickness (in)	Thermal conductivity (W/m-K)	Dielectric strength (V)
Thermal grease	0.003	0.7	
Sn 63	0.005	50	na
Mica	0.002–0.003	0.71	
Phase change	0.002	4	3900
Elastomer	0.010	6	4000
Gap filler	0.010	1.5	4000
Epoxy film	0.003	6.5	na
Diamond-filled epoxy	0.005	11.6	>2250
Underfill	0.005	0.25–1.1	
Polymeric fiber		30	
Adhesive tape	0.002–0.015	0.6	
Ceramic wafers			
Alumina wafer	0.015–0.060	25	>9000
Aluminum nitride wafer	0.015–0.060	170	>9000
Beryllia wafer	0.015–0.060	217	>11,500
Polyimide film		0.15	

tween the device and the heat sink. Typically, the solder used is lead-tin, which has a thermal conductivity of 51 W/m-°C.[13] This provides several orders of magnitude improvement over the air gap. However, the use of reflow-solder attach may cause other problems.

- The solder reflow temperature may exceed the device's maximum temperature.
- There may be trapped flux that also produces voids.
- The device and heat sink may have large CTE differences, and this could result in bowing or cracking of either the heat sink or the device.

The second way solder can be used to fill gaps is to use a pre cut sheet of solder (a preform) between the device and the heat sink. By applying mechanical pressure, the solder, having a high lead content, compresses easily and fills the gaps. This technique avoids all of the shortcomings addressed for the reflowed solder. The only shortcoming of using the preform technique is that the compressed thickness is typically higher than with reflow soldering.

10.5.6.2 Thermal grease. Thermal grease uses silicone or hydrocarbon oil as a base and is filled with a thermally conductive material, which may range from aluminum oxide and zinc oxide powder to CVD diamond. The resulting thermal resistance is a function of the particle size of the filler material and the thermal conductivity of the filler and vehicle. Larger particles may result in a larger bond thickness and a higher thermal resistance. The typical thermal grease used in production has a thermal conductivity of approximately 1.0 W/m-K. Some newer greases have improved this to as high as 16.0 W/m-K.[97,101]

Thermal greases are somewhat volatile and may evaporate over time. Because these greases do not provide adhesion, some form of mechanical attachment is necessary to apply sufficient pressure and minimize bond thickness. Care in the application of silicon-based greases is required, as they can contaminate solder areas. It should be noted that thermal grease does not provide electrical insulation.

10.5.6.3 Elastomers. Elastomers are electrically insulating materials, usually in the form of silicone rubber pads, ranging in thickness from 0.001 to 0.20 in and filled with high thermal conductivity materials such as boron nitride and alumina. They are easier to handle than the thermal grease, but they require a higher mechanical pressure to completely fill the voids. Figure 10.65 shows how the thermal impedance of an elastomeric pad varies with applied pressure. Depending on their formulation, elastomers have thermal conductivities in the range of 1 to 6 W/m-K. Typical pressures used in device attachment to heat sinks and circuit card assemblies range from as low as 10 psi to over 400 psi. The use of excessive pressure can create detrimental stresses. For example, delicate leads and solder joints can be broken as a result of excessive pressure. While resilient, these elastomers have a fixed amount of material, which limits the minimum bond thickness. As a result, the thermal resistance of elastomers used as a gap filler is higher.

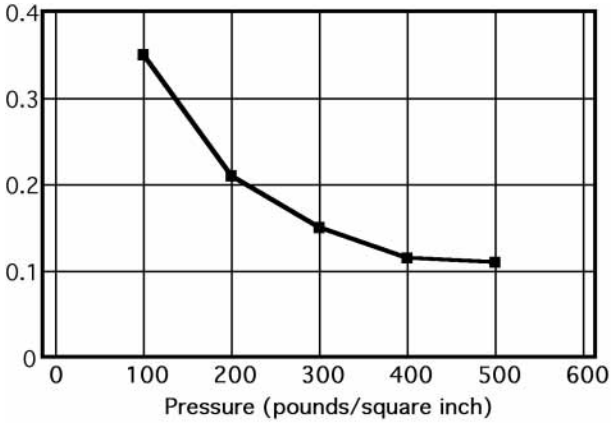


Figure 10.65 Thermal resistance vs. pressure for an elastomer pad.

When there is a large space in the thermal path, a special elastomer called a *gap filler* is used for filling it and lowering the thermal resistance. This material ranges in thickness from 0.02 to >0.20 in. The thermal conductivity is in the order of 3 W/m-K. A special feature of gap fillers is their elasticity, which allows them to return to their original thickness when the pressure is released. This is useful in the manufacturing process and facilitates rework. Because of their high elasticity, gap fillers eliminate stresses in mounting.[102]

10.5.6.4 Thermally conductive adhesives. Thermally conductive adhesives may be filled with high-thermal-conductivity materials such as boron nitride, ceramic, or CVD diamond and provide adhesion between the package and the heat sink. These adhesives may be electrically conducting or insulating, depending on the application. Table 10.20 lists some thermally conductive adhesives used for device attachment to heat sinks and circuit card assemblies. The selection of the adhesive depends on its thermal conductivity, its electrical insulation if required, its thickness, and its curing profile. The use of an adhesive with a high temperature cure, i.e., greater than 150°C, may cause damage to the circuit card or to other components. The goal in using an adhesive to attach the heat sink is to have as thin a bond line as possible so that the lowest overall thermal resistance is obtained. These adhesives are available as one of two types: liquid (paste) or in a preform (tape or precut sheet). The latter can be as thin as 0.003 in, and the liquid types can be applied as thin as 0.001 in. Liquid materials can provide the lowest bond line thickness, but they may be difficult to control. The thickness for the tape, while always greater than the liquid's, is fixed.[29,30,103]

10.5.6.5 Phase-change materials. Phase-change materials are compounds that are coated onto carrier materials or substrates, both electrical insulating and conductive, and then placed between the heat-producing part and the heat sink or circuit card assembly. The materials are placed under pressure and subsequently heated externally or self-heated to the material's melting temperature, at which they soften and fill all of the interstitial voids between the parts and the heat sink. Figure 10.66 shows the relationship of device temperature versus time when phase-change materials are used. When the part is turned on for the first time, the initial thermal resistance of the phase-change material is high, allowing the part to self-heat briefly to a higher-than-normal operating temperature. This changes the phase change material from a solid to a flowable form at which it wets the interface between the part and the heat sink (or circuit card assembly) and fills all of the voids. After wetting, the part returns to normal operating temperature, and the phase change material returns to a solid state.

The chemical composition of the phase change material determines its melting point. Materials with phase change temperatures as low as 48°C and as high as 130°C are commercially available. The thermal conductivity of the phase change compound itself is in the range of 2 to 4 W/m-K. The overall

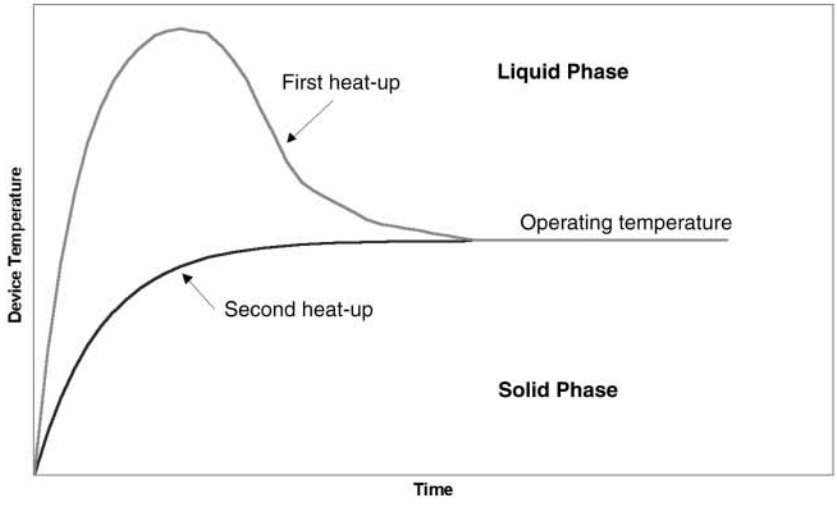


Figure 10.66 Time and temperature relationship for phase-change interface material.

thermal conductivity of the phase change material and its carrier material is highly dependent on the thermal conductivity of the carrier material. When the carrier is fiberglass or polyimide (K = 0.15 W/m-K), the thermal conductivity is low (2.7 W/m-K). The effective thermal conductivity of the aluminum-based phase change material is 112 W/m-K for a 0.002-in carrier.

Phase-change materials come in sheets or precut to sizes that range from 0.002 to 0.020 in thick. The dielectric strength of phase change materials depends on the thickness of the carrier material. When a 0.001-in thick polyimide carrier is used, its dielectric strength is 3900 V.[29,30]

10.5.6.6 Mica. Mica insulators have been used for many years for mounting power devices to heat sinks. Having a typical thickness of 0.002 to 0.003 in, they provide, in conjunction with thermal grease, a low-cost, electrically insulating method of reducing thermal resistance caused by interfacial air gaps. As stated in Sec. 10.5.6.2, the use of thermal grease can cause solder contamination problems. Other shortcomings of mica include its brittleness and inherent low thermal conductivity of 0.75 W/m-K.[65]

10.5.6.7 Adhesive tape. Thermally conductive adhesive tapes are double-sided, pressure-sensitive adhesive films filled with ceramic powder. The adhesive is typically supported either with a carrier made from polyimide film or with aluminum foil to provide ease of handling and strength. If electrical isolation is required, polyimide is the carrier used. These adhesive tapes act in a similar fashion to elastomeric films in that they require some initial mating pressure to conform to the surface irregularities. If the gap between the surfaces is too large, the adhesive tape is unable to fill it. Once a joint is formed

with an adhesive tape, mechanical pressure is no longer required to maintain the mechanical or thermal performance of the joint. From a manufacturing standpoint, adhesive tapes, unlike liquid or preform adhesives, do not require a cure cycle.[97]

10.5.6.8 Polyimide films. Polyimide films, in conjunction with wax or grease, are often used between power dissipating devices and the heat sink. Polyimide has a low thermal conductivity but excels as a result of its high dielectric strength and toughness.

10.5.6.9 Ceramic wafers. Ceramic wafer insulators made from alumina, beryllia, and aluminum nitride provide a high-thermal-conductivity (25 to 218 W/m-K), electrically insulating material for mounting devices to heat sinks. Their typical thickness ranges from 0.015 to 0.060 in. Like mica, they are brittle and crack easily. The cost of ceramic wafer insulators is considerably higher than mica.

To limit the thermal resistance introduced by the ceramic wafer that is used as a device interface, the thickness needs to minimized. As the thickness of the interface material is increased, the voltage breakdown is also increased. Therefore, a trade-off between thermal resistance and voltage breakdown needs to be made. The voltage breakdown of the ceramics used for device interfacing is extremely high as shown in Table 10.21.

TABLE 10.21 Voltage Breakdown of Ceramics Used for Thermal Interfaces[5]

Material	Voltage breakdown (V/0.001 in)
Alumina	600
Beryllia	475
Aluminum nitride	600
LTCC	1000

10.5.6.10 Underfill. To reduce the stress in the attachment of BGAs and flip-chips to circuit cards, an organic material called *underfill* is typically injected between the substrate/die and the circuit card. Underfill material is composed of thermoset polymers and silica fillers. To match the CTE of a solder joint, which is 25 ppm/°C for eutectic solder (Sn 63), an underfill composition with approximately 65 percent silica filler is required. The underfill material has several purposes. It provides good adhesion between the substrate/die and the circuit card, absorbs the stresses between them, and provides some improvement in the thermal path. As noted earlier in this section on interface materials, air has an extremely poor thermal conductivity. Filling the air gap

between the device and the circuit card with a material having a higher thermal conductivity reduces the effective thermal resistance.[84,104] The thermal conductivity of underfill ranges from 0.25 to 1.1 W/m-K.

10.5.6.11 Polymeric composite material (fiber). A new thermal interface material, consisting of high-conductivity fibers combined with a wetting agent, is available from one supplier under the trademark GELVERT.[100] The thermal conductivity of this material is extremely high for interface materials—30 W/m-K. It fills in gaps as large as 0.03 inch under pressures ranging from 1 to 5 psi.

10.5.7 Printed wiring boards

Printed wiring boards (PWBs), also known as printed circuit cards, are used for two key purposes in electronic packaging: interconnection and heat transfer. Almost all electronic components are attached to circuit cards that can be grouped into two categories: rigid and flexible. The most common type of circuit card is the rigid PCB, which is fabricated with copper-clad dielectric materials. These dielectrics consist of a resin that is reinforced with a base fabric. The materials used for the fabric include epoxy-glass (e-glass), S2-glass, quartz, and Aramid fiber. The more commonly known name for Aramid fiber is Kevlar, a trade name of DuPont. Epoxy-glass is the most widely used fabric in PCB applications. The most common resins used are G-10 and FR-4. These resins have a glass transition temperature, T_g, in the range of 105 to 125°C. Polyimides are used as the resin when glass transition temperatures over 200°C are required. As shown in Table 10.14, polyimide resins also have lower CTEs than the epoxy glass resins.[105]

Rigid PCBs are available in a variety of configurations, including single-sided, double-sided, and multilayer. From a thermal management standpoint, the single-sided and double-sided PCBs can be grouped together. Their thermal resistance is directly proportional to the thermal conductivity of the resin material and the thickness of the resin. Table 10.14 lists the thermal conductivities of various PCB dielectric materials. Overall, these dielectrics have a poor thermal conductivity. In the multilayer PCBs, the designer typically uses power and ground planes. Made from layers of copper, these planes serve not only to provide low electrical impedance but also act as heat spreaders. The copper metallization can be as thin as 0.00017 in (1/8 oz/ft^2). As the copper is made thicker, the amount of heat spreading is increased. Some circuit card manufacturers use copper as thick as 0.0067 in (5 oz/ft^2).[106]

In some applications, the printed circuit board is attached to a metal core. This is done for two purposes: heat transfer and to restrain the CTE. For heat transfer, materials with high thermal conductivities, such as aluminum, copper, and various composites, are used. The thermal conductivities of various materials used for printed circuit card cards are listed in Tables 10.14 and 10.18. (Note that some of the same materials used for package bases are also used as cores for circuit cards.) The heat conducts from the component, through any interface material, and through the circuit card into the metal

core. The core then conducts the heat to the card rails. Figure 10.67 shows the construction of a circuit card with a metal core.

Printed circuit cards typically have CTEs in the range of 15 to 20 ppm/°C. When leadless devices such as ceramic ball grid arrays and ceramic chip carriers are used, the CTE of the printed circuit card needs to be reduced so that it is close to CTE of the component package and therefore does not lead to attachment failures. Placing a metal core with a low CTE between two circuit cards, as shown in Fig. 10.67, has the effect of constraining the effective CTE to that of the core. Although aluminum and copper have high thermal conductivities, they also have high CTEs. Therefore, they cannot be used for constraining the CTE. Composite and clad materials such as copper-graphite, aluminum-graphite, copper-Invar-copper, copper-molybdenum, and aluminum-silicon-carbide are used for circuit card cores. These materials offer both low CTE and high thermal conductivity.

Several PCB dielectric materials are suited for very high-frequency operation, typically above 1 GHz, because of their low dielectric constant and their loss tangents. For cost considerations, some manufacturers use a combination of classical dielectrics with the microwave dielectric materials. For thermal modeling of these composite materials, the thermal analyst needs to use Eq. (10.26).

10.5.7.1 Through-hole thermal vias. Another method to improve the thermal conductivity of the PCB is to use thermal vias under the high-power devices as shown in Fig. 10.68. These thermal vias are different from their ceramic coun-

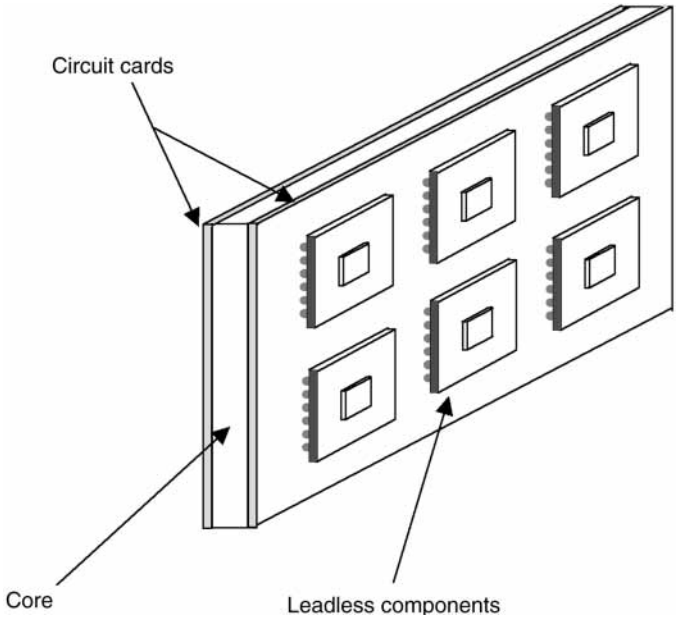


Figure 10.67 Construction of a circuit card with a metal core and the heat flow.

terparts in that the circuit card vias are usually through holes; i.e., the vias go from the top of the card to the bottom. The walls of the vias are typically copper plated as shown in Fig. 10.69. The heat is conducted primarily in the copper plating on the wall of the vias. In some advanced circuit cards with blind and buried signal vias, the thermal via is a series of stacked, filled vias as shown in Fig. 10.70.

Assume that a heat dissipating device is mounted on an FR-4 board, which in turn is mounted on a heat sink as shown in Fig. 10.71. Using superposition, the thermal resistance of the board without thermal vias under the heat dissipating device is calculated first as follows:

$$\theta_{board} = \frac{t}{K_{\text{board}} A_{\text{pkg}}} = \frac{t}{K_{\text{board}} LW} \tag{10.30}$$

where θ_{board} = thermal resistance of the board under the heat dissipating device

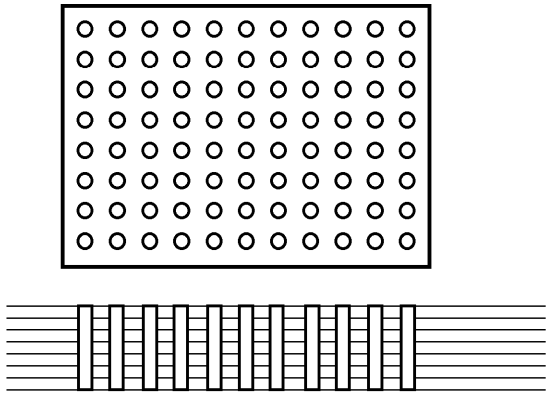


Figure 10.68 Through-hole via array.

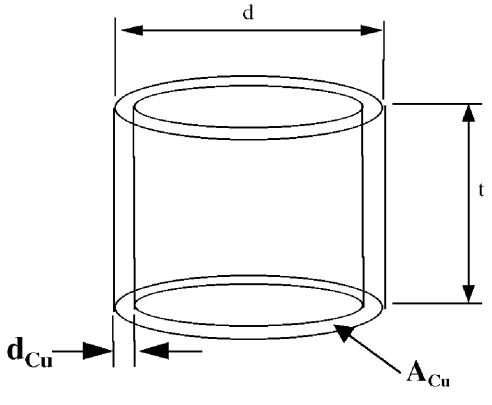


Figure 10.69 Expanded view of through-hole via.

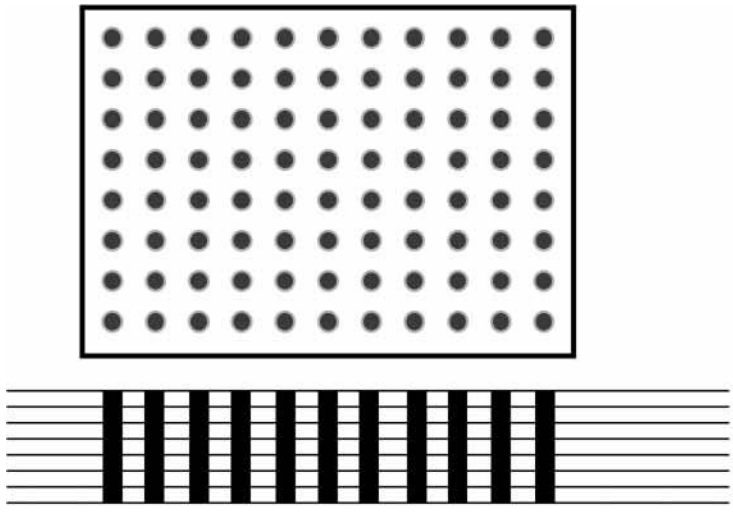


Figure 10.70 Stacked, filled vias in PCB.

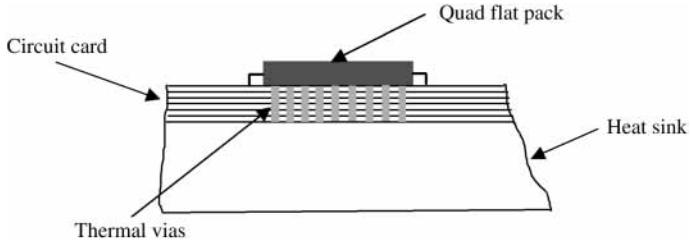


Figure 10.71 Surface mounted QFP on a circuit card with thermal vias mounted on a heat sink.

t = thickness of the board
K = thermal conductivity of the board
A_{pkg} = area of the heat dissipating device = L × W

The thermal resistance of the thermal vias is calculated next. For one unfilled via, its thermal resistance is

$$\theta_{via} = \frac{t}{K_{via} A_{via}} \tag{10.31}$$

where θ_{via} = thermal resistance of the via
t = thickness of the board
A_{via} = cross-sectional area of the via
K_{via} = thermal conductivity of the via

The via's cross-sectional area, shown as A_{cu} in Fig. 10.69, is the area of the copper that conducts the heat. This heat-conducting portion of the via is calculated using Eq. (10.32).

$$A_{\text{Cu}} = \pi\left(\frac{d}{2} - \left(\frac{d}{2} - d_{\text{Cu}}\right)\right)^2 \tag{10.32}$$

where d_{Cu} = thickness of the copper in the via
d = diameter of via

No heat is conducted through the air in the center of an unfilled via. As the thickness of the plating is increased, the thermal conductivity from the board, top to bottom, is also increased.

Because there are n thermal vias in parallel, Eq. (10.31) for the total via thermal resistance θ_{nv} becomes

$$\theta_{nv} = \frac{t}{nK_{\text{via}}A_{\text{via}}} \tag{10.33}$$

The n vias (unfilled) under the heat dissipating device are in parallel with the board material's heat path. Having calculated the thermal resistances of the board alone, and the vias, the equivalent thermal resistance can be looked at as a parallel circuit, shown in Fig. 10.72, whose equivalent thermal resistance is

$$\theta_{\text{equiv}} = \frac{\theta_{\text{board}}\theta_{nv}}{\theta_{\text{board}} + \theta_{nv}} \tag{10.34}$$

It is obvious from Eq. (10.33) that the thermal resistance in the board can be lowered if the number of vias is increased. This approaches a limit imposed by circuit card manufacturers on the via-to-via spacing of through holes.

Ideally, one would like to fill the vias with a high-thermal-conductivity material such as copper to further lower the thermal resistance. However, due to processing concerns, minimum-sized through holes (0.019 in, typically) cannot

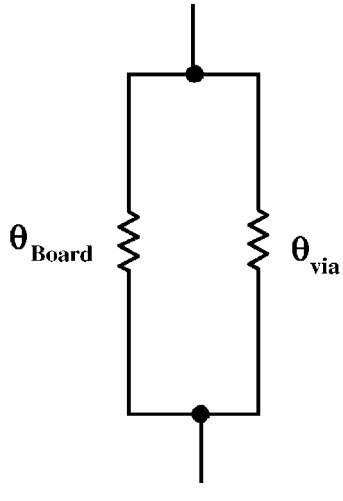


Figure 10.72 Electrical analog of thermal vias in PCB.

be filled with copper plating. Instead, materials such as solder and conductive epoxy are used for filling thermal vias. For filled vias, the electrical analog for the circuit would have three thermal resistances in parallel as shown in Fig. 10.73: the board material, the copper wall, and the fill material. If the vias were filled, then the thermal resistance would be lowered.

The thermal resistance of the via fill material is

$$\theta_{\text{via-fill}} = \frac{t}{nK_{\text{via-fill}}A_{\text{via-fill}}} \tag{10.35}$$

where $A_{\text{via-fill}} = \pi(d - d_{Cu})^2$

The equivalent thermal resistance for the filled vias is

$$\frac{1}{\theta_{\text{equiv}}} = \frac{1}{\theta_{\text{board}}} + \frac{1}{\theta_{\text{via-fill}}} + \frac{1}{\theta_{nv}} \tag{10.36}$$

Thermal via example An array of 121 vias, 0.019 in diameter with 0.001-in copper plating in a 0.060-in thick FR-4 board, is placed under a device whose dimensions are 0.300×0.300 in. The vias are filled with Sn 63 solder. It is necessary to find the equivalent thermal resistance of the board, the vias, and the via fill.

The thermal conductivities (in W/m-°C) of the various materials are[3]

- FR-4 0.35
- Sn 63 50.9
- Copper 396.9

The thermal resistance of the FR-4 board without vias is

$$\theta_{\text{board}} = \frac{t}{K_{\text{board}}A_{\text{pkg}}} = \frac{0.060}{0.35 \times 0.0254 \times 0.3 \times 0.3} = 75°\text{C/W}$$

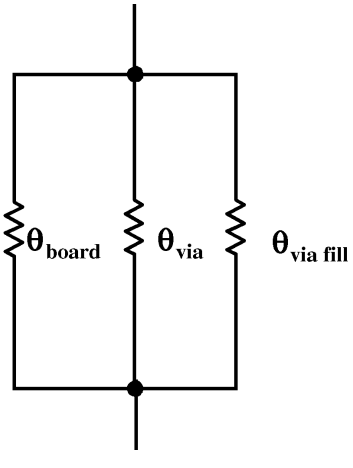


Figure 10.73 Electrical analog of filled thermal vias in PCB.

The thermal resistance of the via fill for n vias is

$$\theta_{\text{via-fill}} = \frac{t}{nK_{\text{via-fill}}A_{\text{via-fill}}}$$

$$= \frac{0.060}{121 \times 50.9 \times 0.0254 \times \pi\left(\frac{0.019}{2} - 0.001\right)^2} = 1.690°\text{C/W}$$

The thermal resistance of the copper-plated via walls is

$$\theta_{nv} = \frac{t}{nK_{\text{via-fill}}A_{\text{via-fill}}} = \frac{0.060}{121 \times 396.9 \times 0.0254 \times \pi\left(\frac{d}{2} - \left(\frac{d}{2} - d_{Cu}\right)\right)^2}$$

$$= 15.66°\text{C/W}$$

The equivalent thermal resistance of the board, the vias, and the via fill is calculated using the electrical analogy for parallel circuits from Eq. (10.36).

$$\frac{1}{\theta_{\text{equiv}}} = \frac{1}{\theta_{\text{board}}} + \frac{1}{\theta_{\text{via-fill}}} + \frac{1}{\theta_{nv}} = \frac{1}{75} + \frac{1}{1.690} + \frac{1}{15.66} = 1.49°\text{C/W}$$

By using solder-filled thermal vias, the thermal resistance of the board under the heat dissipating device was reduced from 75 to 1.49°C/W.

10.5.7.2 Microvias (build-up technology). In high-density printed circuit boards, blind and buried vias are used to connect two layers of circuitry. Fabricated by nonmechanical means, the diameters of microvias can be as small as 0.002 in. Multilayer circuits using this technique are built up one layer at a time and have been given the name of *built-up multilayer.*

Cross sections of metallized microvias formed by various techniques are shown in Fig. 10.74. The walls on each of the vias are plated copper. For thermal modeling, the equations in Sec. 10.5.3.9, developed for through-hole vias, can be used with the dimensions adapted for microvia technology.[105]

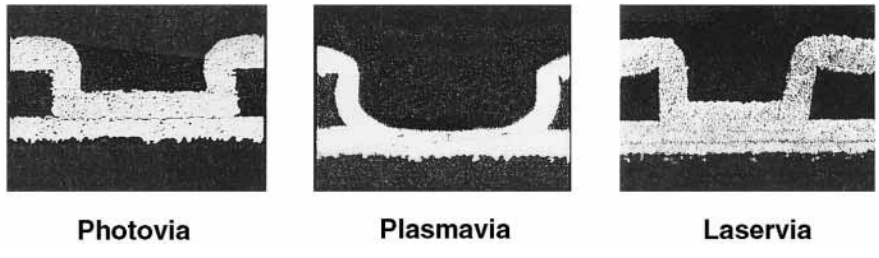


Figure 10.74 Metallized microvia cross section.

10.5.7.3 Direct chip attach to heat sink. Another technique for reducing the thermal resistance under a device is to mount it directly on the heat sink through a cutout in the circuit card as shown in Fig. 10.75. This technique completely eliminates the thermal resistance of the board. It works for direct chip attach (DCA) and packaged components as long as the back of the chip in DCA or the package bottom is not connected to any potential. If the back side of the chip were connected to a nonground potential, then a thin electrically-insulating layer of epoxy or other polymer would be required.[5]

10.5.8 Flexible PCBs

Flexible PCBs consist of ductile, patterned copper foil bonded to thin, flexible dielectric material. They are used in applications in which periodic movement of the circuit is required during circuit operation. The conductor patterns are formed in the same manner as in rigid PCBs. Vias, used for both interconnection and thermal improvement, can be the standard through-type, or they can be buried.

There are two possible conductive thermal paths in a flexible PCB: through the dielectric and through the copper foil. The dielectric material is typically a polyimide with a thermal conductivity of 0.11 W/m-K or a polyester film with thermal conductivity ranging from 0.21 to 0.87 W/m-K. Standard thicknesses of polyimide dielectric layers are 0.0005, 0.001, 0.002, 0.003, and 0.005 in. Because the thermal conductivities of flexible PCB dielectrics are rather low, the main thermal path is through the copper foil.[3,105] To improve the thermal effective thermal conductivity in flexible PCBs, thermal vias can be used as described above.

10.5.9 Plating

Metal packages and substrates are typically plated with materials such as gold, nickel, copper, silver, and tin. Packages are plated to prevent corrosion, whereas substrates are plated to increase electrical conductivity and to facilitate wire bonding. Nickel is used for several reasons, including corrosion protection and as a metal barrier between the base metallization and subsequently applied solder. Although the plating thicknesses may be thin, they need to be considered in accurate thermal modeling. Table 10.22 lists the thermal conductivities of various plated metals used in microelectronic assemblies.

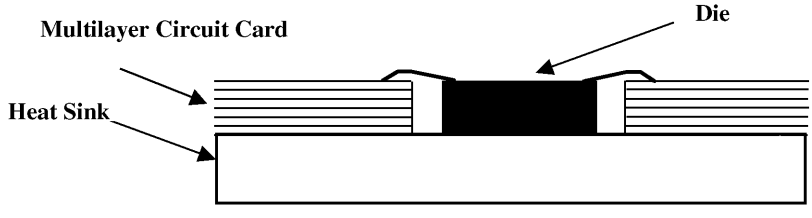


Figure 10.75 Direct die attach to heat sink.

TABLE 10.22 Thermal Conductivities of Plated Metals[65]

Material	Thermal conductivity (W/m-K) at 0°C	Thermal conductivity (W/m-K) at 100°C
Gold	319	313
Silver	429	426
Nickel	94.1	82.7
Copper	401	395
Tin	68.2	63.2

10.5.10 Gases

The thermal conductivities of gases are extremely poor. When a gas is in the thermal path, the resulting thermal resistance will be extremely high. For instance, air, consisting of 78 percent nitrogen and 21 percent oxygen, has a thermal conductivity of 0.0253 W/m-K at sea level. This is approximately 100 times less than the thermal conductivity of epoxies. The thermal conductivity of air varies with altitude as shown in Fig. 10.76.[65]

As shown in Table 10.23, a gas such as helium has a thermal conductivity approximately six times that of air/nitrogen and can provide some additional

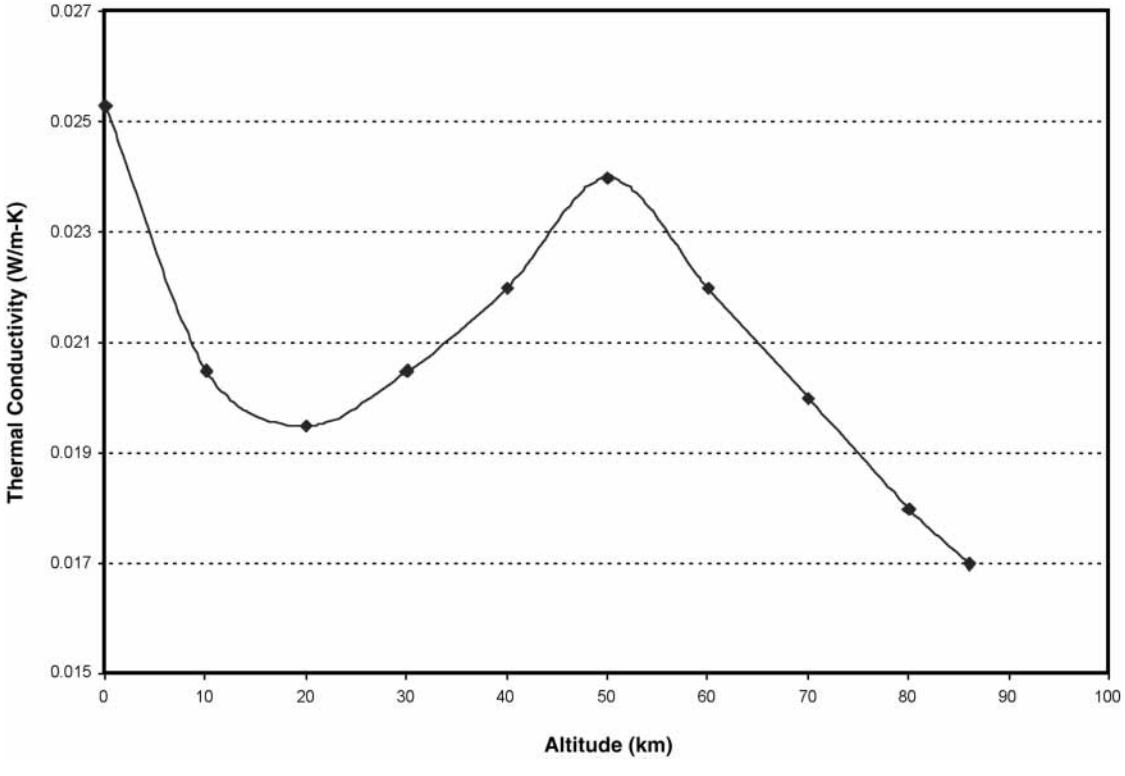


Figure 10.76 Thermal conductivity of air at various altitudes.

TABLE 10.23 Thermal Conductivity of Gases at 1 Atm, in W/m-K *(from Ref. 65)*

Gas	0°C	100°C
Air	0.0024	0.0031
Argon	0.0016	0.021
Carbon dioxide	0.00137	0.0023
Helium	0.0141	0.017
Hydrogen	0.016	0.021
Nitrogen	0.0024	0.0031
Oxygen	0.0024	0.0032

cooling. IBM has used helium as a backfill for its Thermal Conduction Module.[24,65]

10.6 Factors Determining Thermal Resistance

A myriad of physical factors determine the thermal resistance of a semiconductor in an electronic system. All of these factors were captured in Eq. (10.9), which is repeated here.

$$\theta = \frac{X}{KA}$$

Figure 10.77 depicts a chip mounted on a substrate, which in turn is attached to a package. This package is bonded to the printed wiring board with a thermal interface material.

10.6.1 Semiconductor dimensions

The heat in an electronic system is generated in the semiconductor junction, and the junction area "A" in Eq. (10.9) is a key factor in determining the thermal resistance. It is relatively easy to determine the junction size in discrete transistors and diodes. Figure 10.78 shows a picture of a 0.200-in square junction transistor die wherein the junction size can be approximated by the guard ring as 0.160×0.160 in. Heat is not generated across the entire transistor die.

For the voltage regulator die shown in Fig. 10.79, there is a high-power transistor occupying approximately half of the die. Although the low power section dissipates a small amount of heat, it is the power transistor that dissipates the majority of the heat. For an accurate first-order thermal analysis of this die, the junction size to use is that of the high-power transistor, approximately 0.045×0.085 in.

Power MOSFETs consist of thousands of individual transistors in parallel. For example, a 240-mil^2 MOSFET from Fairchild Semiconductor consists of approximately 25,000 transistors in parallel.[107] For the power MOSFET thermal model, the thermal analyst usually uses the entire chip area as the junction area.

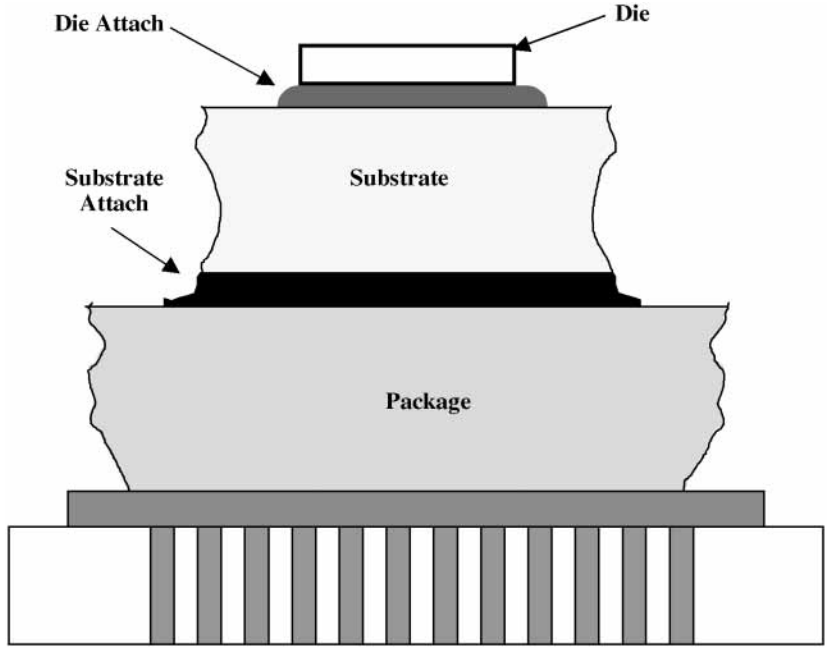


Figure 10.77 Cross-sectional view of packaged die.

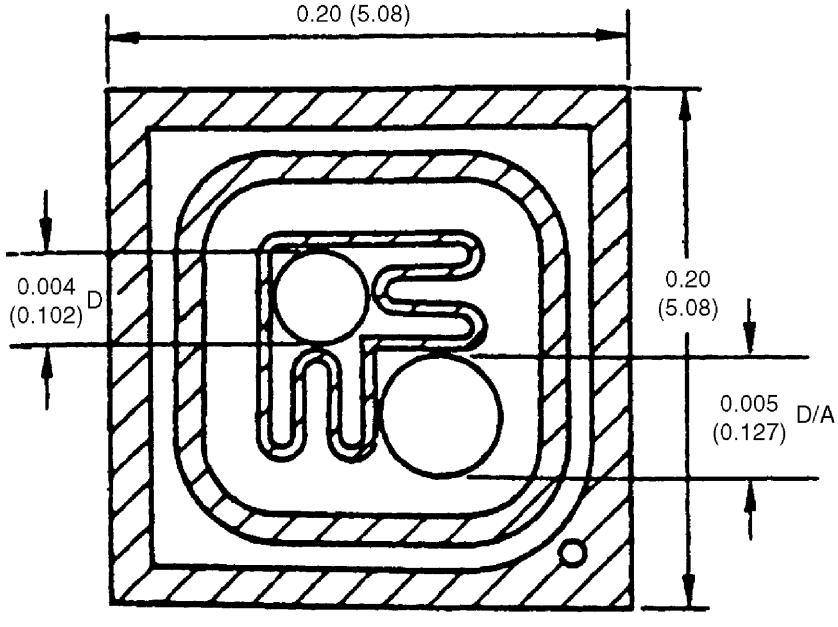


Figure 10.78 Die topography of junction transistor.

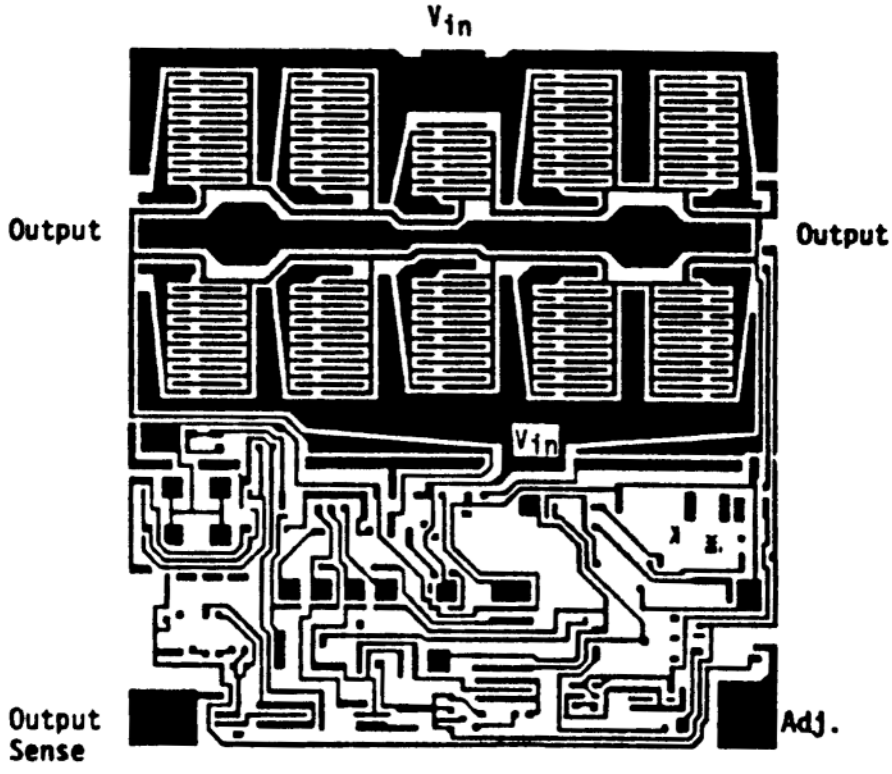


Figure 10.79 Die topography of voltage regulator.

In integrated circuits, the number of junctions can range from as few as a dozen to the millions. When modeling integrated circuits, the thermal analyst usually looks at the entire die as the junction area. However, the analyst may take into account that there are no junctions under the wire bond pads and subtract out that small amount of area. If the integrated circuit has high-current drivers, then the thermal model should be broken down into the low-power section(s) and the high-power driver section(s).

The thickness of the die "X" is an important factor in determining thermal resistance. As wafer sizes have grown from 3- and 4-in diameters to 12-in ones, the thickness has also increased from 0.015 to 0.030 in. Figure 10.80 shows the various wafer thicknesses for different diameters.[108] Many semiconductor foundries thin their wafers down, either with mechanical or chemical methods, mostly to allow the chips to fit into their packages. However, some chip manufacturers use the thinning process to reduce the thermal resistance.

The majority of semiconductors are fabricated from silicon, which has a thermal conductivity of 150 W/m-K (at 25°C). For high-frequency applications, typically starting at 1 GHz, gallium arsenide is used as the semiconductor material. Other materials used include indium phosphide, silicon carbide, gallium phosphide, gallium antimony, indium arsenide, and indium antimony. Because of the substance's lower thermal conductivity (45 W/m-K), gallium ar-

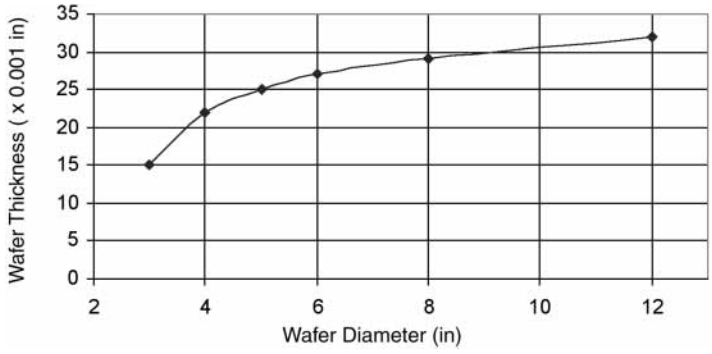


Figure 10.80 Wafer thickness vs. wafer diameter.

senide chips are routinely thinned down to lower the thermal resistance. Gallium arsenide chips are also thinned to reduce the impedance of through-hole vias from the top to the bottom of the chip. Typical thicknesses of gallium arsenide used in the microelectronic assemblies are 0.002 and 0.006 in.

10.6.2 Die attach material and thickness

In most packaging applications, the semiconductor die needs to be attached to the next level of packaging with die attach material on the back side of the chip. The thermal conductivity of this adhesive material is usually the most important factor in determining thermal resistance. The die attach material is typically chosen for both manufacturability and thermal performance. Organic materials such as epoxy are used because of their ease of application and, in some cases, ease of rework. Epoxies, however, have very low thermal conductivities, typically in the range of 1 to 2 W/m-K as detailed in Table 10.7. Solder materials, such as gold-tin and lead-tin, offer considerably higher thermal conductivity, typically in the range of 40 to 60 W/m-K, but at the expense of manufacturability. An alternative material for die attach, silver glass, with a thermal conductivity of 60 to 80 W/m-K, offers many of the advantages of both the organic materials and the solders.

For any die attach material selected, the second most important factor determining thermal resistance is the die attach bond line. As defined in Eq. (10.9), the thermal resistance of the die attach is directly proportional to the thickness "X." The goal is to minimize the die attach thickness and maintain sufficient strength so that the die does not come off during its application. The uniformity of the die attach material is also an important factor in determining thermal resistance. If the die attach bond line had a variation in it, then a mean thickness would be used in that layer's thermal resistance calculation. An extremely thick die attach bond line can result in hot spots on the die. A condition worse than an extremely thick die attach is the presence of voids. Mathematically, voids reduce the effective cross-sectional area of the die attach. For the X-ray of the die attach shown in Fig. 10.81, there is approximately 10 percent voiding. This can be modeled as shown in Eq. (10.37), where the area term "A" is reduced by the percentage voiding "V."

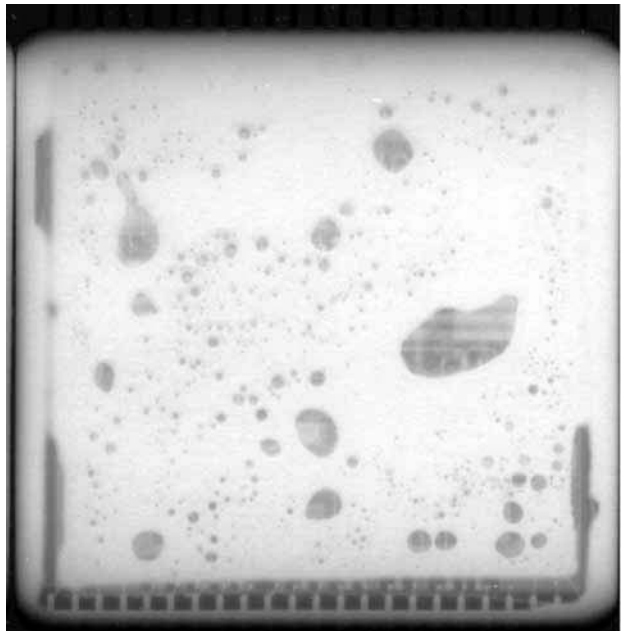


Figure 10.81 X-ray of hybrid substrate attach.

$$\theta = \frac{t}{K(1 - VxA)} = \frac{t}{K(0.9A)} \tag{10.37}$$

10.6.3 Substrate material and thickness

When a substrate is used in the packaging, there are two key parameters in determining thermal resistance. The thermal conductivity of the material is the most important parameter. The second most important parameter is the substrate thickness. Ninety-six percent alumina with single-layer metallization has a thermal conductivity of 21 W/m-K. The same alumina with five thick film dielectric layers has an effective thermal conductivity in the z-direction of only 15.9 W/m-K. High-power applications typically use beryllium oxide as a substrate. Its thermal conductivity is 248 W/m-K. This is an improvement of 8 times over 96 percent alumina. With five layers of dielectric, beryllium oxide has an effective thermal conductivity in the z-direction of 178 W/m-K. Aluminum nitride, with a thermal conductivity of 170 W/m-K, is also used as a substrate in high power applications.

The presence of thermal vias in the substrate can produce significant improvement in the effective thermal conductivity. For example, the 951 LTCC substrate material from DuPont has a published thermal conductivity of 3.0 W/m-K.[35] The same material with an array of gold-filled thermal vias (0.006-in diameter, 0.018-in pitch) has a thermal conductivity of 24.56 W/m-K.[41] The maximum via diameter and pitch are determined for each substrate type by the manufacturer. Exceeding these values can cause substrate warping or

cracking as a result of the higher CTE of the via fill as compared to dielectric material.

The thickness of the substrate dielectric material is an important factor in determining the thermal resistance. Thick-film glass has a thermal conductivity of 3.0 W/m-K.[35] This is only 10 percent of the thermal conductivity of 96 percent alumina. Substrate manufacturers typically use two to four printings[109] of dielectric between each metallization layer. The fired thickness of each dielectric printing is typically 12 to 14 μm. These multiple layers are used to prevent pinholes in the dielectric that lead to shorting between layers. With additional printings of dielectric, the dielectric layer becomes thicker, and the thermal resistance of that layer becomes higher.

Often, power or ground planes are used in multilayer substrates. These planes are typically solid metal or in grid form. In addition to providing low electrical resistance, they also serve the purpose of heat spreading.

10.6.4 Substrate attach material and thickness

When substrates are used, they must be attached to the package with either solder or some organic adhesive material. The same parameters that determine thermal resistance for the die attach material, thermal conductivity and thickness, apply for the substrate attach. If organics are used for the substrate attach, the thermal resistance will be significantly higher than if a solder were used.

10.6.5 Package material

As described in Sec. 10.5.5, semiconductor packages can be divided into two types: hermetic and nonhermetic. The key parameters for both package types in determining thermal resistance are the thermal conductivity and material thickness of the base material. The best thermal conductivity material used for package bases is copper, with a value of 397 W/m-K. On the opposite end of the thermal conductivity spectrum is LTCC, with a value of 3.0 W/m-K.[12] As described in Eq. (10.9), the thinner the material, the lower the value of thermal resistance. However, as the material becomes too thin, the structural integrity of the package is compromised. During environmental screening or during operation in severe environments, a thin package base can deflect and cause cracking of semiconductors and substrates.

The nonhermetic, plastic encapsulated semiconductor package comes in several variations. The majority of these package types have plastic molding compound under the die as shown in Fig. 10.36. This material typically has very low thermal conductivity of 0.5 to 1.0 W/m-K. To lower the thermal resistance of plastic packages, some manufacturers use an exposed metal pad on the back side of the package. This exposed pad, usually part of the lead frame, is called an *exposed paddle*. When made from copper, this paddle provides a low thermal path from the die to the circuit card and provides excellent heat spreading. When the paddle is exposed and fabricated with Alloy 42 with a thermal conductivity of 15.9 W/m-K,[24] there is a significant thermal conductivity improvement over packages made with plastic bottoms.

10.6.6 Package interface

The physical designer may have used all of the materials and processes in packaging the semiconductor to achieve the lowest thermal resistance, but may have added significant thermal resistance in attaching the device to the circuit card or the heat sink. A noted in Sec. 10.5.9, air, with its low 0.025 W/m-K thermal conductivity, must be eliminated, or at least minimized, from the thermal path. This requires the attachment of the package to the circuit card or heat sink with a thermally conductive material that fills the gaps between the package and the circuit card or heat sink. If the material is too thick, then the thermal resistance increases linearly. If too thin, there may be air gaps and higher thermal resistance. The various materials used to fill the gaps have been described in Sec. 10.5.6. Many of these materials, such as the adhesives and gap pads, have thermal conductivities in the range of 0.6 to 6.0 W/m-K. At the upper end of the thermal conductivity range for the package interface materials is the solder perform. For example, Sn 63 solder has a thermal conductivity of 51 W/m-K. As discussed in Sec. 10.5.6, the thermal conductivity of many of the interface materials is a function of the pressure applied. Using an incorrect pressure, or a pressure that can significantly vary, will cause variations in the thermal resistance.

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