SECTION 6

INTEGRATED CIRCUITS AND MICROPROCESSORS

Digital and analog integrated circuits are the fundamental building blocks of today's electronic systems, digital ICs being dominant. They can emulate many functions for which analog circuitry was previously required. Nevertheless, because the real world is largely analog in nature, the analog IC remains the primary interface.

The extraordinary rate of progress in making dynamic random-access memories (DRAM) smaller and more powerful is reflected in their wide use, and, for example, in the rapid obsolescence of lesser-performing computer models.

The microprocessor, over its 30-some-year life span, has become a powerful tool for the design engineer, who embeds it in a broad range of intelligent digital devices.

Finally, Chap. 6.5 in this section covers nanotechnologies. The rapid developments in nanofabrication techniques have spawned a new era in microcomponent developments, including microelectromechanical components (see Chap. 8.5). C.A.

In This Section:

CHAPTER 6.1
DIGITAL INTEGRATED CIRCUITS*

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INTRODUCTION

This and the following two sections will discuss the design and application of two major classes of integrated circuits (ICs): digital and analog and their application to both memory and logic circuits, which are shown for both bipolar and complementary MOS (CMOS) technologies.

Digital circuits are the most widespread and commonly used integrated circuits today. They process signals in binary bits. They are distinguished by their function and their performance. Analog circuits are less common and process signals as waveforms.

Analog circuits play a critical role intrinsic to the connection of electronic systems to the physical world and analog electronics have a rich and long history. More recently, digital electronics have become sufficiently sophisticated that computations on numerical values (representing the value of analog signals at regularly spaced intervals in time) can often be used to perform several traditional signal processing functions that previously required analog circuits. This transition of several traditional analog circuit functions into the digital world has accelerated, providing the capability of "programming" the digital computations to perform different traditional analog circuit functions or "reconfiguring" the digital components of an integrated circuit to change the operations performed. However, the analog circuits usually are required for the interface between the physical world (where things are usually analog) and the digital world. The combination of both analog and digital circuitry on the same VLSI circuit has allowed a wide range of applications to develop. Such "mixed signal" ICs are seen in various "embedded systems" such as those used in automobiles (sensors and computers measuring and controlling ignitions, and so forth).

In this section, the basic parameters used to measure the performance of digital circuits are first introduced. This is followed by a description of the different digital integrated circuit technologies, and their function in systems.

Logic Performance Parameters

Although there are a wide variety of parameters of interest, such as environmental, operating speed, voltage range, availability and cost, five key parameters are generally used in comparing digital circuit families.

Speed

This indicates how fast a digital circuit can operate. It is usually specified in terms of gate propagation delay, or as a maximum operating speed such as the maximum clock rate of a shift register or a flip-flop.

Gate propagation delay is defined as the time between the transition of an input signal between two states and the resulting response of the output signal.

*The contents of this chapter have been extracted and significantly updated from "Integrated Circuits" by F. F. Mazda, Butterworth, 1983.

Power Dissipation

This gives a measure of the power which the digital circuit draws from the supply. It is measured as the product of the supply voltage and the mean supply current for given operating conditions such as speed and output loading. Low power dissipation is an obvious advantage for portable equipment. However, since the amount of power which can be dissipated from an integrated circuit package is limited, the lower the dissipation, the greater the amount of circuit which can be built into a silicon die.

Speed-Power Product

The "power-delay" product is obtained by multiplying the power dissipation of a component by the delay between the input signal change and the output response. The product represents the energy associated with the functional operation of the component. The concept of power-delay product extends well beyond its use with simple devices or logic functions to larger scale systems. In general, a given component will be characterized by an energy (power-delay product) but allow trade-offs between the delay (or speed—reciprocal of the delay) and the power dissipation with the constraint that the power-delay product remain constant. This conforms to our intuitive expectation that if we are willing to accept higher power dissipation in a component we can achieve higher speed operation. Figure 6.1.1 illustrates the general theme. Here, three different circuits are characterized by different energies (i.e., representing different energies associated with different VLSI technologies) but each of these circuits can be adjusted either for high-speed operation at high-power dissipation or for low-power dissipation operation at lower speeds).

Current Source and Sink

This measures the amount of current which the digital circuit can interchange with an external load. Generally digital circuits interconnect with others of the same family and this parameter is defined as a *fan-out*, which is the number of similar gates which can be driven simultaneously from one output. The *fan-in* of a circuit is the number of its parallel inputs.

Noise Susceptibility and Generation

Digital circuits can misoperate if there is noise in the system. This may be a slowly changing noise, such as a drift in the power supplies, or high-energy spikes of noise caused by switching transients. Some types of logic

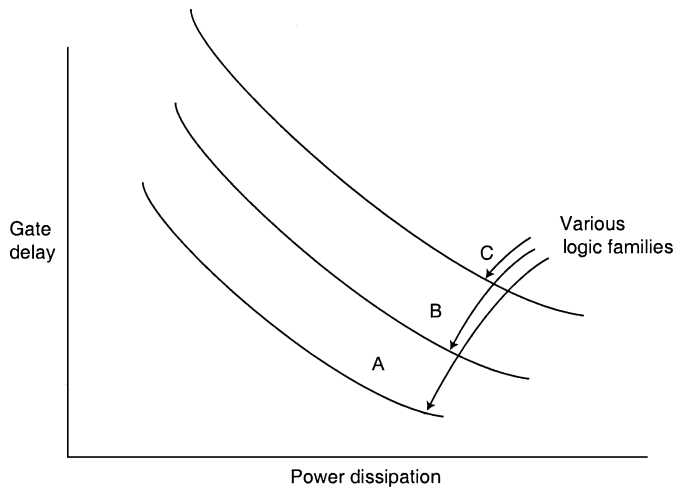


FIGURE 6.1.1 Speed vs. power curves.

families can tolerate more noise than others, and generally the faster the inherent speed of the logic, the more it is likely to be affected by transient noise.

Digital circuits also generate noise when they switch and this can affect adjacent circuits. Noise generation is a direct function of the current being switched in the circuit and the speed with which it is changed.

Comparisons of Various Digital Circuit Families

Today's advanced VLSI circuits draw upon several advantages of silicon CMOS circuits over earlier technologies. During the era of lower density digital circuits, eras of small-scale integration (SSI) and large-scale integration (LSI), bipolar circuit technologies were dominant. Fabricated vertically, small distances were more easily obtained than laterally, an advantage leading to higher performance bipolar circuits than found in MOS circuits. The table below shows the relative advantages of those earlier versions of digital technology. As the number of transistors in an IC increased and as technologies evolved to provide very small lateral distances, MOS circuits became increasingly competitive. The initial NMOS logic (using an NMOS pull-down circuit in combination with a pull-up resistor) was quickly replaced by CMOS technologies, once fabrication techniques had advanced to allow fabrication of both NMOS and PMOS transistors in the same substrate (essentially by creating "wells" deeply doped opposite to the substrate doping to create the other type of MOSFET). Today, CMOS is clearly the dominant technology and each successive generation of microfabrication technology increases the relative advantages of CMOS over the earlier bipolar forms of digital logic. Some of the principles of these earlier bipolar circuits are described later, providing an understanding of the various ways in which basic devices could be arranged to yield the basic digital functions of logic. In contrast to analog circuits which require a very linear response to input analog signals, digital logic circuits are deliberately nonlinear—switching between one state and another in response to the input signal and producing a fundamental regeneration of the binary logic states at the output of the circuit.

Comparison of Logic Families (1 = best, 6 = worst)

Logic family	Speed	Power	Fan out	Noise
DTL	4	4	3	3
TTL	3	4	3	3
ECL	1	6	2	2
NMOS	5	2	2	2
CMOS	3	1	1	1

BIPOLAR LOGIC CIRCUITS

This section discusses digital circuits using bipolar technology.

Saturating Bipolar Logic Circuits

One of the earliest digital circuit families was the resistor-transistor logic (RTL) family. Figure 6.1.2*a* shows a 3-input NAND gate. When the three transistors are OFF, R4 *pulls up* the output voltage D toward Vcc. If any of the three transistors turns ON (base voltage high), that transistor *pulls down* the output voltage toward 0 V. To provide full output voltage swings, the ON (OFF) state resistance of a transistor must be small (large) compared to R4. Diode-transistor logic (DTL), Fig. 6.1.2*b*, was another early bipolar logic technology, using pull-down diodes in combination with a pull-up resistor to drive the base of the output transistor. Replacing the multiple input resistors with simpler diodes leads to smaller gate areas. In addition, the dependence of the output resistance of the RTL circuit on inputs A to C is eliminated.

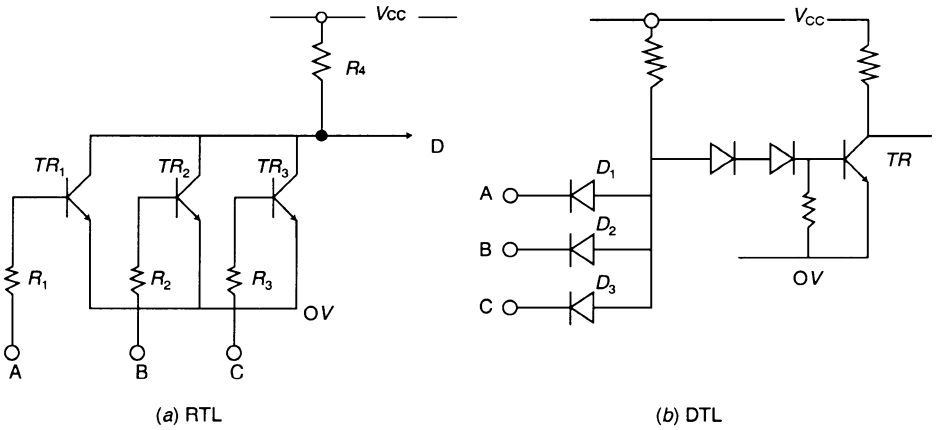


FIGURE 6.1.2 Resistor-transistor logic and diode-transistor logic.

The RTL and DTL logic families were quickly replaced by transistor-transistor logic (TTL) (Fig. 6.1.3), further simplifying the input configuration (here three emitters placed in the same transistor structure) while adding an active pull-up transistor TR1 in combination with the pull-down transistor to achieve faster outputs. The TTL logic family developed into a variety of subfamilies, each optimized for different performance objectives and remained the mainstream digital logic technology through the evolution from SSI through MSI to LSI. The increasing number of gates per IC required a decrease in power dissipation per gate to avoid a concurrent increase in the power dissipation of the IC. This limited the extension of the TTL logic family into VLSI since the TTL gate's power dissipation could not be decreased sufficiently. CMOS technologies have replaced TTL as the mainstream logic technology in VLSI. However, the TTL circuits continue to see use in BiCMOS, a technology that combines CMOS circuits with bipolar circuits on the same IC to achieve speed and current drive advantages as needed.

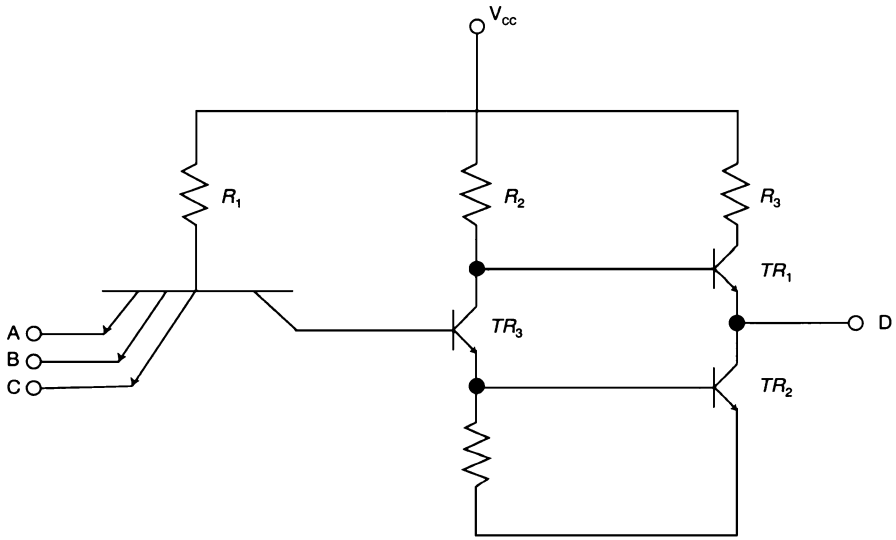


FIGURE 6.1.3 Transistor-transistor logic gate.

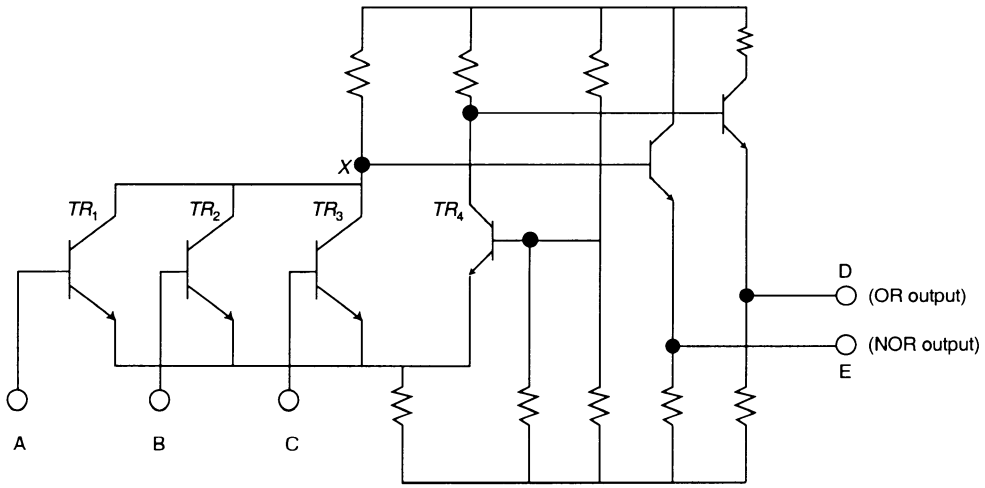


FIGURE 6.1.4 Emitter-coupled logic gate.

Nonsaturating Bipolar Logic Circuits

When in the saturated ON state, an excess charge density appears within the bipolar transistors. Switching the transistor to the OFF state requires that this excess charge density be removed, limiting the speed of the gates. One method to reduce the charge storage delays is to use Schottky transistors in the TTL gate. The Schottky diode prevents the transistor from saturating, leading to faster switching times. Such Schottky TTL logic circuits, either in low-power versions or high-speed versions, generally replaced the saturating TTL circuits discussed earlier.

Another nonsaturating bipolar logic family was the standard when high speed was a priority. This is the emitter-coupled logic (ECL) family (Fig. 6.1.4) in which separate transistors for each input and optimized designs for the highest possible speed are used. The amplifier consisting of TR4 and the input transistors drives the output transistors providing both noninverted and inverted outputs. The output transistors are designed with low resistance, providing high output current drive and high speed. Current flow into the gate from the power supply is nearly constant, avoiding noise problems seen in other bipolar logic circuits. The ECL logic circuits used supply voltages different from TTL logic and also had smaller output voltage swings, making connection of TTL logic and ECL logic difficult to interface (special interface circuits were available).

MOS LOGIC CIRCUITS

MOS technologies emerged early in the history of digital logic but suffered from poor performance because of the device structures being fabricated as lateral structures (with larger distances) in contrast to the bipolar device structures which took advantaged of small distances achieved with vertical structures. As device dimensions decreased, this disadvantage also decreased, with MOS device performance improving with each scaling to smaller device sizes. Initial MOS logic circuits used either NMOS or PMOS transistors (Figs. 6.1.5 and 6.1.6), a fabrication constraint since these different transistors used different type substrates (P-type and N-type, respectively).

Figure 6.1.7 shows a basic three input NMOS gate as the pull-up circuit and a resistor used as the pull-down element. That pull-down resistor is realized as a transistor in the ON-state to achieve a small area resistor. The symbol for the MOS transistor directly illustrates one feature that provides a fundamental advantage over bipolar transistors. In particular, the input is coupled capacitively to the device, with the result that all inputs are to capacitors, rather than to the resistances appearing at bipolar transistor inputs. For this reason, the output current from D need not be a dc current to maintain the output level. Instead, the output current is merely that needed to charge the capacitance of the MOS input being driven, going to zero when that capacitance has been

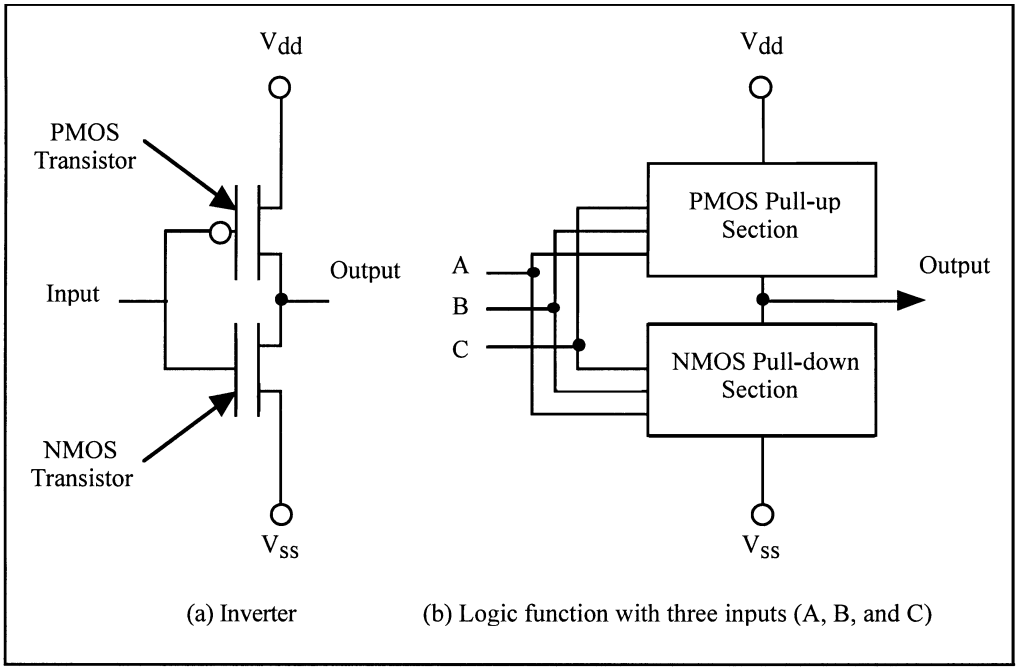


FIGURE 6.1.5 CMOS logic gates.

charged. The result is that, aside from small leakage currents, the dc power dissipation is zero when the pull-up transistors are OFF (output is low). The NMOS circuit does dissipate power when one or more pull-up transistors is in the ON-state since a dc current flows through that transistor through the pull-down resistor.

As technologies advanced, it became possible to efficiently dope selective regions of a substrate in such a manner as to obtain a "well" doped opposite to the substrate. For example, if the substrate is P-type (to create NMOS transistors), a deep well can be doped N-type and PMOS transistors fabricated in that N-type "substrate" region. Being able to fabricate both NMOS and PMOS transistors in the same silicon substrate allows today's CMOS circuits to be created. Figure 6.1.5*a* shows a basic inverter using a PMOS transistor for the pull up and an MOS

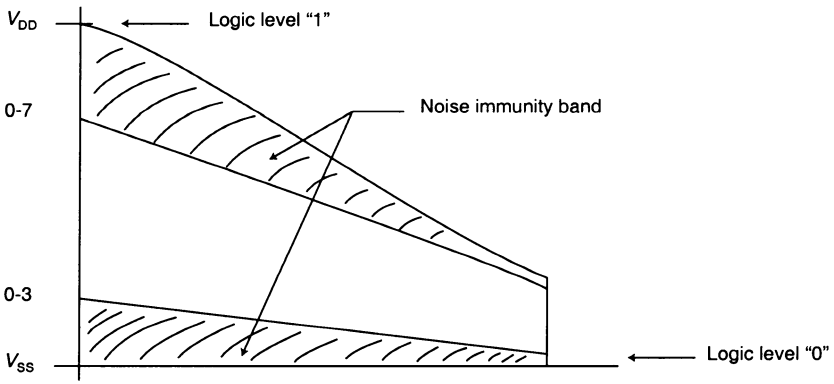


FIGURE 6.1.6 Noise immunity bands for CMOS logic.

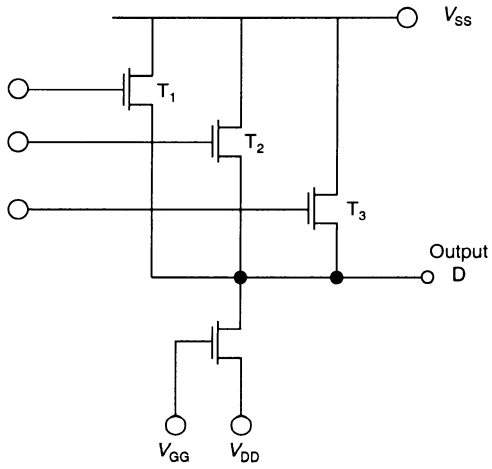


FIGURE 6.1.7 NMOS NOR gate.

transistor for pull down. Figure 6.1.5*b* shows the general organization of a CMOS circuit, consisting of a pull-up circuit using PMOS transistors and a pull-down circuit using NMOS transistors. Properly designed, the same set of digital inputs to the pull down are also applied to the pull up, as shown. Noise immunity characteristics of CMOS logic circuits are shown in Fig. 6.1.6.

The CMOS logic circuits using pull-up and pull-down sections such as shown in Fig. 6.1.5*b* require the same number of transistors in the pull-up section as in the pull-down section but do provide static logic functions (the output is held indefinitely so long as the inputs do not change). Dynamic CMOS logic replaces either the pull-up (pull-down) section with a single transistor used to precharge the capacitive load seen by the output (capacitive since outputs drive the gate of subsequent logic circuits and the gate is essentially a capacitance). When this transistor is turned on and the corresponding pull-down (pull-up) section is OFF, the capacitive load is precharged to logic "1" ("0"). Next, the precharge transistor is turned OFF and the pull-down (pull-up) section is activated, either leaving the output unchanged or driving the output capacitance to logic "0" ("1"). Figure 6.1.8 illustrates the general technique for such "dynamic logic," with the clock signal used to control the activations of the precharge pull-up transistor and of the pull-down section in this example.

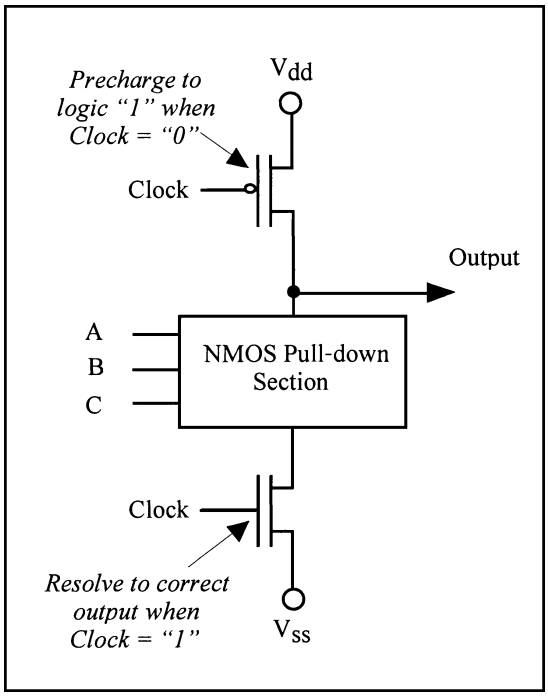
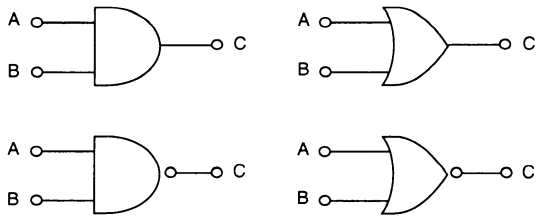


FIGURE 6.1.8 Dynamic CMOS logic gate.



AND and NAND gates | OR and NOR gates

A	B	AND	NAND	OR	NOR
0	0	0	1	0	1
0	1	0	1	1	0
1	0	0	1	1	0
1	1	1	0	1	0

FIGURE 6.1.9 Commonly used gates and truth table.

DIGITAL LOGIC CIRCUITS

The circuits which are described in this and subsequent sections can be fabricated using any of the bipolar or CMOS logic technologies described earlier. The electrical characteristics such as speed and power consumption will be determined by the logic family but the function will be the same in all cases. The circuits described range from simple to more complex types.

Gates

Figure 6.1.9 shows commonly used gates and a truth table gives the functional performance in logic 1 and 0 states. Gates are usually available as hex inverter, quad two input, treble three input, dual four input, and single eight input. AND-OR-INVERT gates are also available and these are used to connect the outputs of two gates together in a wired-OR connection.

In a CMOS transmission gate a *p*- and an *n*-channel transistor are connected together. A gate signal turns on both transistors and so provides an ac path through them, whereas when the transistors are off the gate blocks all signals.

Gates are also made in Schmitt trigger versions. These operate as the discrete component circuits and exhibit an hysteresis between the ON and OFF switching positions.

Flip-flops

Flip-flops are bistable circuits which are mainly used to store a bit of information. The simpler types of flip-flops are also called latches. Figure 6.1.10 shows the symbol for some of the more commonly used flip-flops. There are many variations such as master-slave, J–K, edge-triggered, and gate flip-flops.

In the master–slave set–reset flip-flop, a clock pulse is required. During the rising edge of the clock information is transferred from the *S* and *R* inputs to the master part of the flip-flop. The outputs are unchanged at this stage. During the falling edge of the clock the inputs are disabled so that they can change their state without affecting the information stored in the master section. However, during this phase the information is transferred from the master to the slave of the flip-flop is disabled when no clock pulse is present.

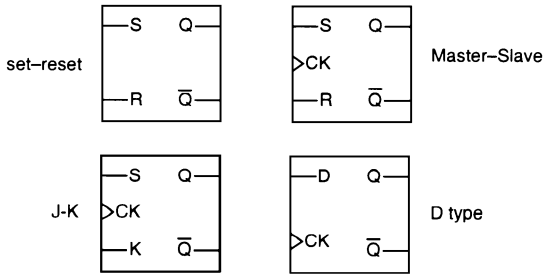


FIGURE 6.1.10 Commonly used flip-flops.

J–K flip-flops are triggered on an edge of the clock waveform. Feedback is used internally within the logic such that the undeterminate state, when both inputs are equal to logic 1, is avoided. Now when the inputs are both at 1, the output will continually change state on each clock pulse. This is also known as *toggling*.

D-type flip-flops have a single input. An internal inverter circuit provides two signals to the J and K inputs so that it operates as a J–K flip-flop, having only two inputs modes.

Counters

Flip-flops can be connected together to form counters in a single package. There are primarily two types, asynchronous and synchronous. The synchronous counters may be subdivided into those with ripple enable and those with parallel or look-ahead carry.

In an asynchronous counter the clock for the next stage is obtained from the output of the preceding stage so that the command signal ripples through the chain of flip-flops. This causes a delay so asynchronous counters are relatively slow, especially for large counts. However, since each stage divides the output frequency of the previous stage by two, the counter is useful for frequency division.

In a synchronous counter, the input line simultaneously clocks all the flip-flops so there is no ripple action of the clock signal from one stage to the next. This gives a faster counter, although it is more complex since internal gating circuitry has to be used to enable only the required flip-flops to change state with a clock pulse. The enable signal may be rippled through between stages or parallel (or look-ahead) techniques may be used, which gives a faster count.

Counters are available commercially, having a binary or BCD count, and which are capable of counting up or down.

Shift Registers

When stored data are moved sequentially along a chain of flip-flops, the system is called a shift register. Commercial devices are available in sizes from four bits to many thousands of bits.

The shift register is serial-in, serial-out, but it is possible to have systems that are parallel data input and output. The only limitation is the number of pins available on the package to accommodate the inputs and outputs. Shift registers can also be designed for left or right shift.

In the register, input data ripple through at the clock pulse rate from the first to the last stage. Sometimes it is advantageous to be able to clock the inputs and outputs at different rates. This is achieved in a first-in first-out (FIFO) register. Each data bit has an associated status and input data are automatically moved along until it reaches the last unused bit in the chain. Therefore the first data to come in will be the first to be clocked out. Data can also be clocked into and out of the register at different speeds, using the two independent clocks.

Data Handling

Several code converter integrated circuits are available commercially. A typical example is a BCD to decimal converter. These converters can also be used as priority encoders. An example may be considered to be a ten-input priority encoder. Several of the lines 0 to 9 may be energized simultaneously but the highest number will generate a BCD output code.

Another example is an eight-channel multiplexer. The channel select lines connect one of the eight data input lines to the output line using BCD code.

Timing

A variety of commercial devices are available to give monostable and astable mutivibrators. Most of these incorporate control gates so that they are more versatile when used in digital systems. A gated monostable will trigger when the voltage at the transistor goes to a logic 1.

External resistors and capacitors are used to vary the duration of the monostable pulse. By feeding the output back to the input, this circuit can also be operated as an astable multivibrator.

Drivers and Receivers

Digital integrated circuits have limited current and voltage drive capability. To interface to power loads, driver and receiver circuits are required, which are also available in an integrated circuit package. The simplest circuit in this category is an array of transistors. Usually the emitters or collectors of the transistors are connected together inside the package to limit the package pin requirements.

For digital transmission systems line drivers and receivers are available. The digital input on the line driver controls an output differential amplifier stage, which can operate into low impedance lines. The line receiver can sense low-level signals via a differential input stage and provide a logic output.

Adders

Adders are the basic integrated circuit units used for arithmetic operations such as addition, subtraction, multiplication, and division. A half-adder adds two bits together and generates a sum and carry bit. A fuller adder has the facility to bring in a carry bit from a previous addition. Figure 6.1.11 shows one bit of the full adder.

The basic single-bit adder can be connected in several ways to add multibit numbers together. In a serial adder the two numbers are stored in shift registers and clocked to the A and B inputs one bit at a time. The carry out is delayed by a clock pulse and fed back to the adder as a carry in.

Serial adders are slow since the numbers are added one bit at a time. A parallel adder is faster. The carry output ripples through from one bit to the next so that the most significant bit cannot show its true value until the carry has rippled right through the system. To overcome this delay, look ahead carry generator may be used. These take in the two numbers in parallel, along with the first carry-in bit, and generate the carry input for all the remaining carry bits.

Adders can be used as subtractors by taking the two's complement of the number being subtracted and then adding. Two's complementing can be obtained by inverting each bit and then adding one to the least significant bit. This can be done within the integrated circuit so that commercial devices are available which can add or subtract, depending on the signal on the control pin.

Adders are used for multiplication by a process of shifting and addition, and division is obtained by subtraction and shifting.

FIGURE 6.1.11 Full adder.

Magnitude Comparators

A magnitude comparator gives an output signal on one of three lines, which indicates which of the two input numbers is larger, or if they are equal. Figure 6.1.12 shows one bit of magnitude comparator. Multibit numbers can be compared by storing them in shift registers and clocking them to the input of the single-bit magnitude comparator, one bit at a time, starting from the most significant bit. Alternatively, parallel comparators may be used where each bit of the two numbers is fed in parallel to a separate comparator bit and the outputs are gated together.

FIGURE 6.1.12 Magnitude comparator.

Rate Multiplier

Rate multipliers can be connected to give a variety of arithmetic functions. A typical example is an adder for adding the numbers X and Y. The clock input in all cases is produced by splitting a single clock into several phases. For the adder $Z = X + Y$ and for the multiplier $Z = XY$.

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