CHAPTER 6.2
ANALOG INTEGRATED CIRCUITS

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INTRODUCTION

Digital logic circuits are designed to preserve the concept of binary states (logic "1" and "0") as voltage levels that are restored to levels defined by the supply voltages at the output of each logic gate. This provides a substantial simplification in the design of complex systems composed of millions of gates—at any point the voltage levels merely reflect the supply voltages at the logic gate driving that point. Analog circuits, on the other hand, must be designed to preserve the concept of a continuum of voltage levels, with the output of an analog component preserving the transformation of an input analog signal into a desired output analog signal. The result is that analog integrated circuits generally do not reach the levels of tens of millions of transistors such as seen in digital logic circuits. The term *analog circuit* has been used somewhat loosely in the past, including circuits such as analog-to-digital converters that convert a continuum of voltage levels into a discrete number corresponding to a set of voltage levels. More recently, the term *mixed signal* VLSI has appeared, representing the placement of both analog circuits and digital circuits on the same integrated circuit. Such mixed signal VLSI merely continues the evolution of the general technology to provide compact and low-cost electronic solutions of practical needs.

One of the developments in digital logic ICs has been the development of *programmable* logic components that can be programmed by the user to implement the logic function desired by the user. Several families of such programmable logic have been developed and present technologies allow not only user programmed logic ICs containing millions of gates but also programmable logic ICs in which the user can embed sophisticated functions such as microprocessors and signal processors. Although not having the efficiency of gate utilization or the speed of fully custom-designed logic ICs, these programmable logic ICs have empowered virtually any user to create low-cost but sophisticated logic circuits through the simple expedient of downloading a configuration file into the IC.

Analog circuits have recently moved also towards such *programmable analog ICs*, providing a set of standard analog circuit functions (operational amplifiers, resistors, and so forth) that can be *programmed* by the user—configuring the interconnections among the analog circuit elements and adjusting the values of some of those elements (e.g., setting the value of a resistor). As these programmable analog IC technologies evolve, programmable VLSI including both digital logic and analog circuit elements will become available, providing the user with powerful components that can be optimized for the specific needs of the user by simply downloading a configuration program to the IC.

There are many distinct types of analog circuit function (operational amplifiers, phase-locked loops, low-noise amplifiers, analog switches, voltage regulators, analog/digital converters, modulators, and so forth). Within each of these analog circuit function types, there are wide ranges of performance specifications. Amplifiers may be intended for lower frequency applications such as audio amplifiers or may be intended for very high frequency applications such as the input amplifier of an RF receiver. Voltage regulators may be required to provide switched local power (generally low current) to subsections of an integrated circuit or may

be required to provide high currents to separate electronic components. Because of the vast differences among the various applications of a particular type of analog circuit, there are corresponding vast differences among the design approaches for those various types. In this chapter, basic analog circuit functions that can be routinely manufactured are reviewed. Specialized techniques for special purpose analog circuits with specialized (and high) performance specifications are not considered. The operational amplifier plays a special role in routine analog circuits and is emphasized here since it demonstrates several of the basic concepts in analog circuit design. Analog-to-digital converters also play a special role, serving as the interface between the analog world and the digital world. Basic analog-to-digital conversions are also discussed. Readers interested in the design and use of analog circuits will find a substantial amount of information (product data sheets, application notes, tutorials, and so forth) available at the websites of the analog IC manufacturers. Although the remarkable evolution of digital ICs is well known (e.g., through the rapid introduction of more powerful personal computers), the equally remarkable advances in analog circuits are far less well known. Although hidden from view within automobiles, cellular telephones, audio equipment, and other consumer products, the miniaturization of analog circuits plays a major role in the rapid expansion of electronics into products of all types, including applications requiring miniaturization of sophisticated analog (and mixed analog/digital) circuit functions.

OPERATIONAL AMPLIFIERS

The operational amplifier, or op amp, was originally developed in response to the needs of the analog computer designer. The object of the device is to provide a gain block whose performance is totally predictable from unit to unit and perfectly defined by the characteristics of an external feedback network. This has been achieved by op amps to varying degrees of accuracy, largely governed by unit cost and complexity. Nevertheless, the accuracy of even low cost units has been refined to a point where it is possible to use an op amp in almost any dc to 1 GHz amplifier/signal processor application.

Ideal Operational Amplifier

The *ideal* operational amplifier of Fig. 6.2.1 is a differential input, single-ended output device that is operated from bipolar supplies. As such, it can easily be used as a virtual earth amplifier. Differential output is possible, although not common, and single supply operation will be discussed later. The ideal op amp has infinite gain, infinite bandwidth, zero bias current to generate a functional response at its inputs, zero offset voltage (essentially a perfect match between the input stages) and infinite input impedance. Because of these characteristics, an infinitesimally small input voltage is required at one input with respect to the other to exercise the amplifier output over its full range.

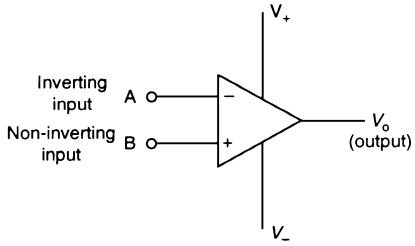

FIGURE 6.2.1 Ideal operational amplifier.

Hence, if one input is held at earth, the other cannot deviate from it under normal operating conditions and becomes a "virtual earth" of the feedback theory definition. The shortfalls against the ideal of practical op amps are now considered with their application consequences.

Input Offset Current

Op-amp fabrication uses monolithic integrated circuit construction, which can produce very well-matched devices for input stages and so on by using identical geometry for a pair of devices fabricated at the same time on the same chip. Nevertheless, there is always some mismatch, which gives rise to the input offset current. This is defined as the absolute difference in input bias current, i.e.,

$$I_{\text{diff}} = |I_A - I_B|$$

Effect of Input Bias and Offset Current

The effect of input bias current will be to produce an unwanted input voltage, which can be much reduced by arranging for the bias current to each input to be delivered from an identical source resistance. Figure 6.2.2 shows a simple inverting amplifier with a gain defined by R_2/R_1, in which R_3 is added to achieve to this effect. In this example the effect of amplifier input impedance is ignored, and signal input impedance is assumed to be zero. In order to balance the bias current source resistance, R_3 is made equal to R_2 in parallel with R_1.

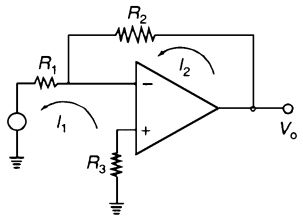

FIGURE 6.2.2 Simple inverting amplifier.

Obviously, the values of the feedback network resistors must be chosen so that, with the typical bias current of the op amp in use, they do not generate voltages that are large in comparison with the supplies and operating output voltage levels. The other sources of error, after balancing source resistances, are the input offset current, and the more insidious effects of the drift of input offset and bias current with temperature, time, and supply voltage, which cannot easily be corrected. Op-amp designers have taken great trouble to minimize the effect of these external factors on the bias and offset current, but, of course, more sophisticated performance is only obtained from progressively more expensive devices. As might be expected, a high precision applications will require an op amp with a high price tag.

Input Offset Voltage and Nulling

As mentioned before a mismatch always exists between the input stages of an op amp, and the input offset voltage (V_{os}) is the magnitude of the voltage that, when applied between the inputs, gives zero output voltage. In bipolar input op amps the major contributor to V_{os} is the bare-emitter voltage mismatch of the differential input stage. General purpose op amps usually have a V_{os} in the region of 1 to 10 mV. This also applies to the modern MOSFET input stage op amps, which achieve an excellent input stage matching with the use of ion implantation. As with the input current parameters, input offset voltage is sensitive to temperature, time, and to a lesser extent input and supply voltages. Offset voltage drift with temperature is often specified as μV per mV of initial offset voltage per °C. As a general rule, the lower the offset voltage of an op amp, the lower is temperature coefficient of V_{os} will be.

Enhanced performance low V_{os} op amps are often produced today by correcting or *trimming* the inherent unbalance of the input stage on chip before or after packaging the device. Techniques used are mainly laser trimming of thin film resistor networks in the input stage and a proprietary process known as *zener zapping*.

Other op amps are available with extra pins connected for a function known as *offset null*. Here a potentiometer is used externally by the user with its slider connected to V_+ or V_- to adjust out the unbalance of the device input stage. A note of caution should be sounded here when using an op amp with an offset null feature in precision circuitry; the temperature coefficient of V_{os} can be changed quite significantly in some op-amp types by the nulling process.

Open Loop Gain

This is one parameter where the practical op-amp approaches the infinite gain ideal very closely and typical gains of 250,000 and higher are quite common at zero frequency. However, it is also common for the gain to start to fall off rapidly at low frequencies, e.g., 10 Hz, with many internally compensated op amps (see Fig. 6.2.3). The commercially available μA741 op amp, for instance, has its gain reduced to unity at around 1 MHz. The closed loop gain is limited by the open loop gain and feedback theory indicates that the greater the difference between open and closed loop gain, the greater the gain accuracy.

Settling Time

Frequently in op-amp applications, such as digital-to-analog converters, the device output is required to acquire a new level within a certain maximum time from a step input change.

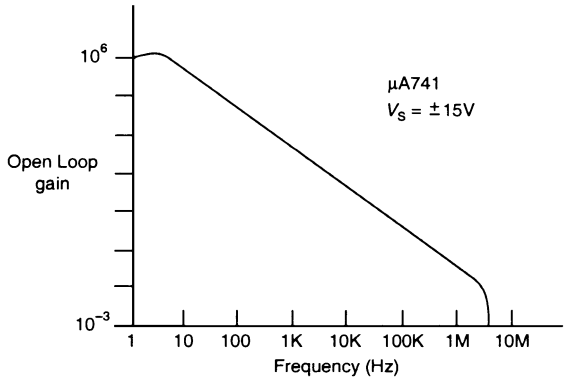

FIGURE 6.2.3 Frequency sensitivity of open loop gain.

The slew rate is obviously a factor in this time, but transient effects will inevitably produce some measure of overshoot and possibly ringing before the final value is achieved. This time, measured to a point where the output voltage is within a specified percentage of the final value, is termed the *settling time*, usually measured in nanoseconds. Careful evaluation of op-amp specifications is required for critical settling time applications, since high-slew-rate op amps may have sufficient ringing to make their settling times worst than medium slew rate devices.

Output Capabilities

As would be expected because of internal design limitations, op amps are unable to achieve an output voltage swing equal to the supply voltages for any significant load resistance. Some devices do achieve a very high output voltage range versus supply, notably those with CMOS FET output stages. All modern op amps have short-circuit protection to ground and either supply built in, with the current limit threshold typically being around 25 μA. It is thus good practice to design for maximum output currents in the 5- to 10-mA region.

Higher current op amps are available but the development of these devices has been difficult because of the heat generated in the output stage affecting input stage drift. Monolithic devices currently approach 1 A and usually have additional circuitry built in to protect against thermal overload and allow output device protection, in addition to normal short-circuit protection.

Power Supply Parameters

The supply consumption will usually be specified at ±5 V, for example, and possibly other supply voltages additionally. Most performance parameters usually deteriorate with reducing supply voltage. Devices are available with especially low power consumption but their performance is usually a trade-off for reduced slew rate and output capability.

Power supply rejection ratio (PSRR) is a measure of the susceptibility of the op amp to variations of the supply voltage. The definition is expressed as the ratio of the change in input offset voltage to the change in supply voltage (μV/V or dB). No op amp ever has a PSRR of less than 70 dB. This should not be taken to indicate that supply bypassing/decoupling is unnecessary. It is good practice to decouple the supplies to general purpose op amps at least every five devices. High speed op amps require careful individual supply decoupling on a by-device basis for maximum stability, usually using tantalum and ceramic capacitors.

Common Mode Range and Rejection

The input voltage range of an op amp is usually equal to its supply voltages without any damage occurring. However, it is required that the device should handle small differential changes at its inputs, superimposed on any voltage level in a linear fashion.

Because of design limitations, input device saturation, and so forth, this operational voltage range is less than the supplies and is termed the common mode input voltage range or swing. As a differential amplifier, the op amp should reject changes in its common mode input voltage completely, but in practice they have an effect on input offset and this is specified as the common mode rejection ratio (CMRR) (μV/V or dB). Note that most general-purpose op amps have a CMRR of at least 70 dB (approximately 300 μV offset change per volt of common mode change) at dc, but this is drastically reduced as the input frequency is raised.

Input Impedance

The differential input resistance of an op amp is usually specified together with its input capacitance. Typical values are 2 MΩ and 1.4 pF for the μA 741.

In practice, the input impedance is usually high enough to be ignored. In inverting amplifiers, the input impedance will be set by the feedback network. In noninverting amplifiers, the input impedance is "bootstrapped" by the op-amp gain, leading to extremely high input impedance for configurations with the feedback case of voltage follower. This bootstrap effect declines as A_{ol} drops off with rising frequency, but it is safe to assume that the circuit input impedance is never worse than that of the op amp itself.

Circuit Stability and Compensation

To simplify design-in and use, many op amps are referred to as "internally" or "fully" compensated. This indicates that they will remain stable for closed loop gains down to unity (100 percent feedback). This almost certainly means that performance has been sacrificed for the sake of convenience from the point of view of users who require higher closed loop gains. To resolve this problem, many op amps are available that require all compensation components to be added externally, according to manufacturers' data and gain requirements. A compromise to this split has been the so-called undercompensated op amps, which are inherently stable at closed loop gains of 5 to 10 and above.

The aim of the standard compensation to shape the open loop response to cross unity gain before the amplifier phase shift exceeds 180°. Thus unconditional stability for all feedback connections is achieved. A method exists for increasing the bandwidth and slew rate of some uncompensated amplifiers known as feedforward compensation. This relies on the fact that the major contributors of phase shift are around the input stage of the op amp and bypassing these to provide a separate high frequency amplifying path will increase the combined frequency response.

OPERATIONAL AMPLIFIER CONFIGURATIONS

Op amps are available ranging from general purpose to ultraprecision. The low-to-medium specification devices are often available in duals and quads. There is a growing trend to standardize on FET input op amps for general-purpose applications, particularly those involving ac amplifiers because of their much enhanced slew rate and lower noise.

Specific devices are available for high speed and high power output requirements. Additionally, some op amps are available as programmable devices. This means their operating characteristics (usually slew rate, bandwidth, and output capability) can be traded off against power supply consumption by an external setting resistor, for instance, to tailor the device to a particular application. Often these amplifiers can be made to operate in the micropower mode, i.e., at low supply voltage and current.

Single-Supply Operational Amplifiers

It is entirely possible to operate any op amp on a single supply. However, the amplifier is then incompatible with bipolar dc signal conditioning. Single-supply operations is entirely suitable for ac amplifiers.

Most later generation op amps have been designed with single supply operation in mind and frequently use pnp differential input arrangements. They have an extended input voltage range, often including ground-in single-supply mode, and are referred to as single-supply op amps.

Chopper and Auto Zero Operational Amplifiers

Many attempts have been made to circumvent the offset and drift problems in op amps for precision amplifier applications. One classic technique is the chopper amplifier, in which the input dc signal is converted to a proportional ac signal by a controlled switch. It is then applied to a high gain accuracy ac amplifier, removing the inherent drift and offset problems. After amplification, dc restoration takes place using a synchronous switching action at the chopper frequency. This is available on a single monolithic device.

Other approaches have used the fact that the output is now required continually, i.e., as in analog to digital converters, and have used the idle period as a self-correction cycle. This again involves the use of a switch, but in this case it is usually used to ground the input of the op amp. The subsequent output is then stored as a replica of actual device error at that moment in time and subtracted from the resultant output in the measurement part of the cycle.

OPERATIONAL AMPLIFIER APPLICATIONS

Op amps are suitable for amplifiers of all types, both inverting and noninverting, dc, and ac With capacitors included in the feedback network, integrators and differentiators may be formed. Active filters form an area where the availability of relatively low cost op amps with precisely defined characteristics has stimulated the development of new circuit design techniques. Filter responses are often produced by op amps configured as gyrators to simulate large inductors in a more practical fashion. Current-to-voltage converters are a common application of op amps in such areas as photodiode amplifiers.

Nonlinear circuit may be formed with diodes or transistors in the feedback loop. Using diodes, precision rectifiers may be constructed, for ac to dc converters, overcoming the normal errors involved with forward voltage drops. Using a transistor in common base configuration within the feedback loop is the basic technique used for generating logarithmic amplifiers. These are extensively used for special analog functions, such as division, multiplication, squaring, square rooting, comparing, and linearization. Linearization may also be approached by the *piecewise* technique, whereby an analog function is *fitted* by a series of different slopes (gain) taking effect progressively from adjustable breakpoints.

Signal generation is also an area where op amps are useful for producing square, triangle, and sine wave functions.

Instrumentation Amplifiers

Many applications in precision measurement require precise, high gain differential amplification with very high common mode rejection for transducer signal conditioning, and so forth. To increase the common mode rejection and gain accuracy available from a single op amp in the differential configuration, a three-op-amp circuit is used, which is capable of much improved performance. The standard instrumentation amplifier format, may be assembled from individual op amps or may be available as a complete (often hybrid) integrated circuit. The inputs are assigned one up amp each which may have gain or act as voltage followers. The outputs of these amplifiers are combined into a single output via the differential op-amp stage. Resistor matching and absolute accuracy is highly important to this arrangement. Suitable resistor networks are available in thin film (hybrid) form.

Comparators

The comparator function can be performed quite easily by an op amp, but not with particularly well-optimized parameters. Specific devices are available, essentially modified op amps, to handle the comparator function in a large range of applications. The major changes to the op amp are to enable the output to be compatible with the logic levels of standard logic families (e.g., TTL, ECL, CMOS) and trade off a linear operating characteristic against speed. A wide common mode input range is also useful. Thus, all the usual op-amp parameters are applicable to comparators, although usually in their role as an interface between analog signals and logic circuits, there is no need for compensation.

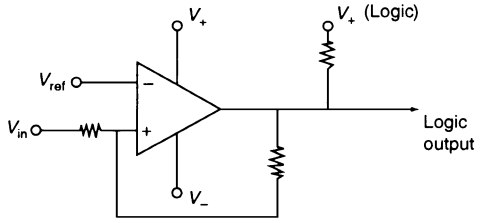

FIGURE 6.2.4 Voltage comparator using op amps.

A typical comparator application shown in Fig. 6.2.4. The circuit has a separate ground terminal to reference the output swing to ground while maintaining bipolar supply operation for the inputs. The output TTL compatibility is achieved by a pull-up resistor to the TTL supply rail V_{CC}, as this is an open collector type comparator. Higher speed comparators will of necessity employ "totem-pole" output structures to maintain fast output transition times. The circuit produces a digital signal dependent on whether the input voltage is above or below a reference threshold. To clean up the switching action and avoid oscillation at the threshold region, it is quite often necessary to apply hysteresis. This is usually relatively easy to achieve with a small amount of positive feedback from the output to input.

General-purpose comparators exhibit response time (time from a step input change to output crossing the logic threshold) in order of 200 ns. Their output currents are limited, compared to op amps, being usually sufficient to drive several logic inputs. Often a strobe function is provided to disable the output from any input related response under logic signal control.

Comparator Applications. Voltage comparators are useful in Schmitt triggers and pulse height discriminators. Analog to digital converters of various types all require the comparator function and frequently the devices can be used independently for simple analog threshold detection. Line receivers, RC oscillators, zero crossing detectors, and level shifting circuits are all candidates for comparator use. Comparators are available in precision and high speed versions and as quads, duals, and singles of the general-purpose varieties. These latter are often optimized for single-supply operation.

ANALOG SWITCHES

Most FETS have suitable characteristics to operate as analog switches. As voltage controlled, majority carrier devices, they appear as quite linear low value resistors in their "on" state and as high resistance, low leakage path in the "off" state.

Useful analog switches may be produced with JEETs (junction field effect transistors) or MOSFETs (metal oxide semiconductor FETs). As a general rule, JFET switches are lowest "off" leakage. Either technology can be integrated in single- or multichannel functions, complete with drivers in monolithic form.

The switched element is the channel of a FET or channels of a multiple FET array, hence the gate drive signal must be referred to the source terminal to control the switching of the drain-source resistance. It can be seen that the supply voltages of the gate driver circuit in effect must contain the allowable analog signal input range. The FET switched element has its potential defined in both states by the analog input voltage and additionally in the off stage by the output potential. The gate drive circuit takes as input of a ground refereed, logic compatible (usually TTL) nature and converts it into a suitable gate control signal to be applied to the floating switch element. The configuration will be such that the maximum analog input range is achieved while minimizing any static or dynamic interaction of the switch element and its control signal. Figure 6.2.5 shows a typical analog switch in block diagram form. This is a dual SPST function. Because of their close relationship to mechanical switches in use,

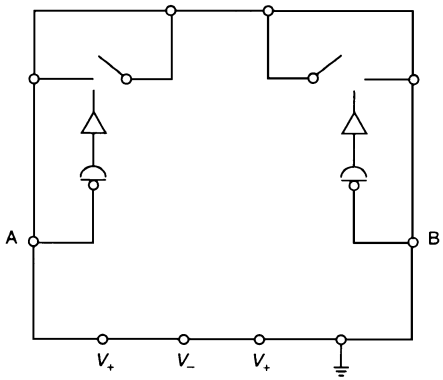

FIGURE 6.2.5 Dual SPST analog switch.

mechanical switch nomenclature is often used, e.g., SPST is single pole, single throw, and DPDT is double pole, double throw, both poles being activated by the same control single. Break-before-make switching is frequently included to avoid shorting analog signal inputs by a pair of switch elements.

The equivalent of single pole multiway switches in monolithic form is referred to as *analog multiplexers*.

Analog Switch Selection

Selection is based on voltage and current handling requirements, maximum on resistance tolerable, minimum off resistance and operating speed. Precautions have to be taken in limiting input overvoltages and some CMOS switches were prone to latch-up, a destructive SCR effect that occurred if the input signal remained present after the supplies have been removed. Later designs have since eliminated this hazard.

SAMPLE AND HOLD CIRCUITS

A sample and hold takes a *snapshot* of an analog signal at a point in time and holds its voltage level for a period by storing it on a capacitor. It can be made up from two op amps connected as voltage followers and an analog switch.

This configuration block diagram is shown in Fig. 6.2.6. In operations, the input follower acts as an impedance buffer and charges the external hold capacitor when the switch is closed, so that it continually tracks the input voltage (the "sample" mode). With the switch turned off, the output voltage is held at the level of the input voltage at the instant of switch off (the "hold" mode). Eventually, the charge on the hold capacitor will be drained away by the input bias current on the follower. Hence the hold voltage *droops* at a rate controlled by the hold capacitor size and the leakage current, expressed as the droop rate in mVs^{-1} μF^{-1}.

When commanded to sample, the input follower must rapidly achieve a voltage at the hold capacitor equivalent to that present at the input. This action is limited by the slew rate into the hold capacitor and settling time of the input follower and it is referred to as the acquisition time. Dynamic sampling also has other sources of error. The hold capacitor voltage tends to lag behind a moving input voltage, due primarily to the on-chip charge current limiting resistor. Also, there is a logic delay (related to "aperture" time) from the onset of the hold command and the switch actually opening, this being almost constant and independent of hold capacitor value. These two effects tend to be of opposite sign, but rarely will they be completely self-cancelling.

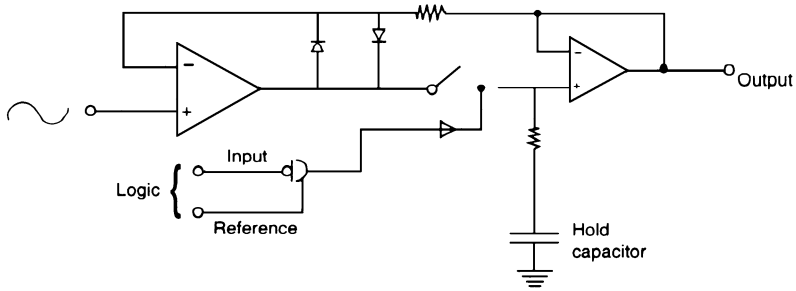

FIGURE 6.2.6 Sample and hold circuit using op amps.

SAMPLE AND HOLD CAPACITOR

For precise applications, the hold capacitor needs more careful selection. To avoid significant errors, capacitors with a dielectric exhibiting very low hysteresis are required. These dielectric absorption effects, are seen as changes in the hold voltage with time after sampling and are not related to leakage. They are much reduced by using capacitors constructed by polystyrene, polypropylene, and PTFE.

The main applications for sample and hold circuits are in analog to digital converters and the effects of dielectric absorption can often be much reduced by performing the digitization rapidly after sampling, i.e., in a period shorter than the dielectric hysteresis relaxation time constant.

DIGITAL-TO-ANALOG CONVERTERS

Digital-to-analog converters (DACs) are an essential interface circuit from the digital world into the analog signal processing area. They are also the key to many analog-to-digital converter techniques that relay on cycling a DAC in some fashion through its operating range until parity is achieved between the DAC output and the analog input signal. All DACs conform to the block diagram of Fig. 6.2.7. The output voltage is a product of the digital input word and an analog reference voltage. The output can only change in discrete steps and the number of steps is immediately defined by the digital inputs. Should this be eight, e.g., an 8-bit DAC, the number of steps will be 256 and the full-scale output will be 256 times voltage increment related to the reference.

Although various techniques can be used to produce the DAC function, the most widely used is variable scaling of the reference by a weighing network switched under digital control. The building blocks of this kind of DAC are (a) reference voltage; (b) weighing network; (c) binary switches; and (d) an output summing amplifier. All may be built in, but usually a minimum functional DAC will combine network and switches.

R-2R Ladders

The weighing network could be binary weighted with voltage switching and summation achieved with a normal inverting op amp. However, even in this simple 4-bit example, there is a wide range of resistor values to implement and speed is likely to suffer due to the charging and discharging of the network input capacitances during conversion. The resistor ladder network employs current switching to develop an output current proportional to the digital word and a reference current. The current switching technique eliminates the transients involving the nodal parasitic capacitances. Significantly, only two resistance values are required and the accuracy of the converter is set by the ratio precision rather than of the absolute value. Analog IC fabrication is capable of accommodating just such resistance value constraints quite conveniently. Monolithic DACs are available in 8- and 12-bit versions and recently in 16 bit. Sixteen-bit and above DACs are also available in hybrid form.

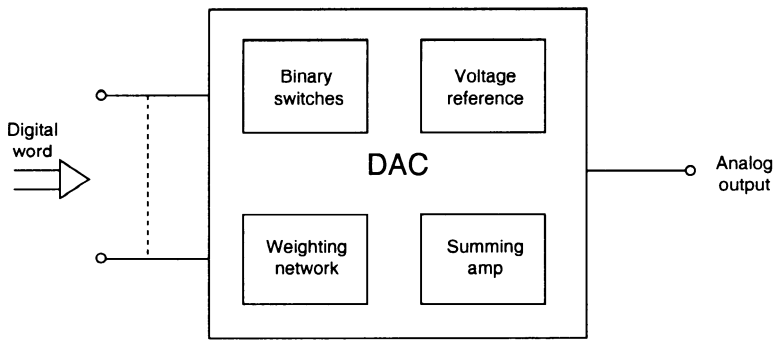

FIGURE 6.2.7 Digital-to-analog converter.

Resolution, Linearity and Monotonicity

Resolution has already been touched upon as being defined by the digital word length and reference voltage increment. However, it is important to note that it is quite possible to have, say, a 12-bit DAC in terms of resolution which is incapable of 12-bit accuracy. This is because of nonlinearities in the transfer function of the DAC. It may well be accurate at full scale but deviate from an ideal straight line response because of variations in step size at other points on the characteristic. Linearity is specified as a worst case percentage of full-scale output over the operating range. To be accurate to n bits, the DAC must have a linearity better than $^1/_2$ LSB (LSB = least significant bit, equivalent to step size) expressed as a percentage of full scale (full scale = 2 in. × step size).

Differential linearity is the error in step size from ideal between adjacent steps and its worst-case level determines whether the converter will be monotonic. A monotonic DAC is one in which, at any point in the characteristic from zero to full scale, an increase in the digital code results in an increase in the absolute value of the output voltage. Nonmonotonic converters may actually "reverse" in some portion of the characteristic, leading to the same output voltage for two different digital inputs. This obviously is a most undesirable characteristic in many applications.

Settling Time

The speed of a DAC is defined in terms of its settling time, very similar to an op amp. The step output voltage change used is the full-scale swing from zero and the rated accuracy band is usually $+^1/_2$ LSB. Settling times of 100 = 200 ns are common with 8-bit, 4-2R ladder monolithic DACs. The compensation of the reference op amp will have a bearing on settling time and must be handled with care to maintain a balance of stability and speed.

Other DAC Techniques

There are many other methods that have been proposed and used for the DAC function. There is insufficient space here to make a full coverage. However, mention should be made of the pulse width technique. The digital inputs are assigned time weighing so that in, say, a 6-bit DAC, the LSB corresponds to 1 time unit and the MSB to 32 time units. The time units are derived by variable division from a master clock and usually clocked out at a rate which is some submultiple of the master clock.

The duty cycle will then vary between 0 and 63/64 in its simplest form. This pulse rate is integrated by an averaging filter (usually RC) to produce a smooth dc output. The full scale is obviously dependent on the pulse height and this must be related back to a voltage reference, albeit only a regulated supply. This type of DAC* is often used for generating control voltages for voltage controlled amplifiers used for volume, brightness, color, and so forth (TV application), and it is possible to combine two 6-bit pulse width ratio outputs for 12-bit resolution (not accuracy) to drive voltage controlled oscillators, i.e., varactor tuners. This is one application (tuning) where nonmonotonicity can be acceptable.

ANALOG-TO-DIGITAL CONVERTERS

Analog-to-digital converters (ADCs) fall into three major categories: (a) direct converters; (b) DAC feedback; and (c) integrating.

Direct or "Flash" Converters

Flash converters have limited resolution but are essential for very high-speed applications. They also have the advantage of providing a continuous stream of the digitized value of the input signal, with no *conversion time*

waiting period. They consist of a reference voltage which is subdivided by a resistor network and applied to the inputs of a set of comparators. The other inputs of the comparator are common to the input voltage. A digital encoder would then produce, in the case of a 3-bit converter, for example, a weighted 3-bit output from the eight comparator inputs. The method is highly suitable to video digitization and is usually integrated with a high-speed digital logic technology such as ECL or advanced Schottky TTL. Flash converters in monolithic form of up to 9-bit resolution have been built.

Feedback ADCs

Feedback ADCs use a DAC within a self-checking loop, i.e., a DAC is cycled through its operating range until parity is achieved with the input. The digital address of the DAC at that time is the required ADC output. Feedback ADCs are accurate with a reasonably fast conversion time. Their resolution limitations are essentially those of the required DAC cost, performance, and availability.

Feedback ADCs require a special purpose logic function known as a successive approximation register (SAR). The SAR uses an iterative process to arrive at parity with the ADC input voltage in the shortest possible time. It changes the DAC addresses in such a way that the amplitude of the input is checked to determine whether it is greater or smaller than the input on a bit sequential basis, commencing with the MSB. This implies continuous feedback from a comparator on the analog input and DAC output connected to the SAR.

Figure 6.2.8 shows a block diagram of a 10-bit ADC available on a single chip. The 10-bit DAC is controlled by a 10-bit SAR with an internal clock, and the DAC has an on-board reference. The digital output is fed through tristate buffers to ease the problems of moving data onto a bus-structured system. These are high impedance (blank) until the device is commanded to perform a conversion.

After the conversion time, typically 25 μs for this type of device, a data ready flag is enabled and correct data presented at the ADC output. An input offset control is provided so that the device can operate with bipolar inputs. Because of the nature of the conversion process, satisfactory operation with rapidly changing analog inputs may not be achieved unless the ADC is preceded by a simple and hold circuit.

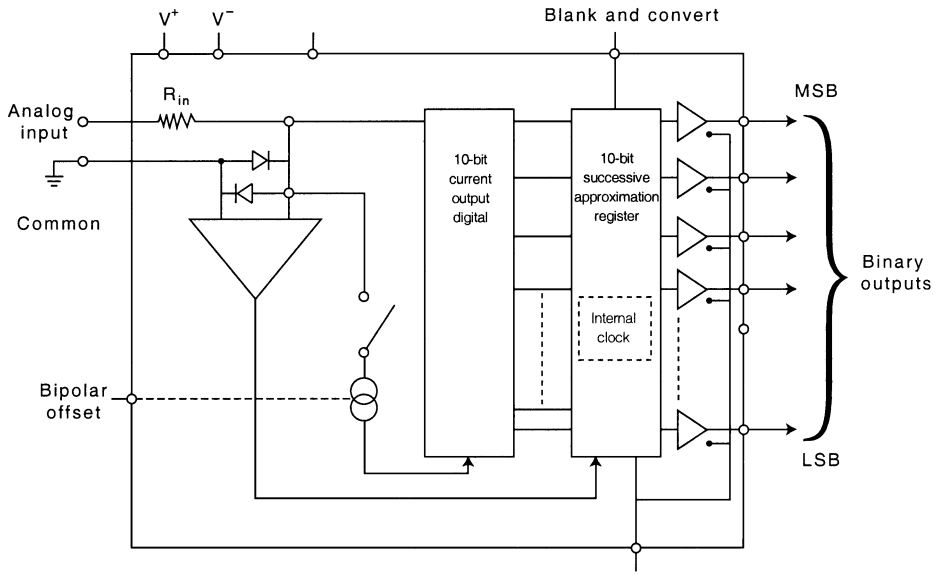

FIGURE 6.2.8 10-bit analog-to-digital converter.

Integrating ADCs

Integrating ADCs use a variety of techniques, but all usually display high resolution and linearity. They also have a much greater ability to reject noise on the analog input than other types of ADC. The penalty that is paid for this is a much longer conversion time which is also variable with actual input voltage. These factors make integrating ADCs very suitable for digital voltmeter, panel meter, and other digital measuring applications.

BIBLIOGRAPHY

Jaeger, R. C., "Microelectronic Circuit Design," Irwin McGraw-Hill, 1997.

Muller, J., and T. Kamins, "Device Electronics for Integrated Circuits," John Wiley and Sons, 2003.

Ng, K. K., "Complete Guide to Semiconductor Devices," Wiley Interscience, 2002.

Terrell, D., "Op Amps, Design, Application and Troubleshooting," Butterworth-Heinemann, 1996.