CHAPTER 13.3
DC-DC CONVERTERS

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INTRODUCTION

Power conversion among different dc voltage and current levels is important in applications ranging from spacecraft and automobiles to personal computers and consumer products. Power electronics technology can be used to create a *dc transformer* function for power processing. Today, most dc power supplies rectify the incoming ac line, then use a dc-dc converter to provide a transformer function and produce the desired output voltages. Dc-dc designs often use input voltages near 170 V (the peak value of rectified 120-V ac) or 300–400 V (the peak values of 230, 240 V ac, and many three-phase sources). For direct dc inputs, 48-V sources and 28-V sources reflect practice in the telecommunications and aerospace industries. *Universal input power* supplies commonly handle rectified power from sources ranging between 85 and 270 V ac.

There are a number of detailed treatments of dc-dc converters in the literature. The book by Severns and Bloom (1985) explores a wide range of topologies. Mitchell (1988) offers detailed analysis and extensive treatment of control issues. Chryssis (1989) compares topologies from a practical standpoint, and addresses many aspects associated with actual implementation. Middlebrook has published several exhaustive treatments of various topologies; one example (Middlebrook, 1989) addresses some key attributes of analysis and control. The discussion here follows the treatment in Krein (1998). More recently, Erickson and Maksimovich (2001) have detailed many operation and control aspects of modern dc-dc converters.

DIRECT DC-DC CONVERTERS

The most general dc-dc conversion process is based on a switch matrix that interconnects two dc ports. The two dc ports need to have complementary characteristics, since Kirchhoff's laws prohibit direct interconnection of unlike voltages or currents. A generic example, called a *direct converter*, is shown in Fig. 13.3.1*a*. A more complete version is shown in Fig. 13.3.1*b*, in which an inductor provides the characteristics of a current source. In the figure, only four switch combinations can be used without shorting the voltage source or opening the current source:

Combination	Result
Close 1,1 and 2,2	$V_d = V_{IN}$
Close 2,1 and 2,2	$V_d = 0$
Close 1,1 and 1,2	$V_d = 0$
Close 1,2 and 2,1	$V_d = -V_{IN}$

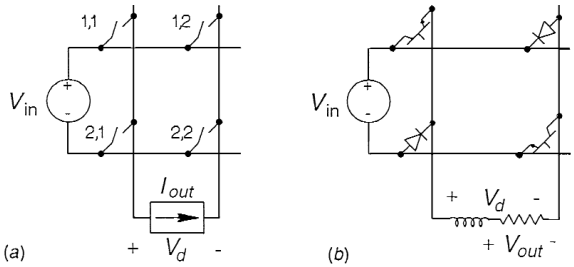

FIGURE 13.3.1 Dc voltage to dc current direct converter: (*a*) general arrangement; (*b*) circuit realization.

Switch action selects among $-V_{in}$, 0, and $+V_{in}$ to provide a desired average output. The energy flow is controlled by operating the switches periodically, then adjusting the *duty ratio* to manipulate the average behavior. Duty-ratio control, or *pulse width modulation*, is the primary control method for most dc-dc power electronics. The switching frequency can be chosen somewhat arbitrarily with this method. Typical rates range from 50 kHz to 500 kHz for converters operating up to 200 W, and from 20 kHz to 100 kHz for converters operating up to 2 kW. In dc-dc circuits that use soft switching or *resonant switching* techniques, the switching frequency is usually adjusted to match internal circuit resonances.

Switching functions $q(t)$ can be defined for each switch in the converter. A switching function has the value 1 when the associated switch is on, and 0 when it is off. The converter voltage v_d in Figure 13.3.1*b* can be written in terms of the switching functions in the compact form

$$v_d(t) = q_{1,1}q_{2,2}V_{in} - q_{1,2}q_{2,1}\,V_{in} \tag{1}$$

For power flow in one direction, two switches suffice. The usual practice is to establish a common ground between the input and output, equivalent to permanently turning on switch 2,2 and turning off switch 1,2 in Fig. 13.3.1. This simplified circuit is shown in Fig. 13.3.2. The transistor is generic: a BJT, MOSFET, IGBT, or other fully controlled device can be used. The voltage $v_d(t)$ in this circuit becomes $v_d(t) = q_1(t)V_{in}$. Of interest is the dc or average value of the output, indicated by the angle brackets as $\langle v_{out}(t)\rangle$. The inductor cannot sustain an average voltage in the periodic steady state, so the resistor voltage average value $\langle v_{out}(t)\rangle = \langle v_d(t)\rangle$. The voltage $v_d(t)$ is a pulse train with period T, amplitude V_{in}, and an average value related to the duty ratio of the switching function. Therefore,

$$\langle v_d(t)\rangle = \langle v_{out}(t)\rangle = \frac{1}{T}\int_0^T q_1(t)V_{in}dt = D_1V_{in} \tag{2}$$

where T is the switching period and D_1 is the duty ratio of the transistor. (Typically, an average value in a dc-dc converter is equivalent to substituting a switch duty ratio D for a switching function q.) If the L-R pair serves

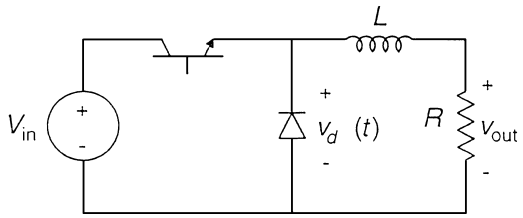

FIGURE 13.3.2 Common-ground direct converter (*buck converter*).

TABLE 13.3.1 Buck Converter Characteristics

Characteristic	Value
Input–output relationships	$V_{out} = D_1 V_{in}$, $I_{in} = D_1 I_{out}$
Device ratings	Must handle V_{in} when off, and I_{out} when on.
Open-loop load regulation	Load has no direct effect on output.
Open-loop line regulation	No line regulation: line changes are reflected directly at the output. Feedback control is required.
Ripple	Governed by choice of inductor. Typically 50 mV $_{peak–to–peak}$ or 1 percent (whichever is higher) can be achieved.

as an effective low-pass filter, the output voltage will be a dc value $V_{out} = \langle v_d(t) \rangle$. The circuit has the basic characteristics of a transformer, with the restriction that $V_{out} \le V_{in}$. The name *buck converter* is used to reflect this behavior.

The buck converter, sometimes called a *buck regulator*, or a *step-down converter,* is the basis for many more sophisticated dc-dc converters. Some of its characteristics are summarized in Table 13.3.1. Load regulation is perfect in principle if the inductor maintains current flow. Line regulation requires closed-loop control. Although these relationships are based on ideal, lossless switches, the analysis process applies to more detailed circuits. The following example illustrates the approach.

Example: Relationships in a dc-dc converter.

The circuit of Fig. 13.3.3 shows a dc-dc buck converter with switch on-state voltage drops taken into account. What is the input–output voltage relationship? How much power is lost in the converter?

To analyze the effect of switch voltages, KVL and KCL relations can be written in terms of switching functions. When averages are computed, variables such as inductor voltages and capacitor currents are eliminated since these elements cannot sustain dc voltage and current, respectively. Circuit laws require

$$\begin{aligned} v_d(t) &= q_1(t)\,(V_{in} - V_{s1}) - q_2(t) V_{s2}, \qquad V_{out} = v_d(t) - v_L \\ i_{in}(t) &= q_1(t) I_L, \qquad I_{out}(t) = I_L - i_C(t) \end{aligned} \tag{3}$$

In this circuit, the inductor will force the diode to turn on whenever the transistor is off. This can be represented with the expression $q_1(t) + q_2(t) = 1$. When the average behavior is computed, the duty ratios must follow the relationship $D_1 + D_2 = 1$. The average value of $v_d(t)$ must match V_{out}, and the average input will be the duty ratio of switch 1 multiplied by the inductor current. These relationships reduce to

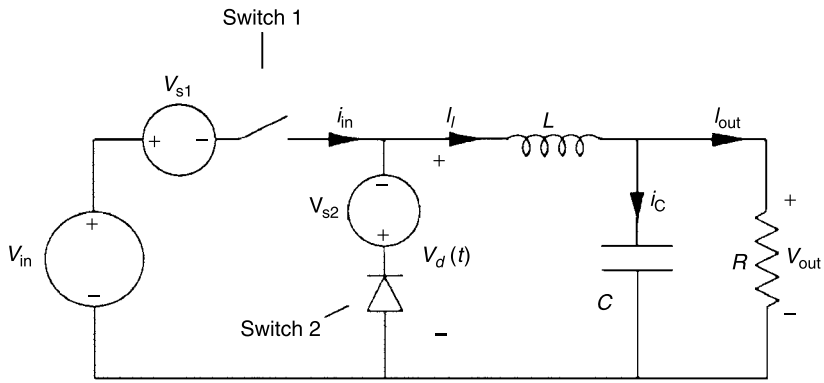

FIGURE 13.3.3 Buck converter with switch forward drop models.

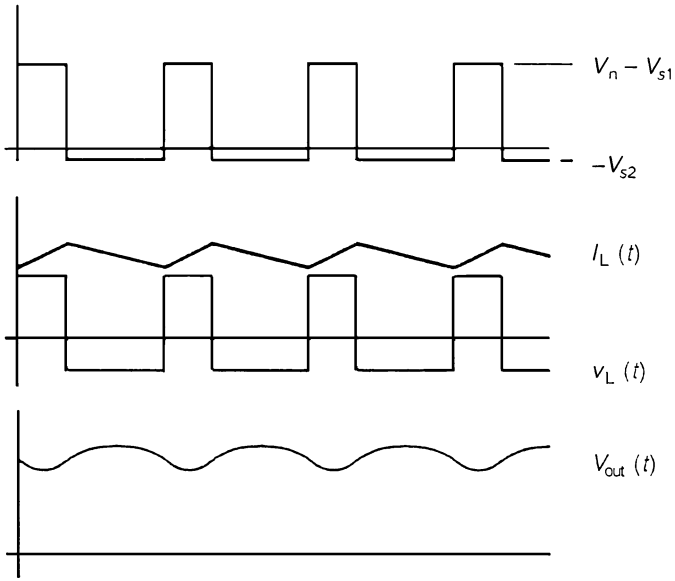

FIGURE 13.3.4 Buck converter waveforms.

$$\begin{aligned} V_{\text{out}} &= D_1(V_{\text{in}} - V_{s1} + V_{s2}) - V_{s2} \\ \langle i_{\text{in}}(t)\rangle &= D_1 I_{\text{out}} \\ P_{\text{in}} &= \langle i_{\text{in}}(t) V_{\text{in}}\rangle = D_1 V_{\text{in}} I_{\text{out}} \\ P_{\text{out}} &= V_{\text{out}} I_{\text{out}} = D_1(V_{\text{in}} - V_{s1} + V_{s2}) I_{\text{out}} - V_{s2} I_{\text{out}} \end{aligned} \tag{4}$$

When the switch voltage drops V_{s1} and V_{s2} have similar values, the loss fraction is approximately the ratio of the diode drop to the output voltage.

The primary design considerations are to choose an inductor and capacitor to meet requirements on output voltage ripple. The design process is simple if a *small ripple assumption* is used: since V_{out} is nearly constant, the voltage across the inductor will be a pulsed waveform at the switching frequency. The current $i_L(t)$ will exhibit triangular ripple. Some waveform samples appear in Fig. 13.3.4. The current swings over its full peak-to-peak ripple during either the transistor on time or the diode on time. The example below takes advantage of the triangular variation to compute the expected ripple.

Example: *Buck converter analysis.*

A buck converter circuit with an R-L load and a switching frequency of 200 kHz is shown in Fig. 13.3.5. The transistor exhibits on-state drop of 0.5 V, while the diode has a 1 V forward drop. Determine the output ripple for 15 V input and 5 V output. From Eq. (5), the duty ratio of switch 1 should be 6/15.5 = 0.387. Switch 1 should be on for 1.94 μs, then off for 3.06 μs. At 5 V output, the inductor voltage is 9.5 V with switch 1 on and –6 V with switch 1 off. The inductor current has di/dt = (9.5 V)/(200 μH) = 47.5 kA/s when #1 is on and di/dt = –30 kA/s when #2 is on. During the on time of switch 1, the current increases (47500 A/s)·(1.93 μs) = 0.092 A. Here, the time constant L/R = 200 μs, which is 65 times the switch 2 on time. It would be expected that the current change is small and linear. The current change of 0.092 A produces an output voltage change of 0.092 V for this 1 Ω load. Figure 13.3.6 shows some of the important waveforms in idealized form. The output voltage is nearly constant, with $V_{\text{out}} = 5 \pm 0.046$ V, consistent with the assumptions in the analysis. The output power is 25 W. The input average current is $D_1 I_{\text{out}}$ = 0.387(5 A) = 1.94 A. The input power therefore is 29.0 W, and the efficiency is 86 percent. This neglects any energy consumed in the commutation process.

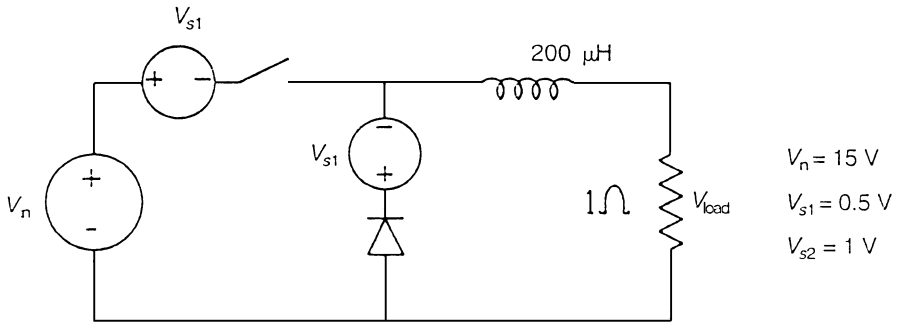

FIGURE 13.3.5 Buck converter example.

More generally, the buck converter imposes $V_{in} - V_{out}$ on the inductor while the transistor is on. The current derivative *di/dt* over a given time interval is the linear change $\Delta i_L/\Delta t$. For the on-time interval $\Delta t = D_1 T$, the peak-to-peak ripple Δi_L *is*

$$\Delta i_L = \frac{(V_{in} - V_{out})D_1 T}{L} = \frac{V_{in}(1 - D_1)D_1 T}{L} \tag{5}$$

If only inductive filtering is used, the output voltage ripple is the load resistance times the current ripple.

If an output capacitor is added across the load resistor, its effect can be found by treating the inductor as an equivalent triangular current source, then solving for the output voltage. Assuming that the capacitor handles the full ripple current, it is straightforward to integrate the triangular current to compute the ripple voltage. The process is illustrated in Fig. 13.3.7. Voltage $v_C(t)$ will increase whenever $i_C(t) > 0$. The voltage increase is given by

$$\Delta v_C = \frac{1}{C}\int_0^{T/2} i_C(t)\,dt \tag{6}$$

The integral is the triangular area $^1/_2(T/2)(\Delta i_L/2)$, so

$$\Delta v_C = \frac{T\Delta i_L}{8C} \tag{7}$$

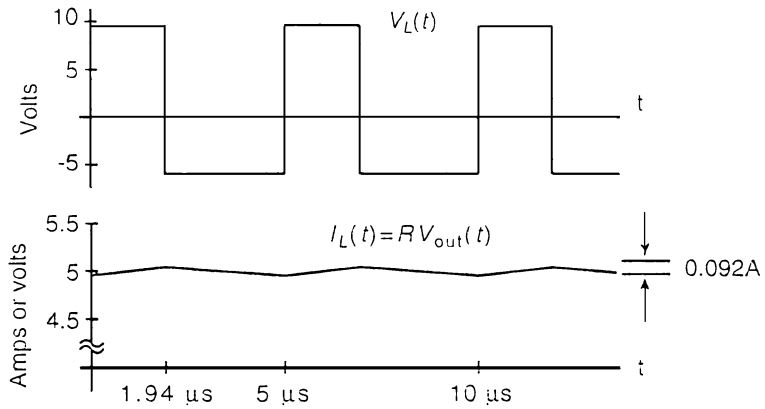

FIGURE 13.3.6 Buck converter inductor voltage and output current.

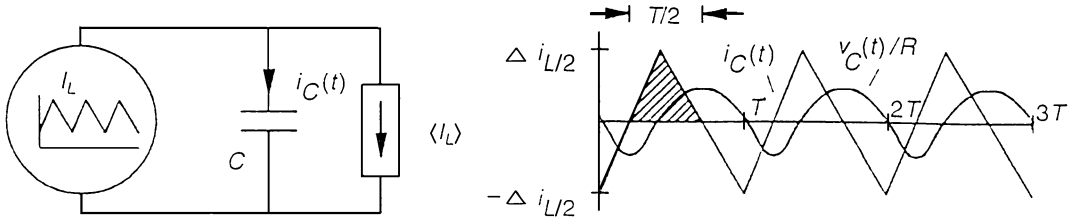

FIGURE 13.3.7 Output ripple effect given the addition of capacitive filter.

This expression is accurate if the capacitor is large enough to provide significant voltage ripple reduction.

An alternative direct dc-dc converter has a current source input and voltage source output. The relationships for this *boost converter* are dual to those of the buck circuit. The input current and output voltage act as fixed source values, while the input voltage and output current are determined by switch matrix action. For the common-ground version in Fig. 13.3.8*b*, the transistor and diode must operate in complement, so that $q_1 + q_2 = 1$ and $D_1 + D_2 = 1$. For ideal switches,

$$\begin{aligned} q_1 + q_2 &= 1 \\ v_t(t) &= q_2 V_{\text{out}} = (1 - q_1) V_{\text{out}} \\ i_{\text{out}} &= q_2 I_{\text{in}} = (1 - q_1) I_{\text{in}} \\ \langle v_t \rangle &= D_2 V_{\text{out}} = (1 - D_1) V_{\text{out}} \\ \langle i_{\text{out}} \rangle &= (1 - D_1) I_{\text{in}} \end{aligned} \tag{8}$$

With these energy storage devices, notice that $V_{\text{in}} = \langle v_t \rangle$ and $I_{\text{out}} = \langle i_{\text{out}} \rangle$. The relationships can be written

$$V_{\text{out}} = \frac{1}{1 - D_1} V_{\text{in}} \qquad \text{and} \qquad I_{\text{in}} = \frac{1}{1 - D_1} I_{\text{out}} \tag{9}$$

The output voltage will be higher than the input. The boost converter uses an inductor at the input to create current-source behavior and a capacitor at the output to provide voltage source characteristics. The capacitor

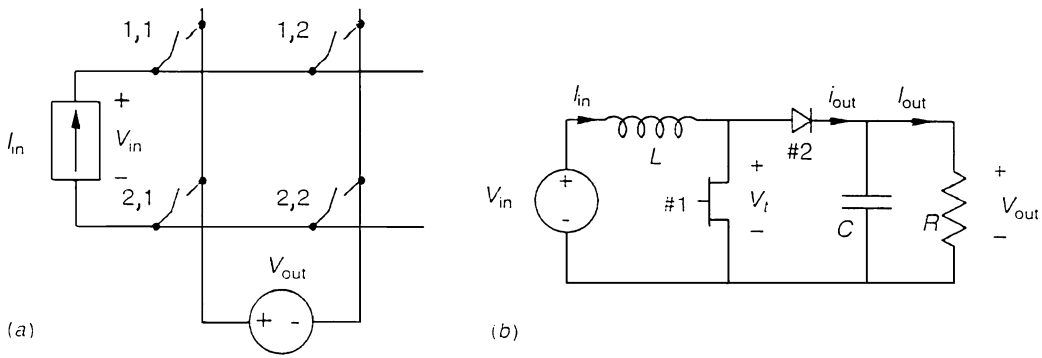

FIGURE 13.3.8 Boost dc-dc converter: (*a*) general arrangement; (*b*) common-ground version.

TABLE 13.3.2 Relationships for the Boost Converter

Characteristic	Value
Input–output relationships	$V_{out} = V_{in}/(1 - D_1)$, $I_{out} = I_{in}(1 - D_1)$
Open-loop load regulation	Load does not alter output
Open-loop line regulation	Unregulated without control
Device ratings	Must handle V_{out} when off or I_{in} when on
Input–output relationships with switch drops	$V_{out} = (V_{in} - V_{s2} - D_1V_{s1} + D_1V_{s2})/(1 - D_1)$, $I_{out} = I_{in}(1 - D_1)$
Inductor ripple relationship	$\Delta i_L = V_{in}D_1T/L$ (if Δi_L is small compared to the input current)
Capacitor ripple relationship	$\Delta v_C = I_{out}D_1T/C$

is exposed to a square-wave current signal, and produces a triangular ripple voltage in response. Table 13.3.2 provides a summary of relationships, based on ideal switches.

INDIRECT DC-DC CONVERTERS

Cascade arrangements of buck and boost converters are used to avoid limitations on the magnitude of V_{out}. A buck-boost cascade is developed in Fig. 13.3.9. This is an example of an *indirect converter* because at no point in time does power flow directly from the input to the output. Some of the switches in the cascade are redundant, and can be removed. In fact, only two switches are needed in the final result, shown in Fig. 13.3.10. The current source, called a *transfer current source*, has been replaced by an inductor.

The voltage across the inductor, v_t, is V_{in} when switch 1 is on, and $-V_{out}$ when switch 2 is on. The transfer current source value is I_s. The inductor cannot sustain dc voltage drop, so $\langle v_t \rangle = 0$. The voltage relationships are

$$\begin{aligned} q_1 + q_2 &= 1 \\ v_t &= q_1V_{in} - q_2V_{out} \\ \langle v_t \rangle &= 0 = D_1V_{in} - D_2V_{out} \end{aligned} \tag{10}$$

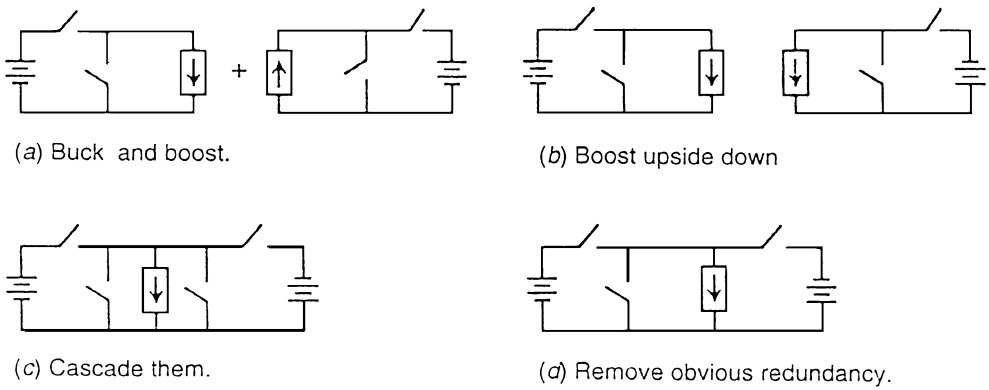

FIGURE 13.3.9 Cascaded buck and boost converters. (From Krein (1998), copyright © 1998 Oxford University Press, Inc., U.S.; used by permission.)

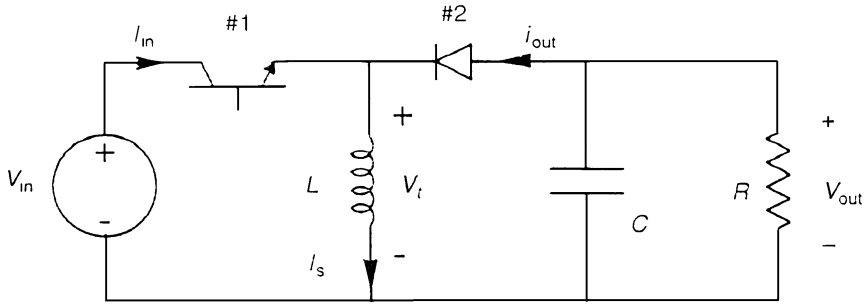

FIGURE 13.3.10 Buck-boost converter.

The last part of Eq. (10) requires $D_1 V_{in} = D_2 V_{out}$ in steady state. The switches must act in complement, so $D_1 + D_2 = 1$, and

$$V_{out} = \frac{D_1}{1 - D_1} V_{in} \tag{11}$$

A summary of results is given in Table 13.3.3. The cascade process produces a negative voltage with respect to the input. This polarity reversal property is fundamental to the buck-boost converter.

A boost-buck cascade also allows full output range with a polarity reversal. As in the buck-boost case, many of the switches are redundant in the basic cascade, and only two switches are required. The final circuit, with energy storage elements in place, as shown in Fig. 13.3.11. The center capacitor serves as a *transfer voltage source.* The transfer source must exhibit $\langle i_t \rangle = 0$, since a capacitor cannot sustain dc current. Some of the major relationships are summarized in Table 13.3.4. In the literature, this arrangement is called a Ćuk converter, after the developer who patented it in the mid-1970s (Middlebrook and Ćuk, 1977). The transfer capacitor must be able to sustain a current equal to the sum of the input and output currents. The RMS capacitor current causes losses in the capacitor's internal equivalent series resistance (ESR), so low ESR components are usually required.

Figure 13.3.12 shows the *single-ended primary inductor converter* or SEPIC circuit (Massey and Snyder, 1977). This is a boost-buck-boost cascade. As in the preceding cases, the cascade arrangement can be simplified to require only two switches. The transfer sources C_t and L_t carry zero average power to be consistent with a capacitor and an inductor as the actual devices. The relationships are

$$\begin{aligned} v_{in} &= q_2(V_{out} + V_{t1}), \quad \langle v_{in} \rangle = D_2(V_{out} + V_{t1}) \\ i_{out} &= q_2(I_{in} + I_{t2}), \quad \langle i_{out} \rangle = D_2(I_{in} + I_{t2}) \\ i_{t1} &= -q_1 I_{t2} + q_2 I_{in}, \quad \langle i_{t1} \rangle = 0 = -D_1 I_{t2} + D_2 I_{in} \end{aligned} \tag{12}$$

TABLE 13.3.3 Buck-Boost Converter Relationships

Characteristic	Value
Input–output voltage relationship	$\lvert V_{out}\rvert = V_{in} D_1/1 - D_1)$, $I_{in} = \lvert I_{out}\rvert\, D_1/(1 - D_1)$, output is negative with respect to input
Device ratings	Must handle $\lvert V_{in}\rvert + \lvert V_{out}\rvert$ when off, $\lvert I_{in}\rvert + \lvert I_{out}\rvert$ when on
Inductor current	$I_L = \lvert I_{in}\rvert - \lvert I_{out}\rvert$
Regulation	Perfect load regulation. No open-loop line regulation
Inductor ripple current	$\Delta i_L = V_{in} D_1 T/L$
Capacitor ripple voltage	$\Delta v_C = \lvert I_{out}\rvert\, D_1 T/C$
Output range	Ideally, any negative voltage can be produced

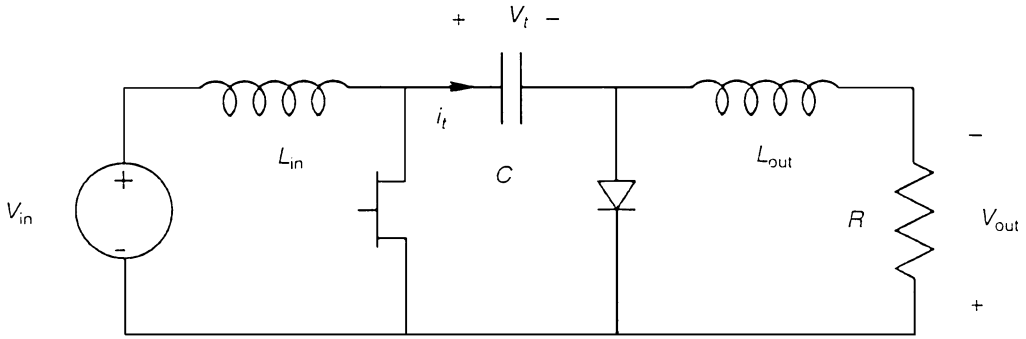

FIGURE 13.3.11 Boost-buck converter.

$$v_{t2} = -q_1 V_{t1} + q_2 V_{\text{out}}, \quad \langle v_{t2} \rangle = 0 = -D_1 V_{t1} + D_2 V_{\text{out}}$$
$$q_1 + q_2 = 1, \quad D_1 + D_2 = 1$$

Some algebra will bring out the transfer source values and input-output ratios:

$$I_{t2} = \frac{D_2}{D_1} I_{\text{in}} = \frac{1 - D_1}{D_1} I_{\text{in}}$$
$$V_{t1} = \frac{D_2}{D_1} V_{\text{out}} = \frac{1 - D_1}{D_1} V_{\text{out}} \tag{13}$$
$$\langle v_{\text{in}} \rangle = D_2 \left(V_{\text{out}} + \frac{1 - D_1}{D_1} V_{\text{out}} \right) = \frac{1 - D_1}{D_1} V_{\text{out}}$$

This is the same input–output ratio as the buck-boost converter, except that there is no polarity reversal.

These and related indirect converters provide opportunities for the use of more sophisticated magnetics such as *coupled inductors.* In the Ćuk converter, for example, the input and output filter inductors are often coupled on a single core to cancel out part of the ripple current (Middlebrook and Ćuk, 1981). In a buck-boost converter, the transfer source inductor can be split by providing a second winding. One winding can be used to inject energy into the inductor, while the other can be used to remove it. The two windings provide isolation. This arrangement is known as a *flyback converter* because diode turn-on occurs when the inductor output coil voltage "flies back" as the input switch turns off. An example is shown in Fig. 13.3.13.

The flyback converter is one of the most common low-power dc-dc converters. It is functionally equivalent to the buck-boost converter. This is easy to see if the turns ratio between the windings is unity. The possibility of a nonunity turns ratio is a helpful extra feature of the flyback converter. Extreme step-downs, such as the 170-V to 5-V converter, often used in a dc power supply, can be supported with reasonable duty ratios by selecting an appropriate turns ratio. In general, flyback converters are designed to keep the nominal duty ratio close to 50 percent. This tends to minimize the energy storage requirements, and keeps the sensitivity to variation as

TABLE 13.3.4 Relationships for Boost-Buck Converter

Characteristic	Value
Input–output relationships	$\lvert V_{\text{out}} \rvert = D_1 V_{\text{in}}/(1 - D_1)$, $I_{\text{in}} = D_1 \lvert I_{\text{out}} \rvert (1 - D_1)$
Device ratings	Must handle $\lvert V_{\text{in}} \rvert + \lvert V_{\text{out}} \rvert$ when off. Must handle $\lvert I_{\text{in}} \rvert + \lvert I_{\text{out}} \rvert$ when on
Regulation	Perfect load regulation, no line regulation

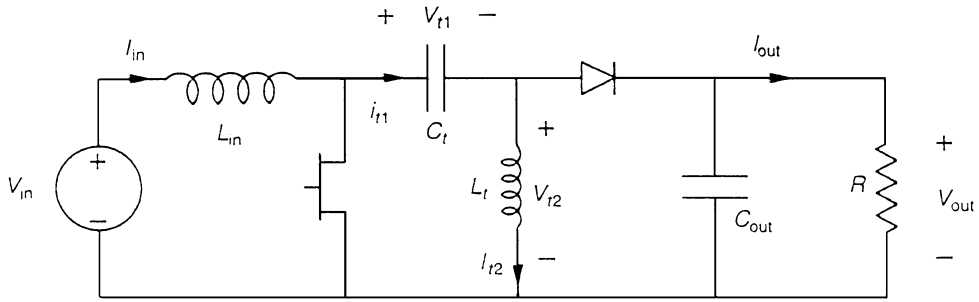

FIGURE 13.3.12 The SEPIC converter. Two transfer sources permit any input-to-output ratio without polarity reversal.

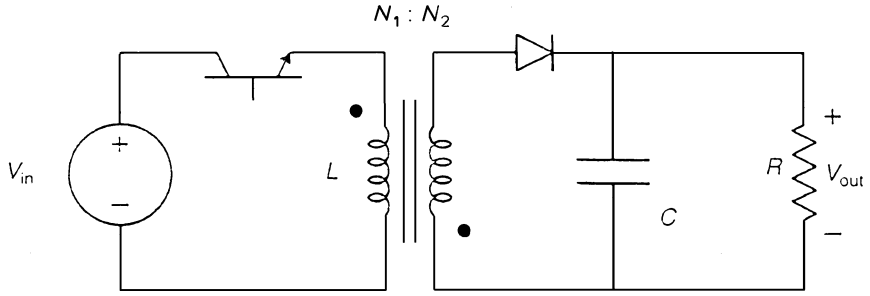

FIGURE 13.3.13 Flyback converter.

low as possible. An additional advantage appears when several different dc supplies are needed: if it is possible to use two separate coils on the magnetic core of the inductor, it should be just as reasonable to use three, four, or even more coils. Each can have its own turns ratio with mutual isolation. This is the basic for many types of multi-output dc power supplies.

One challenge with a flyback converter, as shown in Fig. 13.3.14, is the primary leakage inductance. During transistor turn-off, the leakage inductance energy must be removed. A capacitor or other snubber circuit is used to avoid damage to the active switch during turn-off.

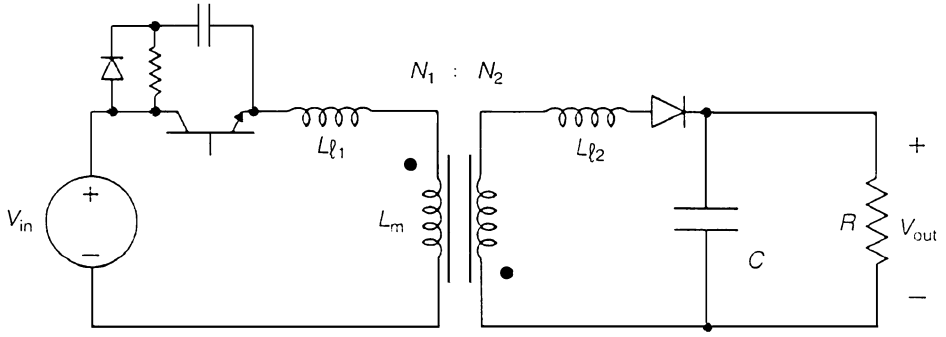

FIGURE 13.3.14 Leakage inductance issue in flyback converter.

FORWARD CONVERTERS

Coupled inductors in indirect converters, unlike transformers, must store energy and carry a net dc current. Basic buck and boost circuits lack a transfer source, so a coupled inductor will not give them isolation properties. Instead, a buck or boost converter can be augmented with a transformer, inserted at a location with only ac waveforms. Circuits based on this technique are called *forward converters.* A transformer can be added either by providing a *catch winding* tertiary or other circuitry for flux resetting, or by using an *ac link* arrangement. With either alternative, the objective is to avoid saturation because of dc current.

Figure 13.3.15 shows the catch-winding alternative in a buck converter. The tertiary allows the core flux to be reset while the transistor is off. Operation is as follows: the transistor carries the primary current i_1 and also the magnetizing current i_m when it is on. Voltage V_{in} is imposed on the primary, and the flux increases. When the transistor turns off, the magnetizing inductance will maintain the current flow in coil 1, such that $i_1 = -i_m$. The diode D_3 permits current $i_3 = i_m(N_1/N_3)$ to flow. The tertiary voltage v_3 flies back to $-V_{in}$, resetting the flux. If $N_1 = N_3$, the duty ratio of switch 1 must not exceed 50 percent so that there will be enough time to bring the flux down sufficiently. If it is desired to reach a higher duty ratio, the ratio N_1/N_3 must be at least $D_1/(1 - D_1)$.

With a catch winding, the primary carries a voltage $v_1 = -N_1/N_3$ after the transistor turns off. The transistor must be able to block $V_{in}(1 + N_1/N_3)$ to support this voltage. For power supplies, this can lead to extreme ratings. For example, an off-line supply designed for 350 V_{dc} input with $N_1/N_3 = 1.5$ to support duty ratios up to 60 percent requires a transistor rating of about 1000 V. This extreme voltage rating is an important drawback of the catch-winding approach.

The secondary voltage v_2 in this converter is positive whenever the transistor is on. The diode D_1 will exhibit the same switching function as the transistor, and the voltage across D_2 will be just like the diode voltage of a buck converter except for the turns ratio. The output and its average value will be

$$v_{out} = q_1 V_{in} \frac{N_2}{N_1}, \quad \langle v_{out} \rangle = D_1 V_{in} \frac{N_2}{N_1} \tag{14}$$

so this forward converter is termed a *buck-derived* circuit.

The ac link configuration comprises an inverter-rectifier cascade, such as the buck-derived half-bridge converter in Fig. 13.3.16. With adjustment of duty ratio, a waveform such as that shown in Fig. 13.3.17*a* is typically used as the inverter output. The signal has no dc component, and therefore a transformer can be used. Once full-wave rectification is performed, the result will be the square wave of Fig. 13.3.17*b*. The average output is

$$\langle v_{out} \rangle = 2aDV_{in} \tag{15}$$

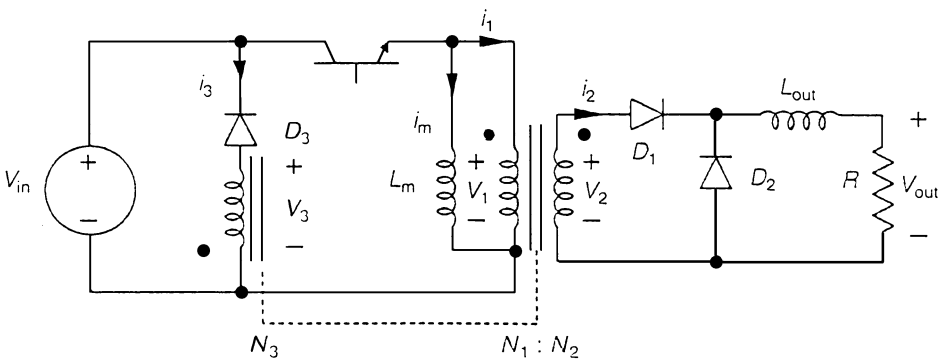

FIGURE 13.3.15 Catch-winding forward converter. (From Krein (1998), copyright © 1998 Oxford University Press. Inc., U.S.; used by permission.)

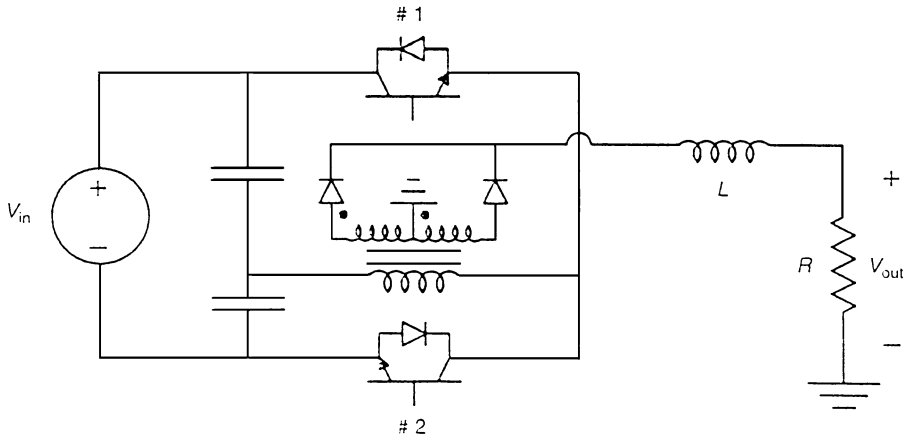

FIGURE 13.3.16 Half-bridge forward converter.

reflecting the fact that there are two output pulses during each switching period. No switch on the inverter side will be on more than 50 percent of each cycle, and the transistors block only V_{in} when off.

Four other forward converter topologies are shown in Fig. 13.3.18. The full bridge circuit in particular has been used successfully for power levels up to a few kilowatts. The others avoid the complexity of four active switches, although possibly with a penalty. For example, the *push-pull* converter in the figure has the important advantage that both switch gate drives share a common reference node with V_{in}. Its drawback is that the transistor must block $2V_{in}$ when off, because of an autotransformer effect of the center-tapped primary. The topologies are compared in Table 13.3.5.

The full-bridge converter perhaps offers the most straightforward operation. The switches always provide a path for magnetizing and leakage inductance currents, and circuit behavior is affected little by these extra inductances. In other circuits, these inductances are a significant complicating factor. For example, magnetizing inductance can turn on the primary-side diodes in a half-bridge converter, altering the operation of duty

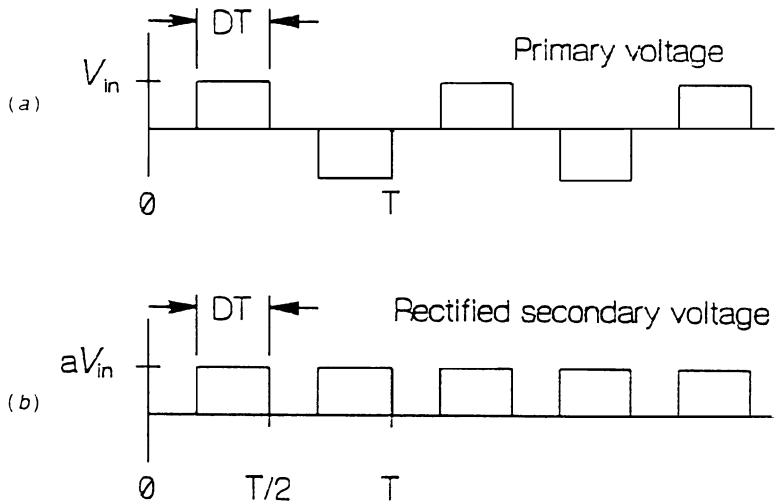

FIGURE 13.3.17 Typical waveforms in inverter-rectifier cascade. (From Krein (1998), copyright © 1998 Oxford University Press, Inc., New York, U.S.; used by permission.)

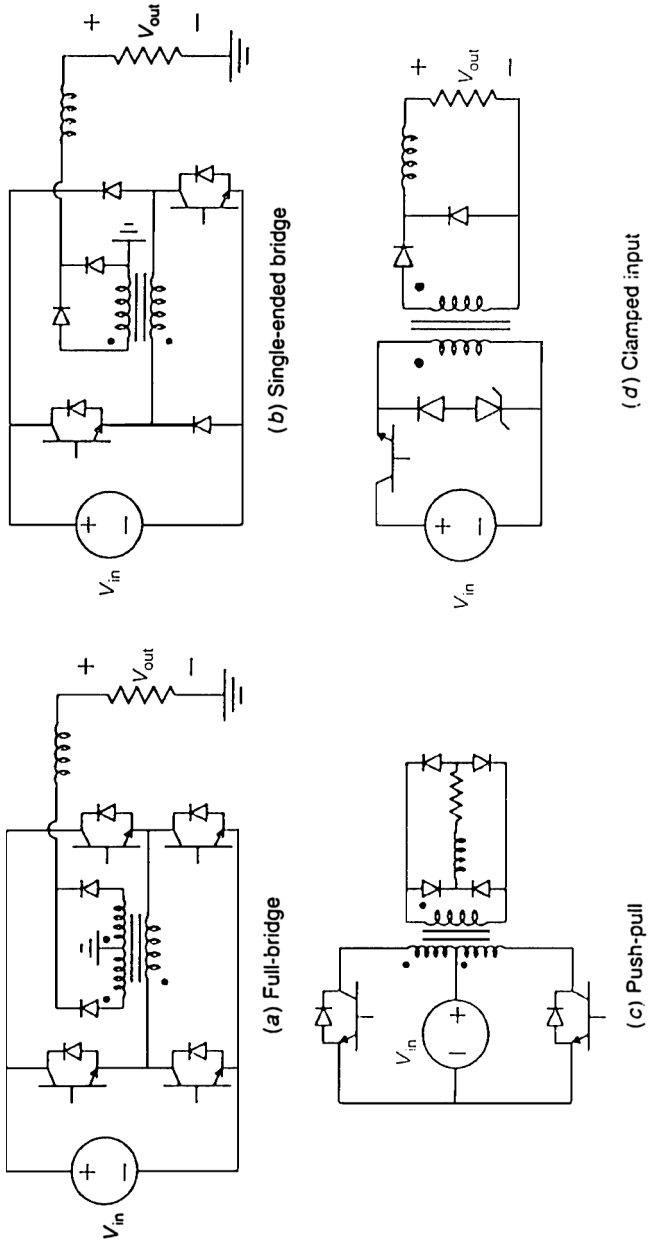

FIGURE 13.3.18 Four alternative forward converter topologies.

TABLE 13.3.5 Characteristics of Common Buck-Derived Forward Converters

Forward Converter Topology	Transistor Off-State Voltage	Flux Behavior	Comments
Full-bridge	V_{in}	Full variation from $-\phi_{max}$ to $+\phi_{max}$	Preferred for high power levels by many designers
Half-bridge	V_{in}	Full variation	Capacitive divider avoids any dc offset in flux. Preferred at moderate power levels by many designers
Single-ended	V_{in}	Variation only between 0 and $+\phi_{max}$	Less effective use of core, but only two transistors
Push-pull	$2V_{in}$	Full variation	Common-ground gate drives. Timing errors can bias the flux and drive the core into saturation
Clamp	$V_{in} + V_z$	Variation only between 0 and $+\phi_{max}$	Similar to catch winding circuit, except that energy in magnetizing inductance is lost

ratio control. Leakage inductance is a problem in the push-pull circuit, particularly since both transistors must be off to establish the portion of time when no energy is transferred from input to output. Snubbers are necessary parts of this converter. These issues are discussed at length in at least one text (Kassakian, Schlecht, and Verghese, 1991).

The boost converter also supports forward converter designs. A boost-derived push-pull forward converter is shown in Fig. 13.3.19. Like the boost converter, this circuit has an output higher than the input but now with a turns ratio. The operation differs from a buck-derived converter in an important way: both transistors must turn on to establish the time interval when no energy flows from input to output. In effect, each transistor has a *minimum* duty ratio of 50 percent, and control is provided by allowing the switching functions to overlap. The output duty ratio associated with each diode becomes $1 - D$, where D is the duty ratio of one of the transistors over a full switching period. The output voltage is

$$V_{out} = \frac{N_2}{N_1}\frac{V_{in}}{2(1-D)} \tag{16}$$

The other forward converter arrangements also have boost-derived counterparts.

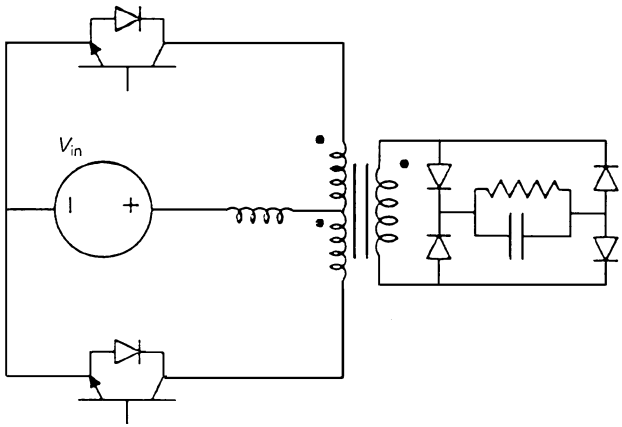

FIGURE 13.3.19 Boost-derived push-pull converter.

In each of the converters discussed so far, it has been assumed that energy storage components have been sufficiently large to be treated as approximate current or voltage sources. This is not always the case. If values of inductance or capacitance are chosen below a certain value, the current or voltage, respectively, will reach zero when energy is extracted. This creates *discontinuous mode* behavior in a dc-dc converter. The values of L and C sufficient to ensure that this does not occur are termed *critical inductance* and *critical capacitance*, respectively. The usual effect of subcritical inductance is that all switches on the converter turn off together for a time. Subcritical capacitance in a boost-buck converter creates times when all switches are on together.

In discontinuous mode, converter load regulation degrades, and closed-loop output control becomes essential. However, discontinuous mode can be helpful in certain situations. It implies fast response times since there is no extra time required for energy buildup. It provides an additional degree of freedom—the extra configuration when all switches are off or on—for control purposes.

Discontinuous mode behavior can be analyzed through the techniques of this subsection, with the additional constraint that all energy in the storage element is removed during each switching period. The literature (Mitchell, 1988; Mohan, Undeland, and Robbins, 1995) provides a detailed analysis, including computation of critical inductance and capacitance.

RESONANT DC-DC CONVERSION TECHNIQUES

The dc-dc converters examined thus far operate their switches in a *square-wave* or *hard-switched* mode. Switch action is strictly a function of time. Since switch action requires finite time, hard-switched operation produces significant switching loss. Resonant techniques for *soft switching* attempt to maintain voltages or currents at low values during switch commutation, thereby reducing losses. *Zero-current switching* (ZCS) or *zero-voltage switching* (ZVS) can be performed in dc converters by establishing resonant combinations. Resonant approaches for soft switching are discussed extensively in Kazimierczuk and Czarkowski (1995).

The SCR supports natural zero-current switching, since turn-off corresponds to a current zero crossing. A basic arrangement, given in Fig. 13.3.20, is often used as the basis for soft switching in transistor-based dc-dc converters as well as for inverters. Starting from rest, the top SCR is triggered. This applies a step dc voltage to the RLC set. If the quality factor of the RLC set is more than $\frac{1}{2}$, the current is underdamped, and will oscillate. When the current swings back to zero, the SCR will turn off with low loss. After that point, the lower SCR can be triggered for the negative half-cycle.

The SCR inverter represents a *series resonant switch* configuration and provides ZCS action. However, SCRs are not appropriate for high-frequency dc-dc conversion because of their long switching times and control limitations. The circuit of Fig. 13.3.21 shows an interesting arrangement for dc-dc conversion, similar to the SCR circuit, but based on a fast MOSFET. In this case, an inductor and a capacitor have been added to a standard buck converter to alter the transistor action. Circuit behavior will depend on the relative values.

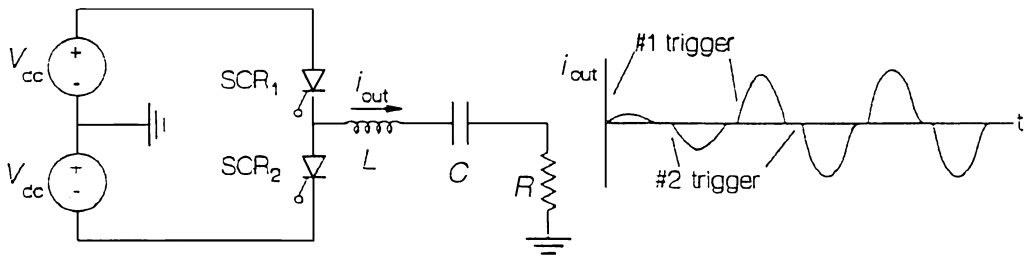

FIGURE 13.3.20 SCR soft-switching inverter. (From Krein (1998), copyright © 1998 Oxford University Press, Inc., U.S.; used by permission.)

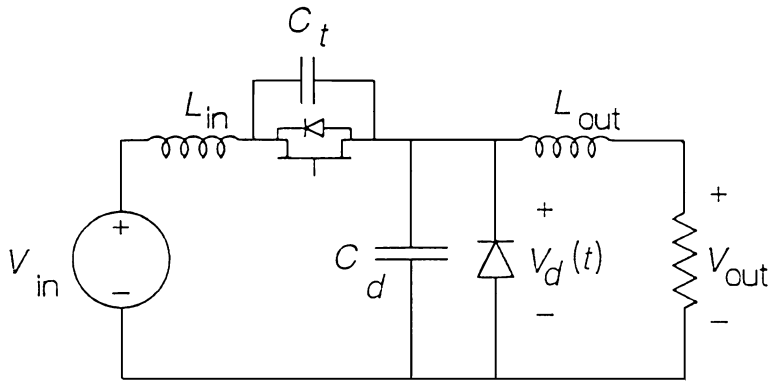

FIGURE 13.3.21 A soft-switching arrangement for a buck converter.

If the capacitor C_t is large, its behavior during the transistor's off interval will introduce opportunities for resonant switching. In this case, the basic circuit action is as follows:

- When the transistor turns off, the input voltage excites the pair L_{in} and C_t. The input inductor current begins to oscillate with the capacitor voltage. The capacitor can be used to keep the transistor voltage low as it turns off.
- The capacitor voltage swings well above V_{in}, and the main output diode turns on.

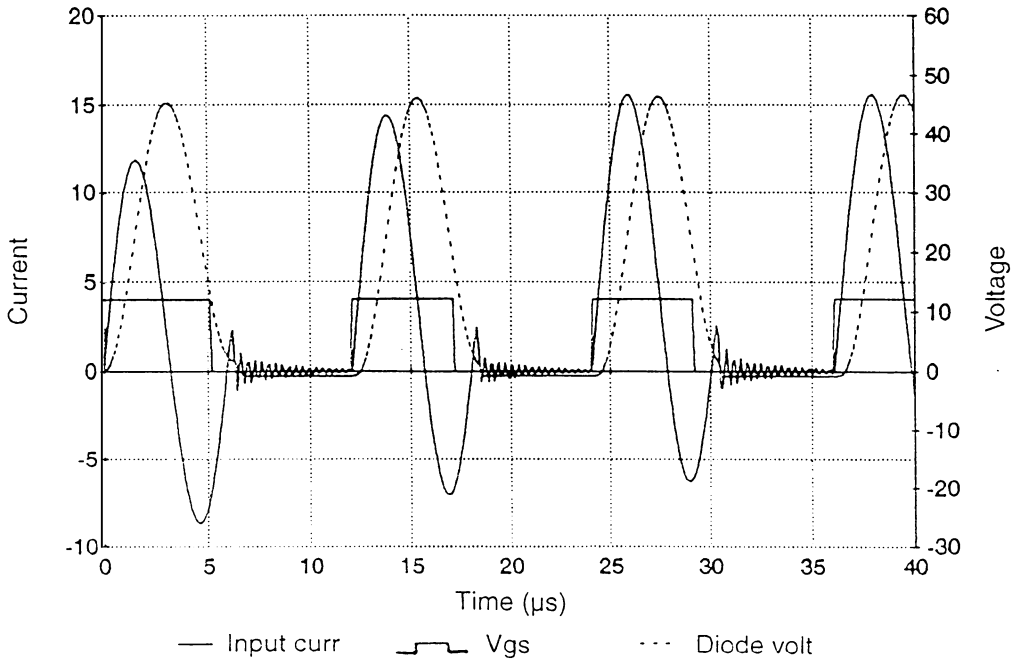

FIGURE 13.3.22 Input current and diode voltage in a resonant buck converter. (From Krein (1998), copyright © 1998 Oxford University Press. Inc., U.S.; used by permission.)

- The capacitor voltage swings back down. There might be an opportunity for zero-voltage turn-on of the transistor when the capacitor voltage swings back to zero.

This represents ZVS action.

When the transistor is on and the main diode is off, the input inductor forms a resonant pair with C_d. This pair provides an opportunity for zero-current switching at transistor turn-off, very much like the zero-current switch action in the SCR inverter. The action is as follows in this case:

- When the transistor is turned on, L_{in} limits the rate of rise of current. The diode remains on initially, and the current builds up linearly because V_{in} appears across the inductor.
- When the current arises to the level I_{out}, the diode shuts off and the transistor carries the full current. The pair L_{in} and C_d form a resonant LC pair, and the current oscillates.
- The current rises above I_{out} because of resonant action, but then swings back down toward the origin.
- When the current swings negative, the transistor's reverse body diode begins to conduct, and the gate signal can be shut off. When the current tries to swing positive again, the switch will turn off.
- The transistor on-time is determined by the resonant frequency and the average output current.

Figure 13.3.22 shows the input current and main diode voltage for a choice of parameters that gives ZCS action in the circuit of Fig. 13.3.21.

Resonant action changes the basic control characteristics substantially. The gate control in both ZVS and ZCS circuits must be properly synchronized to match the desired resonance characteristics. This means that pulse-width modulation is not a useful control option. Instead, resonant dc converters are adjusted by changing the switching frequency—in effect setting the portion of time during which resonant action is permitted. In a ZCS circuit, for example, the average output voltage can be reduced by dropping the gate pulse frequency.

In general, ZCS or ZVS action is very beneficial for loss reduction. Lower switching losses permit higher switching frequencies, which in turn allow smaller energy storage elements to be used for converter design. Without resonant action, it is difficult to operate a dc-dc converter above perhaps 1 MHz. Resonant designs have been tested to frequencies as high as 10 MHz (Tabisz, Gradzki, and Lee, 1989). Designs even up to 100 MHz have been considered for aerospace applications. In principle, resonance provides size reduction of more than an order of magnitude compared to the best nonresonant designs. However, there is one important drawback: The oscillatory behavior substantially increases the on-state currents and off-state voltages that a switch must handle. Under some circumstances, the switching loss improvements of resonance are offset by the extra on-state losses caused by current overshoot. There are magnetic techniques to help mitigate this issue (Erickson, Hernandez, and Witulski, 1989), but they add complexity to the overall conversion system. The switching loss trade-offs tend to favor resonant designs at relatively low voltage and current levels. More sophisticated resonant design approaches, based on Class E methods (Kasimierczuk and Czarkowski, 1995), can further reduce losses.

Example: Input-output relationships in a ZCS dc-dc converter.

Let us explore ZCS switching in a dc-dc converter and analyze the results. The approach in this example follows an analysis in Kassakian, Schlecht, and Verghese (1991). The circuit in Fig. 13.3.21 is the focus, with C_t selected to be small and L_{out} selected to be large. Parameters are $V_{in} = 24$ V, $C_t = 200$ pF, $L_{in} = 2$ μH, $C_d = 0.5$ μF, $L_{out} = 50$ μH, and a 10-Ω load in parallel with an 8 μF filter capacitor. The FET is supplied with a 5-μs pulse with a period of 12 μs.

In periodic steady-state operation, the inductor L_{out} will carry a substantial current. The output time constant is long enough to ensure that the current will not change very much. As a result, the output inductor can be modelled as a current source, with value I_{out}. The diode provides a current path while the transistor is off. Consider the moment at which the transistor turns on. Since the current in L_{in} cannot change instantly, the diode remains on for a time while the input current rises. We have

$$i_{in}(t) = \frac{V_{in}}{L_{in}} t \tag{17}$$

until the current i_{in} reaches the value I_{out}. At the moment $t_{on} = I_{out}L_{in}/V_{in}$, the diode current reaches zero and the diode turns off. The input circuit becomes an undamped resonant tank determined by L_{in} and C_d. For C_d, circuit laws require

$$V_{in} - v_{Cd}(t) - L_{in}C_d\ddot{v}_{Cd}(t) = 0, \qquad v_{Cd}(t_{on}) = 0, \qquad v_{Cd}(t_{on}) = 0 \tag{18}$$

This has the solution

$$v_{Cd}(t) = V_{in}\{1 - \cos[\omega_r(t - t_{on})]\}, \qquad \text{where } \omega_r = \frac{1}{\sqrt{L_{in}C_d}} \tag{19}$$

For the input current, the corresponding solution is

$$i_{in}(t) = I_{out} + \frac{V_{in}\sin[\omega_r(t - t_{on})]}{Z_c}, \qquad \text{where } Z_c = \sqrt{\frac{L_{in}}{C_d}} \tag{20}$$

With the selected parameters, $Z_c = 2\ \Omega$ and $\omega_r = 10^6$ rad/s, corresponding to about 160 kHz. The inductor current will cross zero again a bit more than one half-period after t_{on}. In this example, I_{out} might be on the order of 1 A, so t_{on} corresponds to only about 83 ns. The half-period of the resonant ring signal will be about 3.2 μs. Therefore, a 5-μs gate pulse should ensure that the transistor remains on until the zero crossing point.

When the current crosses zero, the FET turns off, but its reverse body diode turns on and maintains negative flow for approximately another half-cycle, at approximately $t = 6.4\ \mu$s. Since the gate signal is removed between the zero crossings, the FET and its diode will both turn off at the second zero crossing. Figure 13.3.22 is a SPICE simulation for these circuit parameters. The ZCS action should be clear: since the gate pulse is removed while the FET's reverse body diode is active, the complete FET will shut off at a rising current zero crossing. The shut-off point t_{off} is determined by

$$0 = I_{out} + \frac{V_{in}\sin[\omega_r(t_{off} - t_{on})]}{Z_c}, \qquad \omega_r(t_{off} - t_{on}) = \sin^{-1}\left(\frac{-I_{out}Z}{V_{in}}\right) \tag{21}$$

In solving this expression, it is crucial to be careful about the quadrant for $\sin^{-1}(x)$. The rising zero crossing is sought.

Once the FET is off, capacitor C_d carries the full current I_{out}. The voltage $v_{Cd}(t)$ will fall quickly with slope $-I_{out}/C_d$ until the diode becomes forward biased and turns on. The voltage $v_{Cd}(t)$ is of special interest, since the output is $V_{out} = \langle v_{Cd}(t)\rangle$. The average is

$$\langle v_{Cd}\rangle = \frac{1}{T}\left(\int_{t_{on}}^{t_{off}} V_{in}(1 - \cos[\omega_r(t - t_{on})])\,dt + \int_{t_{off}}^{t_{(diode\,on)}} v_{Cd}(t_{off}) - \frac{I_{out}}{C_d}t\,dt\right) \tag{22}$$

The second integral is a triangular area $\frac{1}{2}v_{Cd}(t_{off})^2(C_d/I_{out})$. For $I_{out} \approx 1$ A, the time $t_{off} - t_{on}$ can be found from Eq. (21) to be 6.20 μs. The value $v_{Cd}(t_{off})$ is therefore 83 mV. The average value is $V_{out} = 12.6$ V. This corresponds to $I_{out} = 1.26$ A. In this example, the average value comes out very close to

$$V_{out} = \frac{4.8 \times 10^{-6}\pi}{T} \tag{23}$$

for $T > 6.4\ \mu$s. The solution comes out quite evenly because the current zero-crossing times nearly match those of the resonant sine wave.

In the ZCS circuit, the on time of the transistor is determined by resonant action, provided the gate pulse turns off during a time window when reverse current is flowing through the device's diode. The gate pulses need to have fixed duration to tune the circuit, but the pulse period can be altered to adjust the output voltage.

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