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CHAPTER 13.4
INVERTERS

David A. Torrey

INTRODUCTION

Inverters are used to convert dc into ac. This is accomplished through alternating application of the source to the load, achieved through proper use of controllable switches. This section reviews the basic principles of inverter circuits and their control. Four major applications of inverter circuits are also reviewed.

Both voltage- and current-source inverters are used in practice. The trend, however, is to use voltage-source inverters for the vast majority of applications. Current-source inverters are still used at extremely high power levels, though voltage-source inverters are gradually filling even these applications. Because of the dominance of voltage-source inverters, this section focuses exclusively on this type of inverter.

There are many issues involved in the design of an inverter. The more prominent issues involve the interactions among the power circuit, the source, the load, and the control. Other subtle issues involve the control of parasitics and the protection of controllable switches through the use of snubber and clamp circuits, and the juxtaposition of controller speed with the desire for increased switching frequency, while maintaining high efficiency.

The technical literature contains abundant information on inverters. A set of technical papers is found in Bose (1992). In addition to technical papers, most power electronics textbooks have a section on inverters (Mohan, Undeland, and Robbins, 1995; Kassakian, Schlecht, and Verghese, 1991; Krein, 1998).

AN INVERTER PHASE-LEG

An inverter phase-leg is shown in Fig. 13.4.1. It comprises two fully controllable switches and two diodes in antiparallel to the controllable switches. This phase-leg is placed in parallel with a voltage source. The center of the phase-leg is taken to the load. The basic circuit shown in Fig. 13.4.1 is usually augmented with a snubber circuit or clamp to shape the switching locus of the controllable switches. Insulated gate bipolar transistors (IGBTs) are shown as the controllable switches in Fig. 13.4.1. While the IGBT finds significant application in inverters, any fully controllable device, such as an FET or a GTO, may be used in its place; see Chapter 13.1 for a description of the fully controllable switches that can be used in an inverter.

Basic Principles. In the phase-leg of Fig. 13.4.1, there are two restrictions on the use of the controllable switches. First, at most one controllable switch may be conducting at any time. The dc supply is shorted if both switches are conducting. In practice, one switch is turned off before the other is turned on. This blanking time, also known as dead time, compensates for the tendency of power devices to turn on faster than they turn off. Second, at least one controllable switch (or an associated diode) must be on at all times if the load current is to be nonzero.

If the upper switch is conducting, the load is connected to the positive side of V_{dc}. If the lower switch is conducting, the load is connected to the negative side of V_{dc}. It follows that the voltage applied to the load will, on

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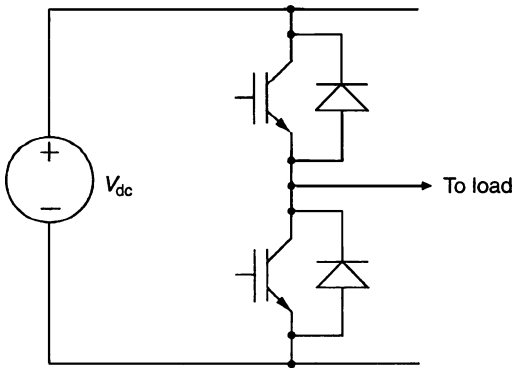

FIGURE 13.4.1 An inverter phase-leg.

average, fall somewhere between 0 and V_{dc}. When the phase-leg of Fig. 13.4.1 is used with one or more additional phase legs, the load voltage can be made to alternate. The details of how it alternates is the responsibility of the controller.

The peak voltage seen by each switch is the total dc voltage across the phase-leg. This is determined by recognizing that one of the two switches is always conducting. The peak current that must be supported by each switch is the peak current of the load. Under balanced control of the two switches, each switch must support the same peak current; each diode must support the same peak current as the switches.

In an effort to improve the efficiency and spectral performance of inverters, the use of inverters with a resonant dc link has been reported in the technical literature (Divan, 1989; Murai and Lipo, 1988). Through periodic resonance of the dc bus voltage to zero, or the dc bus current to zero, the inverter switches can change states in synchronism with these zero crossings in order to reduce the switching losses in the power devices. Figure 13.4.2 shows a schematic for the basic resonant dc link converter (Divan, 1989). The resonance of L_r and C_r forces the bus voltage (the voltage applied to the controllable switches) to swing between zero and $2V_{dc}$. The inverter switches change states when the voltage across C_r is zero. It is often necessary to hold the bus voltage at zero for a brief time to ensure that sufficient energy has been put into L_r to force resonance back to zero voltage across C_r. The bus can be clamped at zero voltage by turning on both switches in an inverter phase-leg. One drawback of the resonant dc link is the increased voltage or current imposed on the power devices. Auxiliary clamp circuits have been implemented to minimize this drawback (Divan and Skibinski, 1989; He and Mohan, 1991; Simonelli and Torrey, 1994). The control of a resonant link inverter is complicated by the simultaneous need to manage energy flow to the load while managing energy in the resonant link.

Snubber Circuits and Clamps. Snubber circuits are used to control the voltage across and the current through a controllable switch as that device is turning on or off. A complete snubber will typically limit the rate of rise in current as the device is turning on and limit the rate of rise in voltage as the device is turning off. Additional circuit components are used to accomplish this shaping of the switching locus. Figure 13.4.3 shows three snubber circuits that are used with inverter legs, one of which has auxiliary switches (McMurray, 1987; McMurray, 1989;

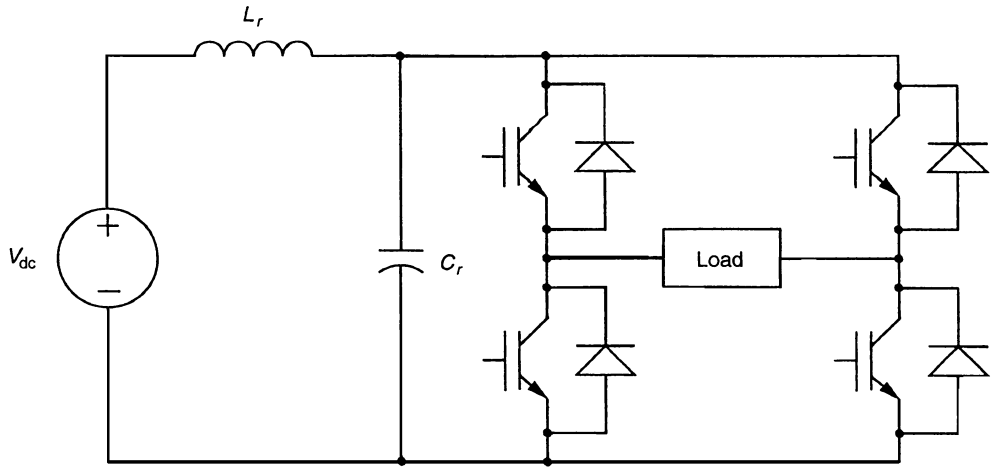

FIGURE 13.4.2 A basic resonant dc link inverter system.

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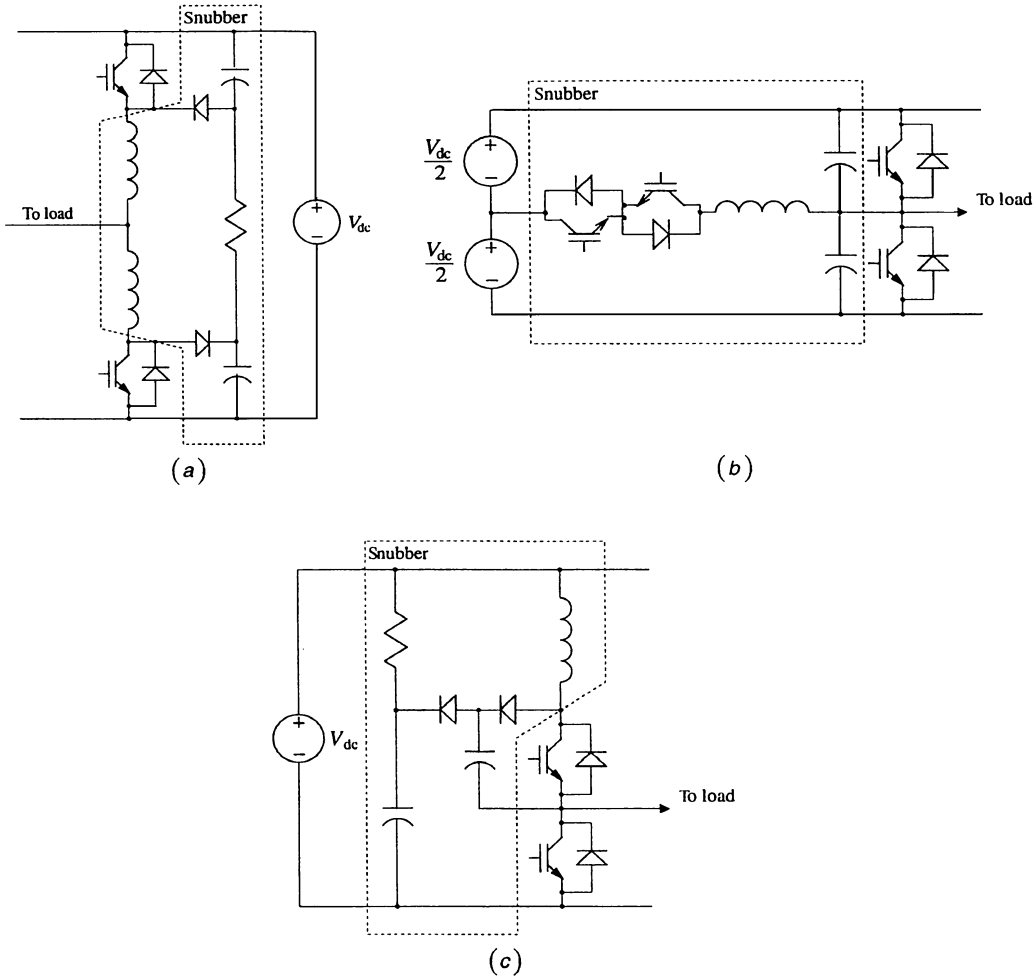

FIGURE 13.4.3 A number of snubber circuits for an inverter phase-leg: (*a*) a McMurray snubber (McMurray, 1987); (*b*) a resonant snubber with auxilliary switches (McMurray, 1989); and (*c*) the Undeland snubber (Undeland, 1976).

Undeland, 1976). Snubber circuits become increasingly important as the power rating of the inverter increases, where the additional cost of small auxiliary devices is justified by improved efficiency and spectral performance.

Clamps differ from snubbers in that a clamp is used only to limit a switch variable, usually the voltage, to some maximum value. The clamp does not dictate how quickly this maximum value is attained. Figure 13.4.4 shows three clamp circuits that are commonly used with inverter legs. The clamp circuits generally become more complex with increasing power level.

Interfacing to Controllable Switches. The interface to the controllable switches within the inverter phase-leg of Fig. 13.4.2 requires careful attention. Power semiconductor devices are generally controlled by manipulating the control terminal, usually relative to one of the power terminals. For example, Figure 13.4.2 shows insulated gate bipolar transistors (IGBTs) as the controllable switches. These devices are turned on and off through the voltage level applied to the gate relative to the emitter. Because the emitter of the upper IGBT moves around, the control of the upper IGBT must accommodate this movement. The emitter voltage of the upper IGBT moves from the positive side of the dc bus when the IGBT is conducting to the negative side of the dc bus when

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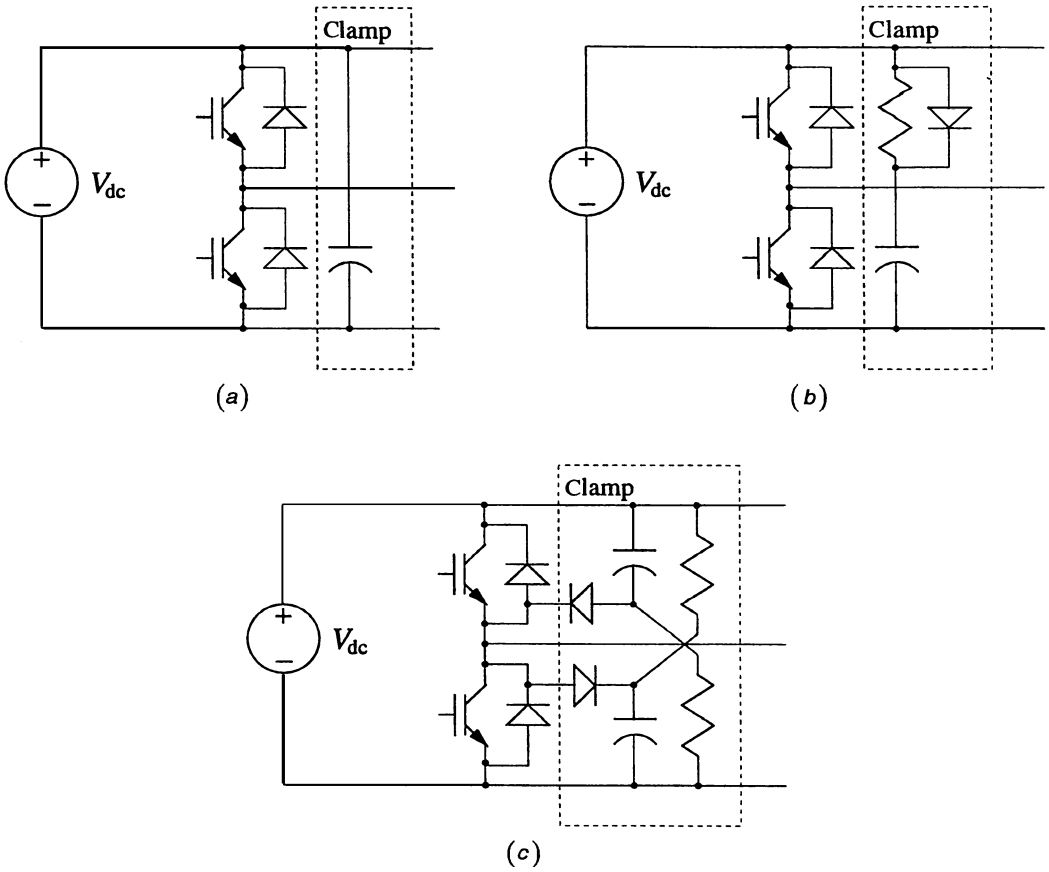

FIGURE 13.4.4 Clamp circuits for an inverter phase-leg: (*a*) low power (~ 50 A); (*b*) medium power (~ 200 A); and (*c*) high power (~300 A).

the lower IGBT is conducting. The circuit responsible for turning the power semiconductor on and off as commanded by a controller is usually known as a gate-drive circuit. Some gate-drive circuits incorporate protection mechanisms for over current or over temperature.

There are a number of approaches that are used to control the semiconductor devices within the inverter. The choice among these approaches is often dictated by the power levels involved, the switching frequency supported by the switches, and the preference of the designer, among others. It is possible to purchase high-voltage integrated circuits (HVICs) that perform the level shifting necessary to take a logic signal referenced to the negative side of the dc bus and control the upper controllable switch in the phase-leg. This approach is generally limited to applications where the controllable switches do not require a negative bias to hold them in the blocking state. High-frequency applications may use transformer-coupled gate drives that are insensitive to the common-mode voltage between the primary and secondary. This approach runs into problems at lower frequencies because the size of the transformer core begins to get large. High-power applications may use optocouplers to optically couple the control information to the gate drive, where the gate drive is supported by an isolated power supply. Often the power supply is the dominant factor in the overall cost of the gate drive.

Figure 13.4.5*a* shows how an HVIC is interfaced to a phase-leg. The capacitors are used as local power supplies for the upper and lower gate drives. In this implementation, the upper capacitor is charged through the diode while the lower switch is conducting. Figure 13.4.5*b* shows a transformer-coupled gate drive for a high-frequency application (Internatonal Rectifier). It is important to design a mechanism for resetting the core in

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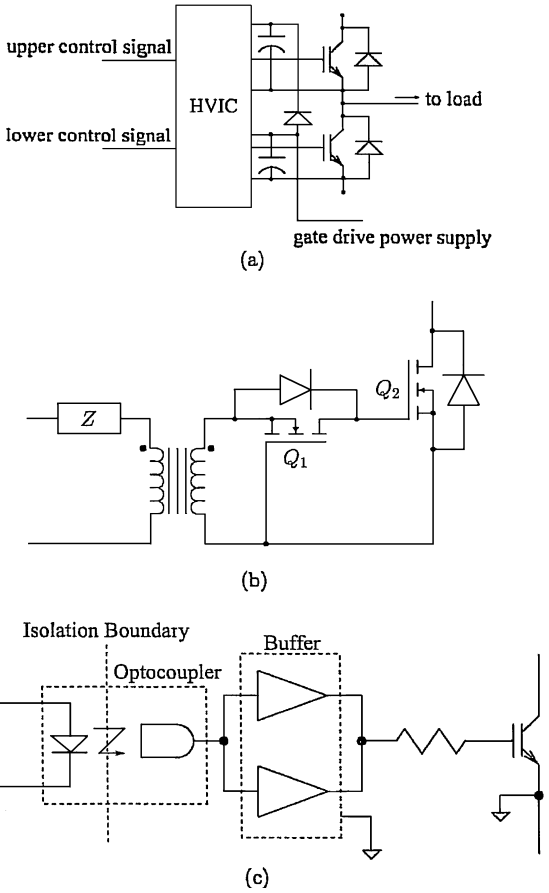

FIGURE 13.4.5 Three common approaches to interfacing to controllable switches: (a) the use of an HVIC; (b) the use of transformer coupling; and (c) the use of an optocoupler.

a transformer-coupled gate drive. In Fig. 13.4.5*b*, the core is reset by driving the transformer primary with a bipolar voltage that provides sufficient volt-seconds to drive the transformer into saturation. This need for core reset may place unacceptable limitations on the duty ratio of the switches for some applications. Figure 13.4.5*c* shows the use of an optocoupler to provide isolation of the control signal going to the gate drive. The isolated power supply required to support the use of the optocoupler is not shown.

SINGLE-PHASE INVERTERS

There are two ways to form a single-phase inverter. The first way is shown in Fig. 13.4.6, where the phase leg of Fig. 13.4.1 is used to control the voltage applied to one side of the load. The other side of the load is connected to the common node of two voltage sources. The half-bridge inverter of Fig. 13.4.6 applies positive voltage to the load when the upper switch is conducting and negative voltage to the load when the lower switch is conducting. It is not possible for the half-bridge inverter to apply zero voltage to the load.

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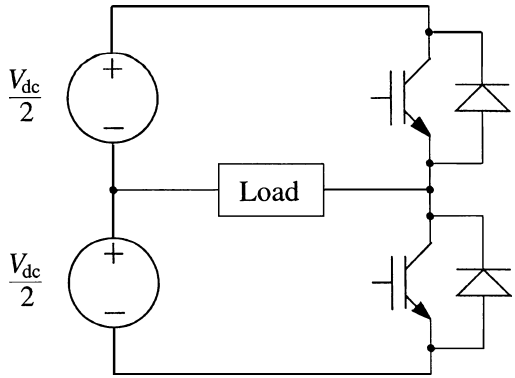

FIGURE 13.4.6 A single-phase inverter using one phase-leg and two dc voltage sources.

A single-phase inverter is also formed by placing the load between two inverter phase-legs, as shown in Fig. 13.4.7. This circuit is often referred to as a full- or H-bridge inverter. Through appropriate control of the inverter switches, positive, negative, and zero voltage can be applied to the load. The zero voltage state is achieved by having both upper switches, or both lower switches, conducting at the same time. Note that this state requires one switch and one diode to be supporting the load current.

THREE-PHASE INVERTERS

A three-phase inverter is used to support both Δ- and Y-connected three-phase loads. The three-phase inverter topology can be derived by using three single-phase full-bridge inverters, with each inverter supporting one phase of the load. Upon careful examination of the resulting connection of the 12 controllable switches with the load, it is seen that there are six redundant switches because phase-legs are connected in parallel. Elimination of the six redundant switches yields the topology shown in Fig. 13.4.8.

There are six switches in the three-phase inverter topology of Fig. 13.4.8. Considering all combinations of the switch states, there are seven possible voltages that may be applied to the load; the cases of all three upper switches being closed and all three lower switches being closed are functionally indistinguishable. The controller is responsible for applying the appropriate voltage to the load according to the method used for synthesizing the output voltage.

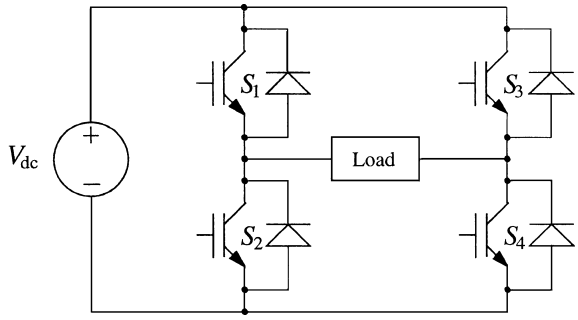

FIGURE 13.4.7 A single-phase inverter using two phase-legs and one dc voltage source.

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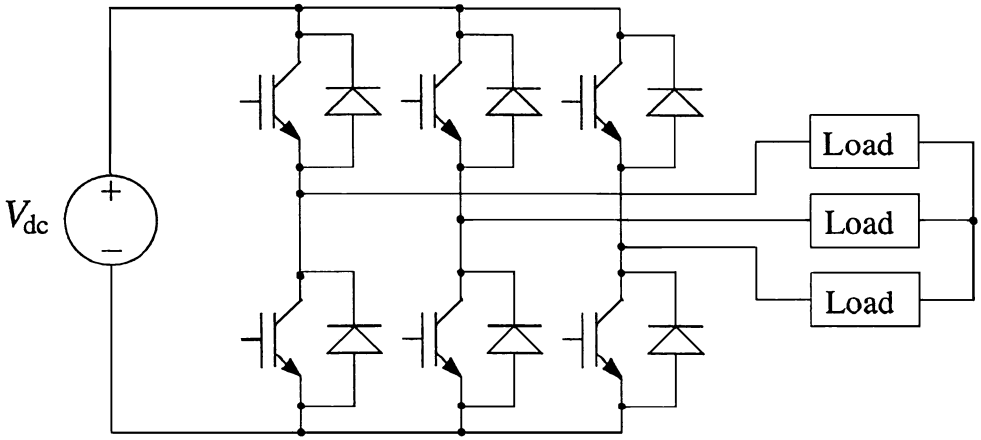

FIGURE 13.4.8 The three-phase inverter topology.

MULTILEVEL INVERTERS

The three-phase inverter of Fig. 13.4.8 applies one of two voltages to each output load terminal. The output voltage is V_{dc} when the upper switch is conducting, and it is zero when the lower switch is conducting. Accordingly, this inverter could be called a two-level inverter. Multilevel inverters are based on extending this concept and are becoming the inverter of choice for higher-voltage and higher-power applications. The discussion here focuses on a three-level inverter; extensions to five or more levels can be found in the technical literature (Lai and Peng, 1996; Peng, 2001).

Among their advantages, multilevel inverters allow the synthesis of voltage waveforms that have a lower harmonic content than a two-level inverter for the same switching frequency. This is because each output terminal is switched among at least three voltages, not just two. In addition, the input dc bus voltage can be higher because multiple devices are connected in series to support the full bus voltage.

Figure 13.4.9 shows one phase-leg of a three-level inverter. In the three-level inverter the dc bus is partitioned into two equal levels of $V_{dc}/2$. The four controllable switches with antiparallel diodes, S_1 through S_4, are connected in series to form a phase-leg. In addition, two steering diodes, D_5 and D_6, are used to support current flow to and from the midpoint of the dc bus. Additional phase-legs would be connected in parallel across the full dc bus.

Operation of four switches is used to connect the load output terminal to either V_{dc}, $V_{dc}/2$, or zero. Switches S_1 and S_2 are used to connect the load to V_{dc}, switches S_2 and S_3 are used to connect the load to $V_{dc}/2$, and switches S_3 and S_4 are used to connect the load to zero.

While switches S_1 and S_2 are conducting, diode D_6 ensures that the voltage across switch S_4 does not exceed $V_{dc}/2$. Similarly, when switches S_3 and S_4 are conducting, diode D_5 ensures that the voltage across switch S_1 does not exceed $V_{dc}/2$. While switches S_2 and S_3 are conducting, the voltage across both S_1 and S_4 is clamped at $V_{dc}/2$; diode D_5 and switch S_2 support positive load current, while diode D_6 and switch S_3 support negative load current.

A three-phase, three-level inverter provides substantially increased flexibility for voltage synthesis over the conventional three-phase inverter of Fig. 13.4.8. The three-phase inverter of Fig. 13.4.8 offers eight switch combinations that support seven different voltage combinations among the three output terminals. A three-phase, three-level inverter offers 27 switch combinations, supporting 19 different voltage combinations among the three output terminals. Further, the increased redundancy of certain voltages provides additional degrees of freedom in designing the voltage synthesis algorithm. These additional degrees of freedom could, for example, be used to minimize the common mode voltage between the three outputs.

Issues within the design and control of the multilevel inverter include the dynamic balancing of the voltages within each level of the dc bus and the switching patterns needed to best synthesize the desired output voltage. One would expect that symmetric operation of the phase-leg should be sufficient for maintaining balanced voltages across each level of the dc bus. The variation in capacitor values, however, will cause the midpoint of the

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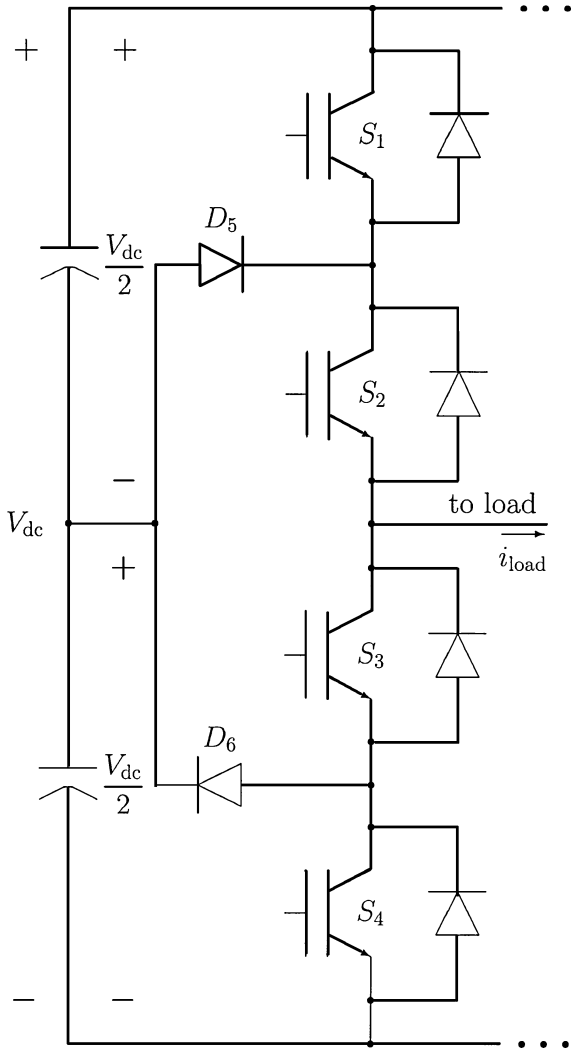

FIGURE 13.4.9 A phase-leg for a three-level inverter.

dc bus to move to a voltage other than $V_{dc}/2$ for symmetric load currents. This shift in voltage will have repercussions on the synthesis of the output voltage.

VOLTAGE WAVEFORM SYNTHESIS TECHNIQUES

There are three principal ways to synthesize the output voltage waveform in an inverter: harmonic elimination, harmonic cancellation, and pulse-width modulation. The synthesis technique that is applied is generally driven by consideration of the required output quality, the inverter power rating (which is closely tied to the speed of the controllable switches), the computational power of the available controller, and the acceptable cost of the inverter. This subsection reviews some of the common techniques used to synthesize the inverter output voltage.

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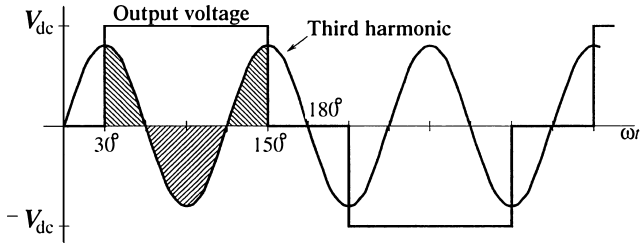

FIGURE 13.4.10 Elimination of the third harmonic.

Harmonic Elimination. Harmonic elimination implies that the output waveform shape is controlled to be free of specific harmonics through the selection of switch transitions (Patel and Hoft, 1973; Patel and Hoft, 1974). That is, the switches are controlled so that one or more harmonics are never generated. This is often accomplished by notching the output waveform. Examples of harmonic elimination are shown in Figs. 13.4.10 and 13.4.11, which respectively show the elimination of only the third harmonic and simultaneous elimination of the third and fifth harmonics from the output of a single-phase inverter.

As suggested by Figs. 13.4.10 and 13.4.11, additional switch transitions must be inserted in the output waveform for each harmonic that is to be eliminated. As the number of notches gets very large, the output voltage waveform begins to resemble something which could be produced by pulse-width modulation. Harmonic

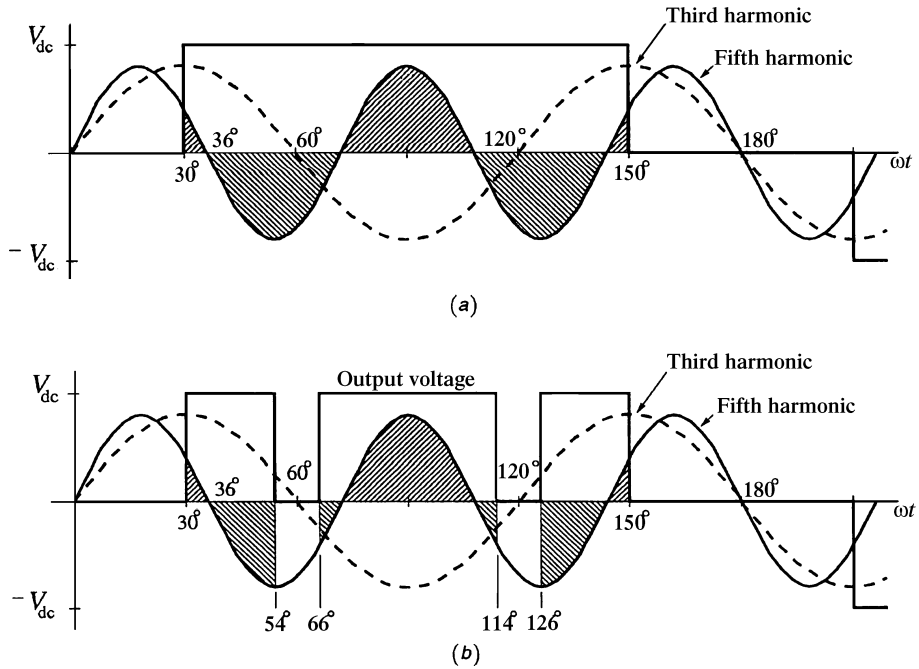

FIGURE 13.4.11 Simultaneous elimination of the third and fifth harmonics: (*a*) shows the fifth harmonic superimposed on the waveform of Fig. 13.4.10: (*b*) shows the switch transitions introduced to eliminate the fifth harmonic without reintroducing the third harmonic.

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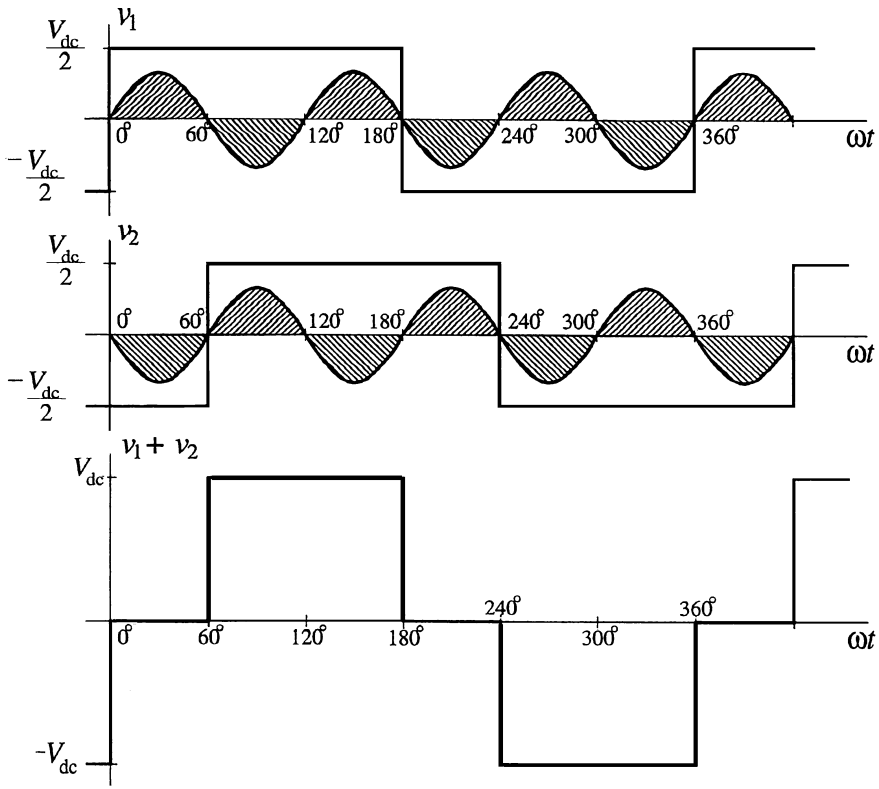

FIGURE 13.4.12 The superposition of two waveforms to cancel the third harmonic.

elimination is sometimes referred to as programmed PWM because the switching angles of the output voltage are programmed according to the intended harmonic content (Enjeti, Ziogas, and Lindsay, 1985).

Harmonic Cancellation. Harmonic cancellation uses the superposition of two or more waveforms to cancel undesired harmonics (Kassakian, Schlecht, and Verghese, 1991). Figure 13.4.12 shows how two waveforms that contain the third harmonic may be phase-shifted and superimposed in order to create a waveform that is free of the third harmonic. The circuit of Fig. 13.4.13 can be used to synthesize the waveform of Fig. 13.4.12.

By combining harmonic cancellation and harmonic elimination, it is possible to create relatively high-quality voltage waveforms. This quality comes at the expense of a more complicated circuit. This additional complexity may be warranted depending on the power level and the specified quality.

Pulse-Width Modulation. Pulse-width modulation (PWM) is a method of voltage synthesis through which high-frequency voltage pulses are applied to the inverter load (Holtz, 1994). The width of the pulses are made to vary at the desired frequency of the output voltage. Successful application of PWM generally involves a wide frequency separation between the carrier frequency and the modulation frequency. This frequency separation moves the distortion in the output voltage to high frequencies, thereby simplifying the required filtering. This subsection reviews two of the more common techniques used for synthesizing voltage waveforms using modulation.

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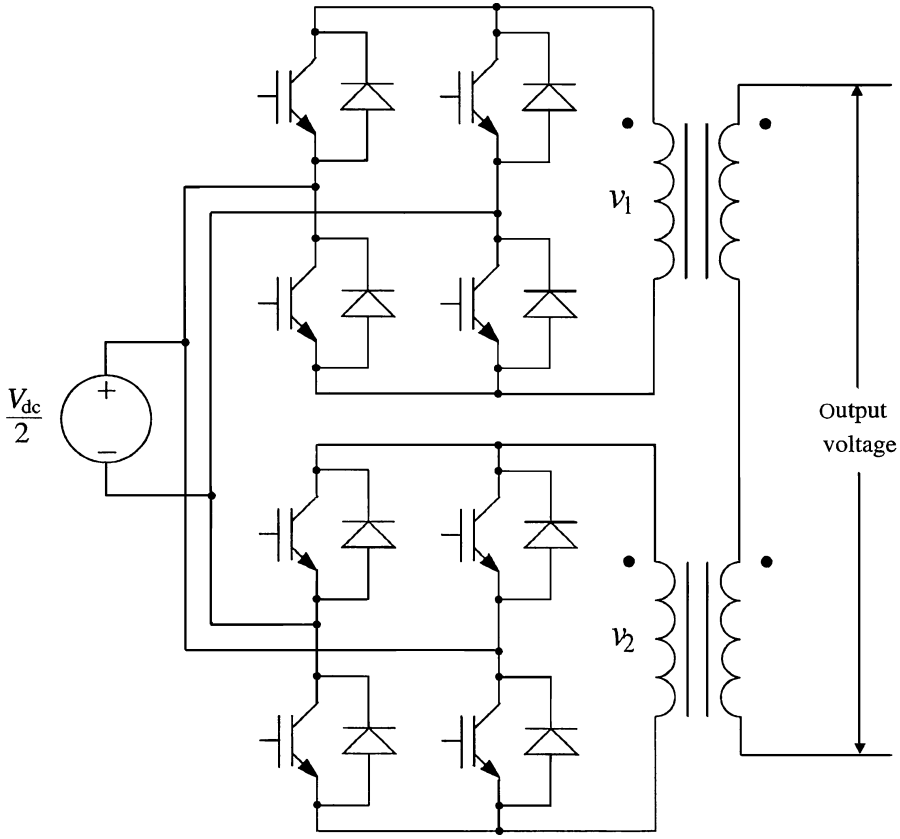

FIGURE 13.4.13 A circuit capable of synthesizing the waveforms of Fig. 13.4.12.

Sinusoidal PWM. Sinusoidal PWM implies that the pulse widths of the output voltage are distributed sinusoidally. The pulse widths are generally determined by comparing a sinusoidal reference waveform with a triangular waveform. The sinusoidal waveform sets the modulation (output) frequency and the triangular waveform sets the switching frequency. Sinusoidal PWM is routinely applied to single- and three-phase inverters.

In a single-phase inverter, the implementation of sinusoidal PWM depends on whether or not both phase-legs are operated at high frequency. Referring to Fig. 13.4.7, we see that it is not necessary for both phase-legs to operate at high frequency. We could, for example, operate switches S_1 and S_2 at high frequency to control the shape of the voltage, while switches S_3 and S_4 are operated at the frequency of the reference sinusoid to dictate the polarity of the output voltage. One advantage of this approach is that the inverter is more efficient because only two of the switches are operated at high frequency. Figure 13.4.14 shows how the sinusoidal pulse widths are created by a comparator and a unipolar triangular carrier (Kassakian, Schlecht, and Verghese, 1991). An alternative approach is to use switches S_2 and S_4 to control the polarity of the output voltage. While switch S_4 is conducting, switches S_1 and S_2 are used to control the shape of the voltage. Similarly, switches S_3 and S_4 are used to control the shape of the voltage, while switch S_2 is conducting. This approach tends to equalize the stress on the two phase-legs, and can simplify the control logic necessary to implement the PWM.

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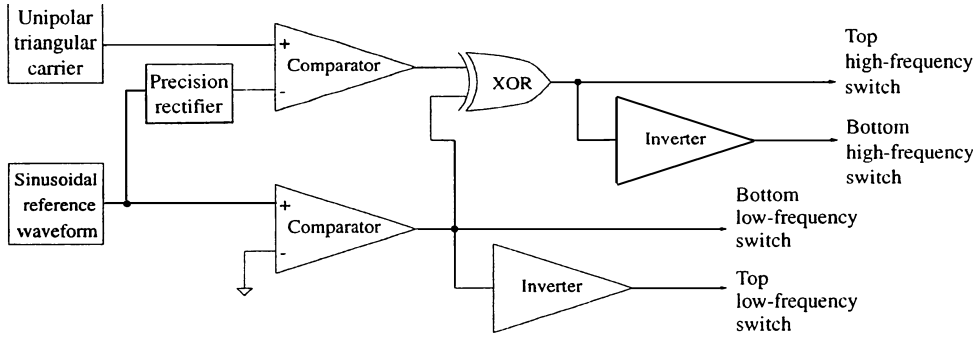

FIGURE 13.4.14 The generation of sinusoidally distributed pulse widths using a unipolar triangular carrier.

A second way of implementing sinusoidal PWM in a single-phase inverter is to operate both phase-legs at high frequency (Vithayathil, 1995). This method of control gives the same output voltage waveform as the high-frequency/low-frequency approach. The basic difference in control structures between the two is that the first method uses a unipolar triangular carrier, while the second way uses a bipolar triangular carrier. Figure 13.4.15 shows how the bipolar triangular carrier is used to create the sinusoidally distributed pulse widths.

Space-Vector PWM. Space-vector modulation is a technique that is becoming the standard method for controlling the output voltage of three-phase inverters. The technique bears great similarity to the field-oriented control techniques which are applied to ac electric machines (Van der Broeck, Skedulny, and Stanke, 1988; Holtz, Lammert, and Lotzkat, 1986; Trzynadlowski and Legowski, 1994).

A balanced set of three-phase quantities can be transformed into direct and quadrature components through the transformation

$$\begin{bmatrix} x_d \\ x_q \end{bmatrix} = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{1}$$

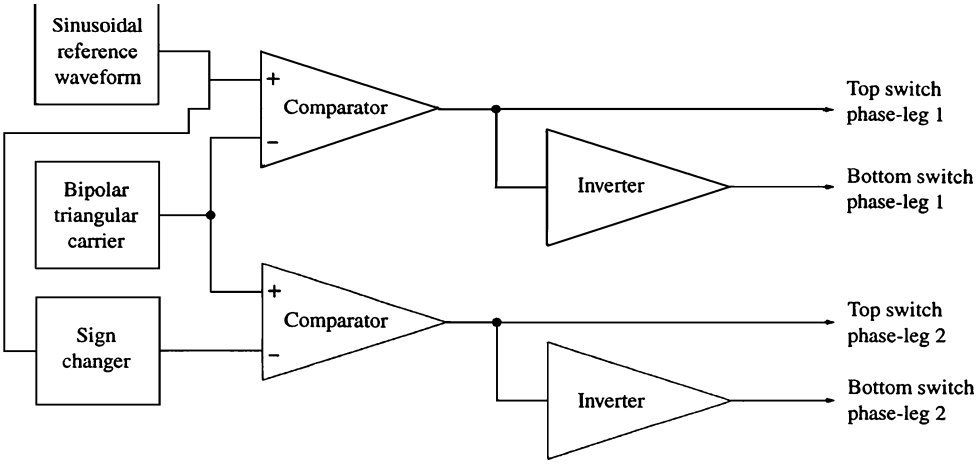

FIGURE 13.4.15 The generation of sinusoidally distributed pulse widths using a bipolar triangular carrier.

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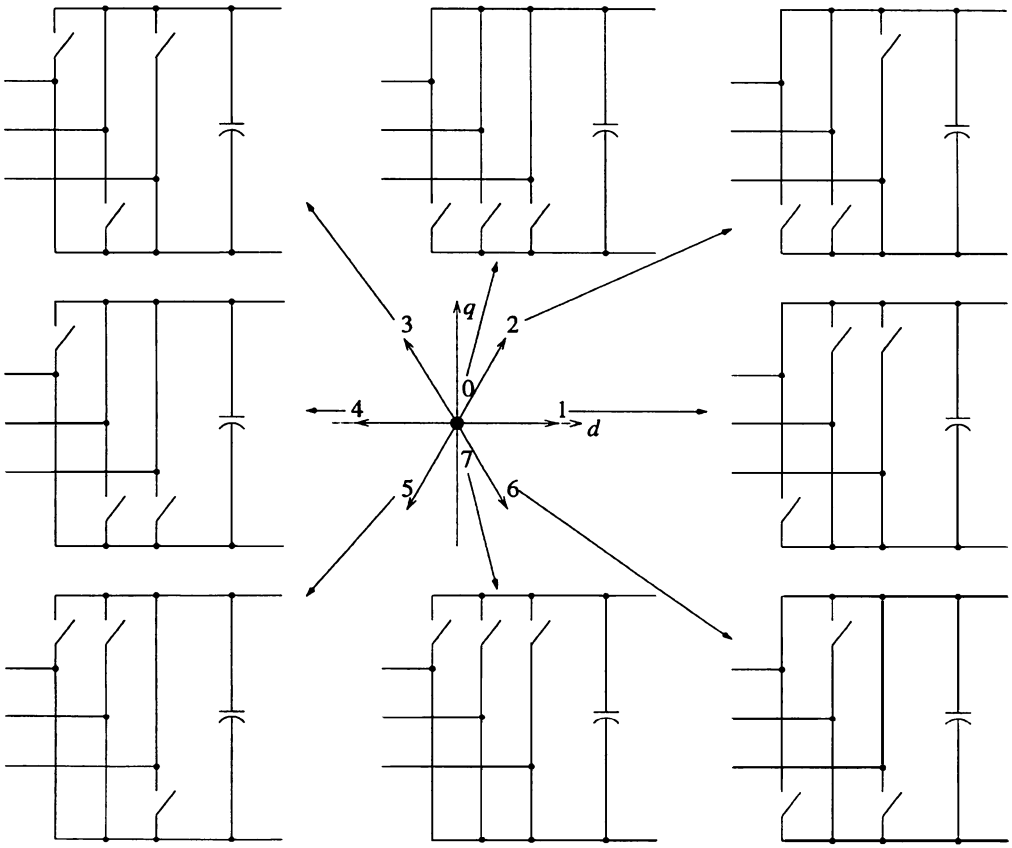

FIGURE 13.4.16 The eight space vectors that can be produced by the three-phase inverter of Fig. 13.4.8.

where x is a voltage or current. A similar transformation exists for taking direct and quadrature components back to phase quantities, though space-vector modulation does not need to use the inverse transformation.

Applying Eq. (1) to the three-phase inverter of Fig. 13.4.8, we see that each distinct switch state of the inverter corresponds with a different space vector. The zero vector can be produced by the electrically equivalent topologies of all upper switches conducting and all lower switches conducting. It is important to note that the six nonzero space vectors created by the inverter states are of the same magnitude ($\sqrt{2/3}V_{dc}$) and are symmetrically displaced. Figure 13.4.16 shows the connection between the three-phase inverter of Fig. 13.4.8 and the generation of the eight space vectors.

Any desired output voltage, up to the magnitude of $V_{dc}/\sqrt{2}$ may be synthesized by taking the three adjacent space vectors in proper proportion. Figure 13.4.17 shows how the desired voltage V^* is synthesized from the space vectors V_1, V_2, and V_0. Over one sampling interval, the duty ratios of V_1, V_2, and V_0 are, respectively,

$$d_1 = \frac{2/\sqrt{3}|V^*|\sin(60° - \gamma)}{\sqrt{2/3}V_{dc}} \tag{2}$$

$$d_2 = \frac{2/\sqrt{3}\,|V^*|\sin\gamma}{\sqrt{2/3}V_{dc}} \tag{3}$$

$$d_0 = 1 - d_1 - d_2 \tag{4}$$

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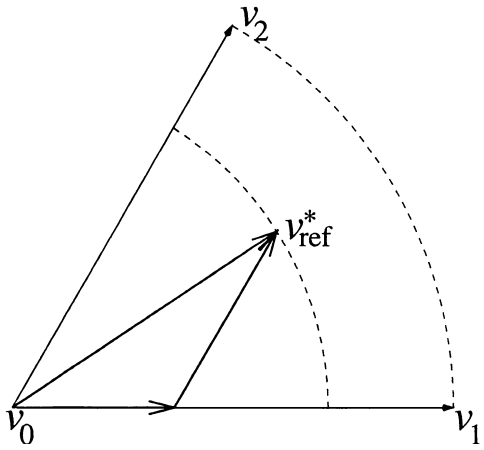

FIGURE 13.4.17 The synthesis of voltage V^* using space vector modulation.

The order used in implementing the space vectors is driven by the desire to minimize the number of switching operations. Careful examination of Figs. 13.4.16 and 13.4.17 reveals that within any of the six segments delimited by space vectors, the move from one vector to the next requires changing the state of only one switch. In practice, the switching in adjacent sampling intervals would apply the sequence $\cdots |V_1|V_2|V_0|V_0|V_2|V_1| \cdots$. Different approaches use different criteria for selecting the best implementation of V_0 (Trzynadlowski and Legowski, 1994).

Extension of the space-vector concept is possible with multilevel inverters (Holmes and McGrath, 2001; Tolbert, Peng, and Habetler, 2000). Multilevel inverters, however, offer a substantially greater number of space vectors from which to choose. With three-level inverters, for example, there are now 19 different space vectors. Additional levels would increase the number of space vectors still further. The number of redundant space vectors also increases in multilevel inverters, thereby offering additional degrees of freedom within the voltage synthesis algorithm. Figure 13.4.18 shows the space vectors that can be created by a three-phase three-level inverter based on the phase-leg of Fig. 13.4.12. The numbers adjacent to each space vector represent the switch configuration of phases a, b, and c, respectively. Space vectors with more than one set of numbers can be achieved with any of the switch combinations indicated. Referring to Fig. 13.4.12, a 0 indicates that switches S_3 and S_4 are connecting the output terminal to the negative side of the dc bus. Similarly, a 1 indicates switches S_2 and S_3 are connecting the output terminal to the midpoint of the dc bus. Finally, a 2 indicates that switches S_1 and S_2 are connecting the load terminal to the positive side of the dc bus.

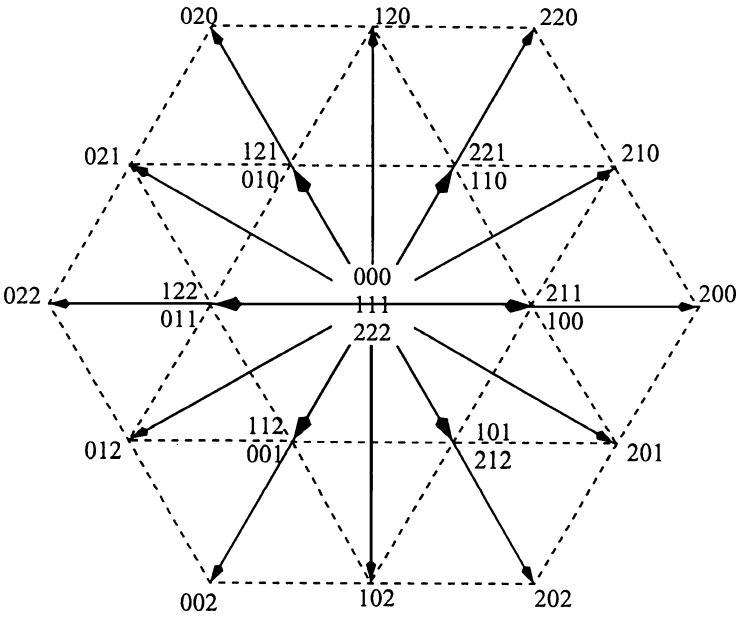

FIGURE 13.4.18 The achievable space vectors associated with a three-phase three-level inverter.

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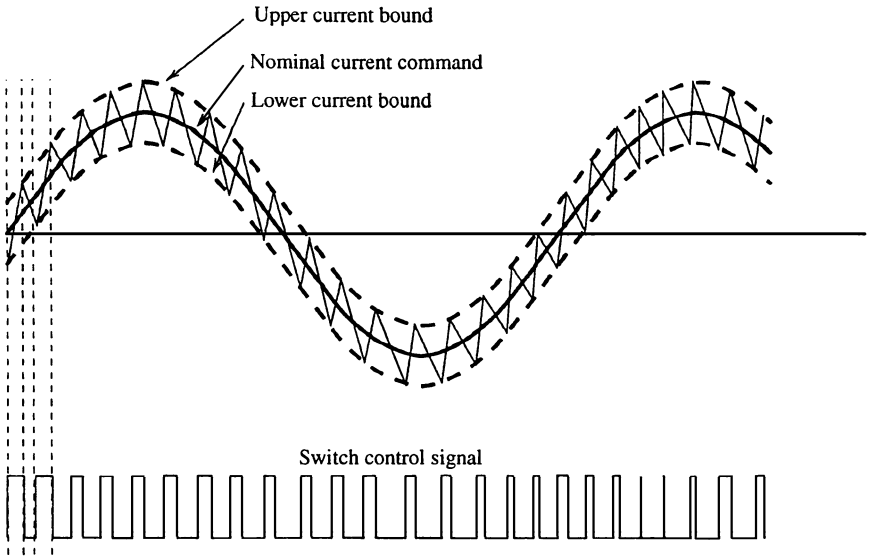

FIGURE 13.4.19 The principles of hysteretic current control.

CURRENT WAVEFORM SYNTHESIS TECHNIQUES

While voltage-source inverters always output a voltage waveform, there are many applications where the details of the voltage waveform are driven by the creation of a current with a specific shape. In this context, the controller is determining the state of each inverter switch based on how well the inverter output currents are tracking commanded output currents. While the PWM techniques of the previous subsection can often be applied to transform a voltage-source inverter into a controlled current source (Brod and Novotny, 1985; Habetler, 1993), there are some additional techniques that are useful in this type of operation. The control techniques described in this subsection are amenable to synthesizing current waveforms with inverters.

Hysteresis and Sliding-Mode Control. Hysteresis and sliding-mode control are very similar in nature. In both of these control approaches, a reference current waveform is established and the switching of the inverter is tied to the relative location of the actual current and the reference waveform (Brod and Novotny, 1985; Bose, 1990; Slotine and Li, 1991; Torrey and Al-Zamel, 1995). Under hysteretic control, a hysteresis band is introduced around the reference waveform in order to limit the switching frequency. Figure. 13.4.19 illustrates the principles of hysteretic control. Sliding-mode control can be implemented in a manner which is indistinguishable from hysteretic control, or it can be implemented as shown in Fig. 13.4.20 where there is a known upper limit on the switching frequency.

A common problem with hysteretic control is that the switching frequency is not fixed and may vary widely over one cycle of the output. This can complicate the design of filters and may raise reliability concerns relative

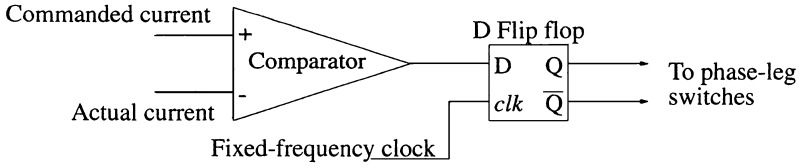

FIGURE 13.4.20 One method of implementing sliding-mode control.

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to the safe operation of the switches. Fixing the switching frequency is possible (Kazerani, Ziogas, and Joos, 1991), at the expense of a hysteresis band that changes throughout each cycle of the output.

Predictive Current Regulation. Predictive current regulation is similar to hysteresis and sliding-mode control in the establishment of a reference current and acceptable error bounds (Holtz, 1994; Wu, Dewan, and Slemon, 1991). The predictive controller uses a model of the system in conjunction with measurements of the system state in order to predict how long the next switching state is to be maintained so that the actual current remains within the established error bounds. In contrast to hysteresis and sliding-mode control, the predictive controller is always looking ahead one sampling interval into the future.

INVERTER APPLICATIONS

This subsection reviews four important applications of inverters: uninterruptible power supplies, motor drives, active power filters, and utility interfaces for distributed generation. Uninterruptible power supplies have become an extremely large market in support of the expanding use of personal computers and other critical loads. These systems are able to support computer operation in the face of unreliable utility power, thereby preventing the loss of data. Motor drives allow for adjustable speed operation of electric motors, thereby providing a better match between the motor output and the power required by the load. The proper application of adjustable speed drives can result in significant energy savings. The increasing application of active power filters and active power line conditioners is a reflection of increasing harmonic distortion on power systems, and the regulatory responses to this distortion. Distributed generation sources (fuel cells, solar photovoltaics, wind turbines, and microturbines) often function as sources of dc power, thereby requiring an inverter to deliver this power to the ac utility grid.

Uninterruptible Power Supplies. An uninterruptible power supply (UPS) uses a battery to provide energy to a critical load in the event of a power system disturbance. There are two basic topologies used in UPS systems, as shown in the block diagrams of Figs. 13.4.21 and 13.4.22 (Mohan, Undeland, and Robbins, 1995). Both single- and three-phase UPS systems are available.

In Fig. 13.4.21, the critical load is always supplied through an inverter. This inverter is fed from either the utility or the battery bank, depending on the availability of the utility. The battery is continually charged when the utility is present. This type of UPS provides effective protection of the critical load by isolating it from utility under- and over-voltages.

In Fig. 13.4.22, the functions of battery charging and the inverter are combined. While the utility is present, the inverter is run as a controlled rectifier to support battery charging. When the utility fails, the load is supplied from the battery-fed inverter. Because an inverter does not have the ability to deliver a larger voltage than that of the dc source, it may be necessary to include a bidirectional dc/dc converter if a low voltage battery is used in the UPS.

Motor Drives. Motor drives can be found in a very wide range of power levels, from fractional horsepower up to hundreds of horsepower (Bose, 1986; Murphy and Turnbull, 1988). These applications range from very

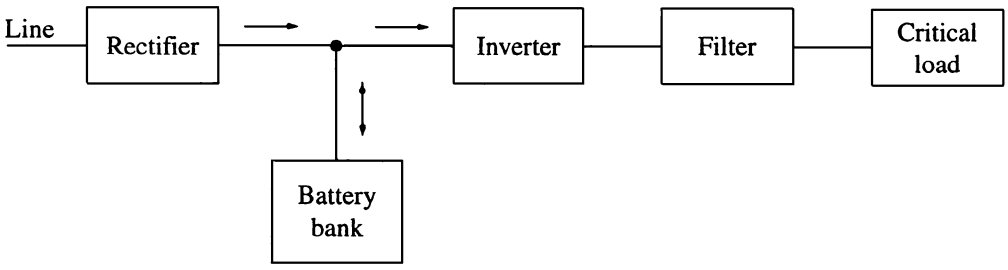

FIGURE 13.4.21 A block diagram for one configuration of a UPS system.

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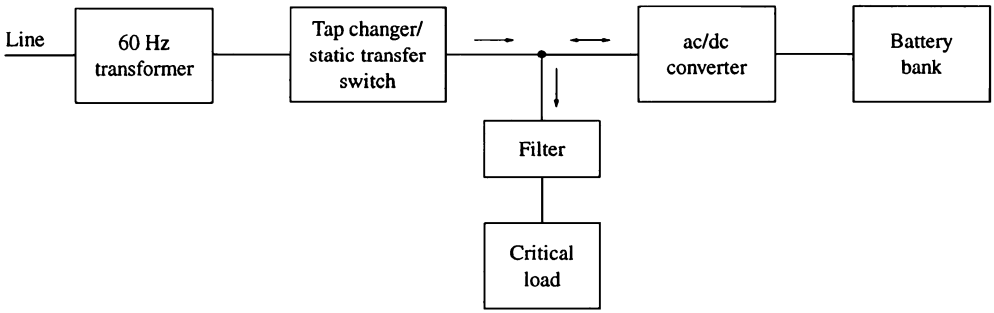

FIGURE 13.4.22 A block diagram for a second UPS system configuration.

precise motion control to adjustable speed operation of pumps and compressors for saving energy. In a motor drive, the inverter is used to provide an adjustable frequency ac voltage to the motor, thereby enabling the motor to operate over a wide range of speeds without derating the torque production of the motor. In order to prevent the motor from being pushed into magnetic saturation, the amplitude of the synthesized voltage is usually tied to the output frequency. In the simplest adjustable speed drives, the ratio of peak output voltage to output frequency is maintained nominally constant, with a small boost at low frequencies to compensate to the resistance of the motor windings. More sophisticated adjustable speed drives implement sensorless flux vector control (Bose, 1997).

Active Power Filters. Active power filters are able to simultaneously provide compensation for the reactive power drawn by other linear loads while compensating for the harmonic currents being drawn by still other nonlinear loads (Gyugyi and Strycula, 1976; Akagi, Kanazawa, and Nabae, 1984; Akagi, Nabae, and Atoh, 1986; Torrey and Al-Zamel, 1995). It is possible to compensate for multiple loads at one point. The basic idea of an active power filter is shown in Fig. 13.4.23. The active power filter is formed by putting an inverter in parallel with the loads for which compensation is needed. The inverter switches are then controlled to force the line current drawn from the utility to be of the desired quality. The inverter is controlled to draw currents that precisely compensate for the undesired components in the currents drawn by the loads. The undesired components may be either reactive or harmonic in nature. In Fig. 13.4.23, i_{utility} is forced to be of the desired quality and phase through the superposition of i_{filter} and $i_{\text{nonlinear loads}}$. With control over i_{filter}, the utility current can be forced to track its intended shape and amplitude.

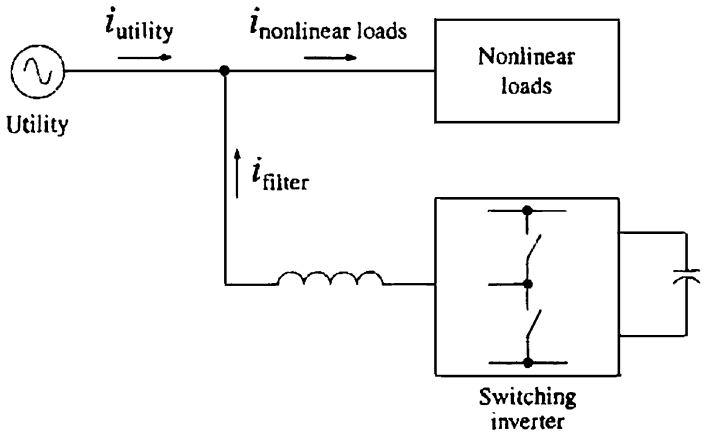

FIGURE 13.4.23 A one-line diagram of an active filter system.

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Distributed Generation. There is an ever-increasing interest in the integration of distributed generation sources into the electric utility system. Distributed generation sources include fuel cells, solar photovoltaics, wind energy, hydroelectric, and microturbines, among others. Their application is sometimes driven by the utility in an effort to use a local resource such as hydroelectric energy, to increase generating capacity without having to increase the capacity of their transmission lines, to add generation capacity incrementally without the large capital investment required of a more traditional generating station, or to increase the reliability of the supply for critical customers. Distributed generation sources are sometimes used by electricity customers to reduce their electricity costs or to increase the reliability of their electricity supply.

Some distributed generation sources naturally provide energy through dc, thereby requiring an inverter to deliver the energy to the utility grid. Fuel cells and solar photovoltaics fall into this category. Other distributed generation sources provide energy through ac with variable frequency and amplitude. Wind turbines, microturbines, and some hydroelectric systems fall into this category. This ac energy is usually delivered to the utility by first rectifying the variable ac into dc and then using an inverter to provide fixed frequency ac with a fixed amplitude to the utility grid. In some cases the rectification process is facilitated by an inverter structure where the flow of energy is from the ac side to the dc side. In this way phase currents can be controlled far more precisely than would be possible with an uncontrolled rectifier.

A significant issue with the deployment of distributed generation sources is the prevention of a situation known as islanding. An inverter that is unable to detect the presence or absence of the utility may continue to feed a section of the utility system even after the utility has taken actions to deenergize that section. This creates a serious safety issue for any utility workers who may be working on the utility system. For this reason, any inverter that is designed to interact with the ac utility must include anti-islanding controls that actively and continuously verify the presence of the larger ac utility system. Techniques for accomplishing this are described in Stevens et al. (2000) for photovoltaic systems, but the techniques described are applicable to other energy sources.

Inverters for distributed generation systems are designed to be either utility interactive or utility independent. The difference between them is found in the control. Utility interactive inverters are controlled to behave as a current source, delivering power to the utility with near-unity power factor. Utility independent inverters behave as voltage sources, where the phase difference between the output voltage and the load current is dictated by the load on the inverter.

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