CHAPTER 14.3
ACTIVE WAVEFORM SHAPING

Paul G. A. Jespers

ACTIVE CIRCUITS

Linear active networks used currently for waveshaping take advantage of negative or positive feedback circuits to improve the performance. Of the linear negative feedback active wave-shaping circuits, the operational amplifier-integrator is widely used.

RC OPERATIONAL AMPLIFIER-INTEGRATOR

In Fig. 14.3.1 it is assumed that the operational amplifier has infinite input impedance, zero output impedance, and a high negative gain A. The overall transfer function is

$$\frac{A}{1+p(1-A)T} \quad \text{where } T = RC \tag{1}$$

This function represents a first-order system with gain A and a cutoff frequency, which is approximately $|A|$ times lower than the inverse of the time constant T of the RC circuit. In Fig. 14.3.1*b* the frequency response of the active circuit is compared with that of the passive RC integrator. The widening of the spectrum useful for integration is clearly visible. For instance, an integrator using an operational amplifier with a gain of 10^4 and an RC network having a 0.1 s time constant has a cutoff frequency as low as 1.6 MHz.

In the time domain, the Taylor expansion of the amplifier-integrator response to the step function is

$$V(t) = E\frac{t}{T}\left[1 - \frac{t}{2!\,|A|\,T} + \frac{t^2}{3!(|A|\,T)^2} - \cdots\right] \tag{2}$$

This shows that almost any desired degree of linearity of $V(t)$ can be achieved by providing sufficient gain.

SWEEP GENERATORS[4]

Sweep generators (also called time-base circuits) produce linear voltage or current ramps versus time. They are widely used in applications such as oscilloscopes, digital voltmeters, and television. In almost all circuits the linearity of the ramp results from charging or discharging a capacitor through a constant-current source. The difference between circuits used in practice rests in the manner of realizing the constant-current source. Sweep generators may also be looked upon as integrators with a constant-amplitude input signal. The latter point of view shows that RC operational amplifier-integrators provide the basic structure for sweep generation.

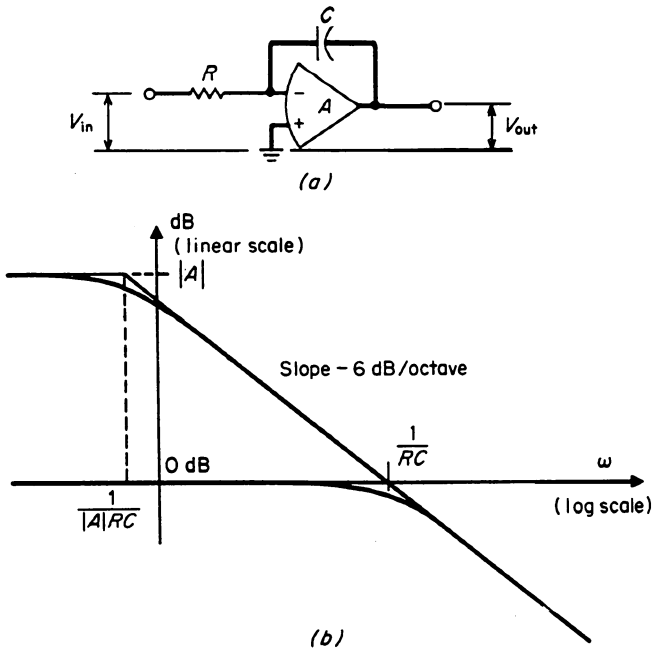

FIGURE 14.3.1 (*a*) Operational amplifier-integrator; (*b*) gain vs. angular frequency.

Circuits delivering a linear voltage sweep fall into two categories, the Miller time base and bootstrap time base. A simple Miller circuit (Fig. 14.3.2) comprises a capacitor C in a feedback loop around the amplifier formed by T_1. Transistor T_2 acts like a switch. When it is on, all the current flowing through the base resistor R_B is driven to ground, keeping T_1 blocked, since the voltage drop across T_2 is lower than the normal base-to-emitter voltage of T_1. The output signal V_{CE} of T_1 is thereby clamped at the level of the power-supply voltage E_{cc}, and the voltage drop across the capacitor C is approximately the same. When T_2 is turned off, it drives T_1 into the active region and

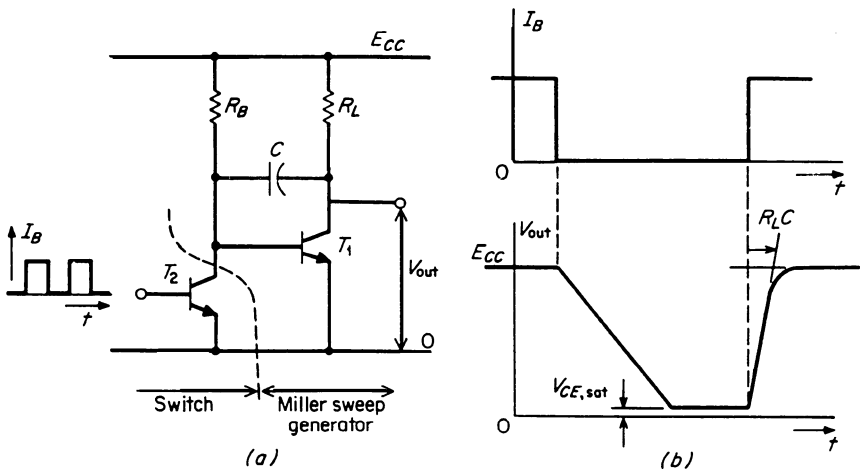

FIGURE 14.3.2 Miller sweep generator: (*a*) circuit; (*b*) input and output vs. time.

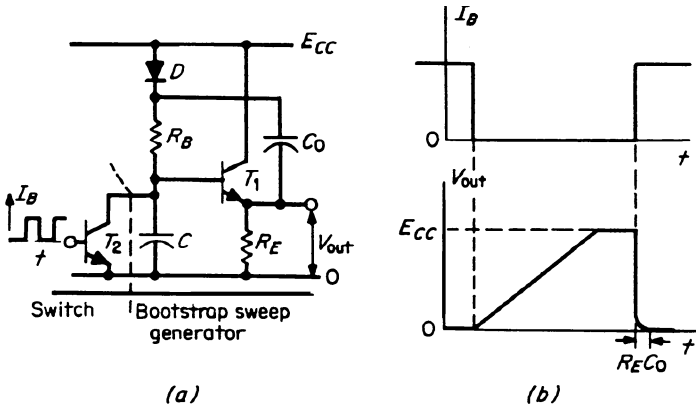

FIGURE 14.3.3 Bootstrap sweep generator: (*a*) circuit; (*b*) input and output vs. time.

causes collector current to flow through R_L. The resulting voltage drop across R_L is coupled capacitively to the base of T_1, tending to minimize the base current; i.e., the negative-feedback loop is closed. The collector-to-emitter voltage V_{CE} of T_1 subsequently undergoes a linear voltage sweep downward, as illustrated in Fig. 14.3.2*b*.

The circuit behaves in the same manner as the *RC* operational amplifier above. Almost all the current flowing through R_B is derived through the feedback capacitor, and only a very small part is used for controlling the base of T_1. The feedback loop opens when T_1 enters into saturation, and the voltage gain of the amplifier becomes small.

When T_2 is subsequently turned on again, blocking T_1 and recharging C through R_L and the saturated switch, the output voltage V_{CE} rises again according to an exponential with time constant $R_L C$.

Figure 14.3.3 shows a typical bootstrap time-base circuit. It differs from the Miller circuit in that the capacitor C is not a part of the feedback loop. Instead the amplifier is replaced by an emitter-follower delivering an output signal V_{out} which reproduces the voltage drop across the capacitor. C is charged through resistor R_B from a floating voltage source formed by the capacitor C_0(C_0 is large compared with C).

First, we consider that the switch T_2 is on. Current then flows through the series combination formed by the diode D, the resistor R_B, and the saturated transistor T_2. The emitter follower T_1 is blocked since T_2 is saturated. Moreover, the capacitor C_0 can charge through the path formed by the diode D and the emitter resistor R_E, and the voltage drop across its terminals is equal to E_{CC}. When T_2 is cut off, the current through R_B flows into the capacitor C, causing the voltage drop across its terminals to rise gradually, driving T_1 into the active region. Because T_1 is a unity-gain amplifier, V_{out} is a replica of the voltage drop across C.

Since C_0 acts as a floating dc voltage source, diode D is reverse-biased immediately. The current flowing through R_B is supplied exclusively by C_0. Since $C_0 \gg C$, the voltage across R_B remains practically constant and equal to the voltage drop across C_0 minus the base-to-emitter voltage of T_1.

Considering that the base current of T_1 represents only a small fraction of the total current flowing through R_B, it is evident that the charging of capacitor C occurs under constant-current and that therefore a linear voltage ramp is obtained as long as the output voltage of T_1 is not clamped to the level of the power-supply voltage E_{CC}.

The corresponding output waveforms are shown in Fig. 14.3.3*b*. After T_2 is switched on again, C discharges rapidly, causing V_{out} to drop, while the diode D again is forward-biased and the small charge lost by C_0 is restored. In practice, C_0 should be at least 100 times larger than C to ensure a quasi-constant voltage source.

More detailed analysis of the Miller and bootstrap sweep generators reveals that they are in fact equivalent. We redraw the Miller circuit as shown at the left of Fig. 14.3.4. Remembering that the operation of the sweep generator is independent of which output terminal is grounded, we ground the collector of T_1 and redraw the corresponding circuit. As shown at the right in the figure, this is a bootstrap circuit, so that the two circuits are equivalent.

Any sweep generator can be regarded as a simple loop (Fig. 14.3.5) comprising a capacitor C delivering a voltage ramp, a loading resistor R_B, and the series combination of two sources: a constant voltage source E_{cc} and a variable source whose emf E reproduces the voltage drop V across the capacitor. The voltage drop across

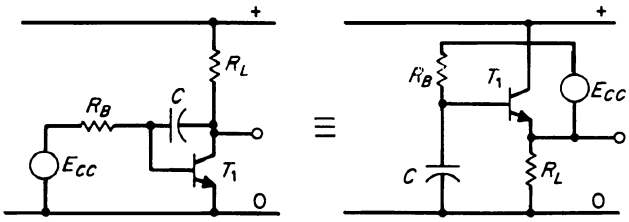

FIGURE 14.3.4 Equivalency of the Miller and bootstrap sweep generators.

R_B consequently remains constant and equal to E_{cc} making the loop current also constant. The voltage ramp consequently is given by

$$E = V = (E_{cc}/R_B C)t \tag{3}$$

Grounding terminal 1 yields the Miller network, while grounding terminal 2 leads to the bootstrap circuit.

Since linearity is one of the essential features of sweep generators, we consider the equivalent networks represented in Fig. 14.3.6. Starting with the Miller circuit, we determine the impedance in parallel with C

$$|A|(R_B \,||\, h_{11}) \tag{4}$$

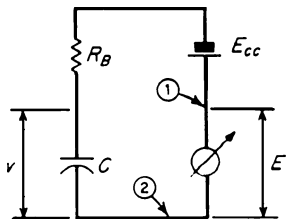

FIGURE 14.3.5 Basic loop of sweep-generator circuits.

where $|A|$ is the absolute value of the voltage gain of the amplifier

$$|A| = (h_{21}/h_{11})R_L$$

Next, considering the bootstrap circuit, we calculate the input impedance of the unity-gain amplifier to determine the loading impedance acting on C. This impedance is

$$R_L h_{21} R_B/(R_B + h_{11}) \tag{5}$$

which turns out to be the same as that given in Eq. (4); i.e., the two circuits are equivalent. To determine the degree of linearity it is sufficient to consider the common equivalent circuit of Fig. 14.3.7 and to calculate the Taylor expansion of the voltage V

$$V = \frac{E_{CC}}{R_B C} t\left[1 - \frac{t}{2!|A|(R_B \| h_{11})C} + \frac{t^2}{3![|A|(R_B \| h_{11})C]^2} - \cdots\right] \tag{6}$$

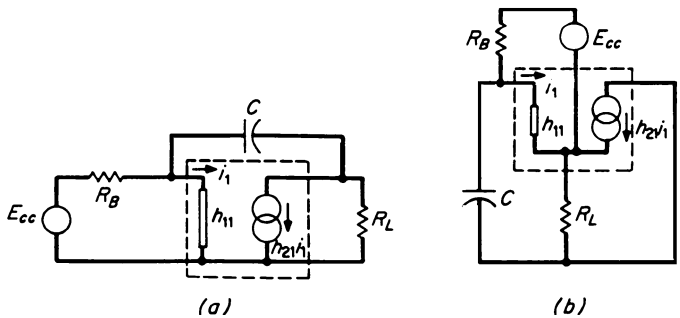

FIGURE 14.3.6 Equivalent forms of (*a*) Miller and (*b*) bootstrap sweep circuits.

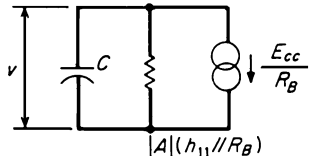

FIGURE 14.3.7 Common equivalent circuit of sweep generators.

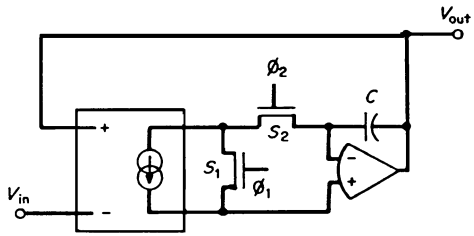

FIGURE 14.3.8 Typical sample-and-hold circuit.

The higher the voltage gain $|A|$, the better the linearity. Thus, an integrated operational amplifier in place of T_1 leads to excellent performance in both the Miller and the bootstrap circuit. Voltage gains as high as 10,000 are easily obtained for this purpose.

SAMPLE-AND-HOLD CIRCUITS[4]

Sample-and-hold circuits are widely used to store analog voltages accurately over time ranging from microseconds to minutes. They are basically switched-capacitor networks, but since the analog voltage across the storage capacitor in the hold mode must be sensed under low impedance, a buffer amplifier is needed. Op-amps with FET input are commonly used for this purpose to minimize the hold-mode droop. The schematic of a widely used integrated circuit is shown in Fig. 14.3.8.

Storage and readout are achieved by the FET input op-amp in the hold mode. During the acquisition time, transistor S_2 is conducting, while S_1 is blocked. Current is supplied by the voltage-dependent current source to minimize the voltage difference between input and output terminals. As soon as S_1 and S_2 change their states, V_{out} ceases to follow V_{in} and remains unchanged.

The main requirements for sample-and-hold circuits are low hold-mode droop, short settling time in the acquisition mode, low offset voltage, and small hold-mode feedthrough. The hold-mode droop is dependent on the leakage current of the op-amp inverting node. Short settling times require high-slew-rate op-amps and large current-handling capabilities for both the current source and the op-amp. The offset voltage is determined by the differential amplifier which controls the current source. Finally, feedthrough is a result of imperfect isolation between the current source and the op-amp. For this reason, a double switch is preferred to a single series switch.

Another important feedthrough problem is related to the unavoidable gate-to-source or drain-overlap capacitance of the MOS switch S_2. When the gate-control signal is switched off, some small charge is always transferred capacitively to the storage capacitor and a small voltage step is superimposed on the output terminal when the circuit enters the hold state. Minimization of this effect can be achieved by increasing the ratio of the storage capacitance to the switch-overlap capacitance. Since the latter cannot be made equal to zero, the storage capacitance must be chosen sufficiently large, but this inevitably lengthens the settling time. One means of alleviating the problem is to compensate the switching charge because of the control signal by injection of an equal and opposite charge on the inverting input node of the op-amp. This can be achieved by means of a dummy transistor controlled by the inverted signal.

NONLINEAR NEGATIVE FEEDBACK WAVEFORM SHAPING

The use of nonlinear devices with negative feedback accentuates the character of waveshaping networks. In many circumstances, this leads to an idealization of the nonlinear character of the devices considered. A good example of this is given by the ideal rectifier circuit.

The negative-feedback loop in the circuit shown in Fig. 14.3.9 is formed by two parallel branches. Each comprises a diode connected in such manner that if V_1 is positive, the current injected by resistor R_1 flows

through D_1, and if V_1 is negative, through D_2. A resistor R_2 is placed in series with D_1, and the output voltage V_2 is taken at the node between R_2 and D_1. Hence, V_2 is given by $-(R_2/R_1)V_1$ when V_1 is positive, independently of the forward voltage drop across D_1.

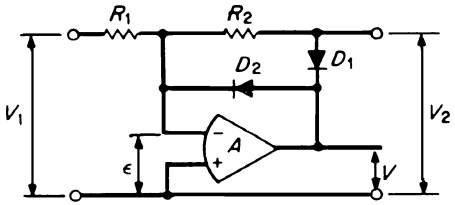

FIGURE 14.3.9 The precision rectifier using negative feedback is almost an ideal rectifier.

When D_1 is forward-biased, the voltage V at the output of the op-amp adjusts itself to force the current flowing through D_1 and R_L to be exactly the same as through R_1. This means that V may be much larger than V_2, especially when V_2 (and thus also V_1) is of the order of millivolts. In fact, V exhibits approximately the same shape as V_2 plus an additional pedestal of approximately 0.6 to 0.7 V. Typical waveforms obtained with a sinusoidal voltage of a few tens of millivolts are shown in Fig. 14.3.10.

The quasi-ideal rectification characteristic of this circuit is readily understood by considering the Norton equivalent network seen from R_2 and D_1 in series. In consists of a current source delivering the current V_1/R_1 in parallel with an almost infinite resistor $|A|\,R$, where A represents the voltage gain of the op-amp. Hence, the current flowing through the branch formed by R_2 and D_1 is delivered by a quasi-ideal current source, and the voltage drop across R_2 is unaffected by the series diode D_1. As for D_2, it is required to prevent the feedback loop from being opened when V_1 is negative. If this could happen, the artificial ground at the input of the op-amp would be lost and V_2 would not be zero.

Other negative-feedback configurations leading to very high output impedances are equally powerful in achieving ideal rectification characteristics. For instance, the unity-gain amplifier used in instrumentation has wide linear ac measurement capabilities (Fig. 14.3.11).

POSITIVE FEEDBACK WAVEFORM SHAPING

Positive feedback is used extensively in bistable, monostable, and astable (free-running) circuits. Astable networks include free-running relaxation circuits whether self-excited or synchronized by external trigger pulses. Monostable and bistable circuits also exist, with one and two distinct stable states, respectively.

The degree to which positive feedback is used in harmonic oscillators differs substantially from that of astable, monostable, or bistable circuits. In an oscillator the total loop gain must be kept close to 1. It needs to compensate only for small losses in the resonating tank circuit. In pulsed circuits, positive feedback permits

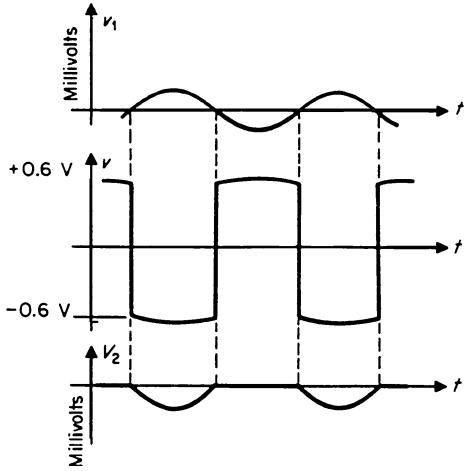

FIGURE 14.3.10 Waveforms of circuit in Fig. 14.3.9.

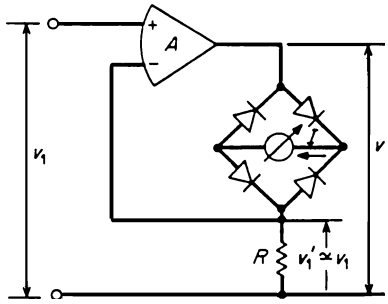

FIGURE 14.3.11 Feedback rectification circuit used in precision measurements.

fast switching from one state to another, e.g., from cutoff to saturation and vice versa. Before and after these occur, the circuit is passive. Switching occurs in extremely short times, typically a few ns. After switching, the circuit evolves more slowly, approaching steady-state conditions.

It is common practice to call the switching time the *regeneration time* and the time needed to reach final steady-state conditions the *resolution time*. The resolution time may range from tens of nanoseconds to several seconds or more, depending on the circuit.

An important feature of triggered regenerative circuits is that their switching times are essentially independent of the steepness of the trigger-signal waveshape. Once instability is reached the transition occurs at a rate fixed by the total loop gain and the reactive parasitics of the circuit itself but independent of the rate of change of the trigger signal itself. Regenerative circuits, therefore, provide means of restoring short rise times.

Positive-feedback pulse circuits are necessarily nonlinear. The most conventional way to study their behavior is to take advantage of piecewise-linear analysis techniques.

Bistable Circuits[5] (Collector Coupled)

Two cascaded common-emitter transistor stages implement an amplifier with a high positive gain. Connecting the output to the input (Fig. 14.3.12) produces an unstable network known as the *Eccles-Jordan bistable circuit* or *flip-flop*. Under steady-state conditions one transistor is saturated and the other is blocked.

Suppose the circuit of Fig. 14.3.12 has the value $R_L = 1$ kΩ, $R = 2.2$ kΩ, and $E_{cc} = 5$ V. Suppose T_1 is at cutoff, and consider the equivalent network connected to the base of T_2. It can be viewed as an emf of 5 V and series resistances of 3.2 kΩ. The base current of T_2 is given by

$$I_{B2} = (5 - 0.7)/3.2 = 1.34 \text{ mA} \tag{7}$$

T_2 being saturated, the collector current is equal to E_{CC}/R_L or 5 mA. A current gain of 4 would be sufficient to ensure saturation of T_2. Hence the collector-to-emitter voltage across T_2 will be very small ($V_{CE,\text{sat}}$), and consequently T_1 will be blocked, as stated initially. The reverse situation, with T_1 saturated and T_2 cut off, is governed by identical considerations for reasons of symmetry. Two distinct stable states thus are possible.

When one of the transistors is suddenly switched from one state to the opposite, the other transistor automatically undergoes an opposite transition. At a given time both transistors conduct simultaneously, which increases the loop gain from zero to a high positive value. This corresponds to the regenerative phase, during which the circuit becomes active.

It is difficult to compute the regeneration time since the operating points of both transistors move through the entire active region, causing large variations of the small-signal parameters. Although determination of the regeneration time on the basis of a linear model is unrealistic and leads only to a rough approximation, we briefly examine this problem since it illustrates how the regeneration phase of unstable networks may be analyzed.

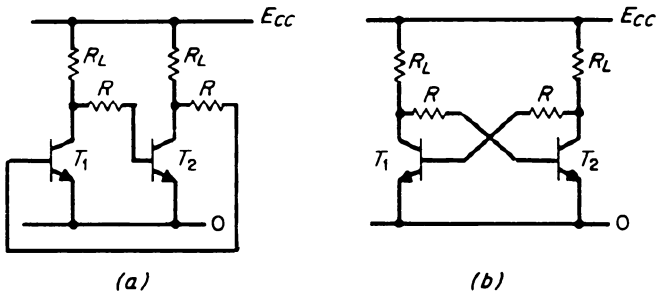

FIGURE 14.3.12 The Eccles-Jordan bistable circuit (flip-flop): (*a*) in the form of two cascaded amplifiers with output connected to input; (*b*) as customarily drawn, showing symmetry of connections.

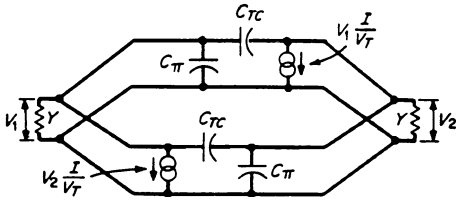

FIGURE 14.3.13 Flip-flop circuit showing capacitances that determine time constants.

First, we introduce two capacitors in parallel with the two resistors R. These capacitors provide a direct connection from collector to base under transient conditions and hence increase the high-frequency loop again. The circuit can now be described by the network of Fig. 14.3.13, which consists of a parallel combination of two reversed transistors without extrinsic base resistances (for calculation convenience) and with two load admittances Y which combine the load and resistive input of each transistor. Starting from the admittance matrix of one of the transistors with its load, we equate the determinant of the parallel combination

$$\begin{vmatrix} p(C_\pi + C_{TC}) & -pC_{TC} \\ \dfrac{I}{V_T} - pC_{TC} & pC_{TC} + Y \end{vmatrix} \tag{8}$$

to zero to find the natural frequencies of the circuit. This leads to

$$pC_\pi + (I/V_T) + Y = 0 \tag{9}$$

and

$$p(C_\pi + 4C_{TC}) + Y - I/V_T = 0 \tag{10}$$

where C_π stands for the parallel combination of C_{TE} and the diffusion capacitance $\tau_F I/V_T$. Only Eq. (10) has a zero with a real positive pole, producing an increasing exponential function with time constant approximately equal to

$$\tau = (C_\pi + 4C_{TC})\, V_T/I \tag{11}$$

Since the diffusion capacitance overrules the transition capacitances at high current, Eq. (11) reduces finally to τ_F. This yields extremely short switching times. For instance, a transistor with a maximum transition frequency f_T of 300 MHz and a τ_F equal to 0.53 ns, exhibits a regeneration time (defined as the time elapsing between 10 and 90 percent of the total voltage excursion from cutoff to saturation or vice versa) equal to $2.2\tau_F$, or 1.2 ns.

A more accurate but much more elaborate analysis, taking into account the influence of the extrinsic base resistance and nonlinear transition capacitances in the region of small-collector current, requires a computer simulation based on the dynamic large-signal model of the bipolar transistor. Nevertheless, Eq. (11) clearly pinpoints the factors controlling the regeneration time; the transconductance and unavoidable parasitic capacitances. This is verified in many other positive-feedback switching circuits.

We consider next which factors control the resolution time still with the same numerical data. We suppose T_1 initially nonconducting and T_2 saturated. The sudden turnoff of T_2 is simulated by opening the short-circuit switch S_2 in Fig. 14.3.14*a*. Immediately, V_{CE2} starts increasing toward E_{cc}. The base voltage V_{BE1} of T_1 consequently rises with a time constant fixed only by the total parasitic capacitance C_T at the collector of T_2 and base of T_1 times the resistor R_L. Hence this time constant is

$$\tau_1 = R_L C_T \tag{12}$$

This time is normally extremely short; e.g., a parasitic capacitance of 1 pF yields a time constant of 1 ns. The charge accumulated across C evidently cannot change, for C is much larger than C_T. So V_{BE1} and V_{CE2} increase at the same rate. This situation is illustrated in Fig. 14.3.14*b*. When V_{BE1} reaches approximately 0.7 V, T_1 starts conducting and a new situation arises, illustrated in Fig. 14.3.14 by the passage from (*b*) to (*c*). This is when regeneration actually takes place, forcing T_1 to go into saturation very rapidly. With the regeneration period neglected, case (*c*) is characterized by the time constant

$$\tau_2 = (R_L/R)C \tag{13}$$

For instance, if C is equal to 10 pF, τ_2 yields 7 ns. Although this time constant is much longer than τ_1, it is still not the longest, for we have not yet considered the evolution of V_{BE2}.

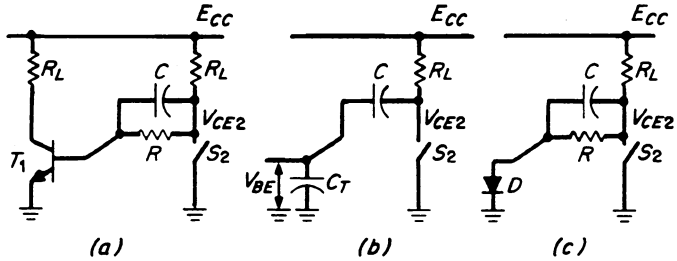

FIGURE 14.3.14 Piecewise analysis of flip-flop switching behavior. Transistor T_2 is assumed to be on before (*a*). The opening of S_2 simulates cutoff. The new steady-state conditions are reached in (*c*).

It is considered in Fig. 14.3.15, where the saturated transistor T_1 is replaced by the closing of S_1. The problem is the same as for the compensated attenuator. Since overcompensation is achieved, V_{BE2} undergoes a large negative-voltage swing almost equal to E_{cc} before climbing toward its steady-state value 0 V. The time constant of this third phase is given by

$$\tau_3 = RC \tag{14}$$

In the present case, τ_3 equals 22 ns.

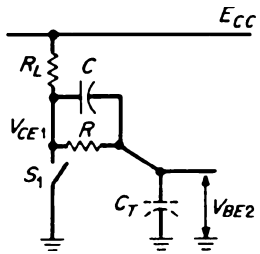

FIGURE 14.3.15 The longest time constant is experienced when T_1 is turned on. This is simulated by the closure of switch S_1.

The voltage variations versus time of the flip-flop circuit thus far analyzed are reviewed in Fig. 14.3.16 with the assumption that the regeneration time is negligible. Clearly *C* plays a double role. The first is favorable since it ensures fast regeneration and efficiently removes excess charges from the base of the saturated transistor, but the second is unfavorable since it increases the resolution time and sets an upper limit to the maximum repetition rate at which the flip-flop can be switched. The proper choice of *C* as well as of R_L and *R* must take this fact into consideration. Small values of the resistances make high repetition rates possible at the price of increased dc power consumption.

INTEGRATED-CIRCUIT FLIP-FLOPS

The Eccles-Jordan circuit (Fig. 14.3.12) is the basic structure of integrated bistable circuits. The capacitor *C* is not present.

The integrated flip-flop can be viewed as two cross-coupled single-input NOR or NAND circuits. In fact, integrated flip-flops vary only in the way external signals act upon them for control purposes. A typical example is given in Fig. 14.3.17 with the corresponding logic-symbol representation. The triggering inputs are called *set S* and *reset R* terminals. Transistors T_3 and T_4 are used for triggering.

The truth for NOR and NAND bistable circuits are

		NOR bistable			NAND bistable		
R	*S*	Q_1	Q_2	Line	Q_1	Q_2	Line
0	0	*Q*	*Q*	1	1	1	5
0	1	1	0	2	1	0	6
1	0	0	1	3	0	1	7
1	1	0	0	4	*Q*	*Q*	8

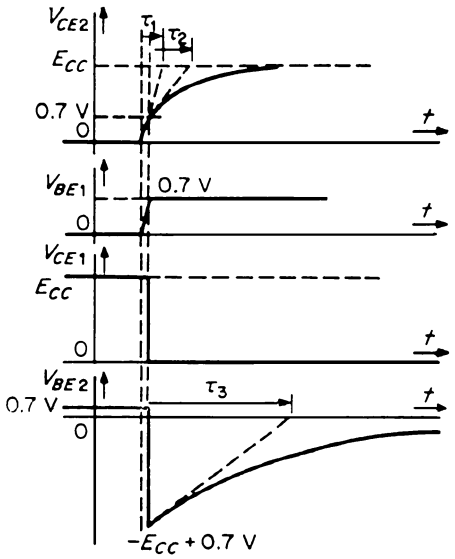

FIGURE 14.3.16 Voltage variations vs. time of flip-flop circuit.

Lines 1 and 8 correspond to situations where the S and R inputs are both inactive, leaving the bistable circuit in one of its two possible states indicated in the tables above by the letters Q and $\overline{Q}$ (Q may be either 1 or 0). If a specified output state is required, a pair of adequate complementary dc trigger signals is applied to the S and R inputs simultaneously.

For instance, if the output pair is to be characterized by $Q_1 = 1$ and $Q_2 = 0$, the necessary input combination, for NOR and NAND bistable circuits, is $S = 1$ and $R = 0$. Changing S back from 1 to 0 does not change anything in the output state in the NOR bistable. The same is true if S is made equal to 1 in the NAND bistable. In both cases, the flip-flop exhibits infinite memory of the stored state. The name *sequential circuit* is given to this class of networks as opposed to previous circuits, which are called combinational circuits.

Lines 4 and 5 must be avoided, for the passage from line 4 to line 1 or from line 5 to line 8 leads to uncertainty regarding the final state of the bistable circuit. In fact, the final transition is entirely out of the control of the input, since in both cases it results solely from small imbalances between transistor parasitics that allow faster switching of one or another inverter.

SYNCHRONOUS BISTABLE CIRCUITS[4]

Sequential networks may be either synchronous or asynchronous. The asynchronous class describes circuits in which the application of an input control signal triggers the bistable circuit immediately. This is true of the circuits thus far considered. In the synchronous class, changes of state occur only at selected times, after a clock signal has occurred.

Synchronous circuits are less sensitive to hazard conditions. Asynchronous circuits may be severely troubled by this effect, which results from differential propagation delays. These delays, although individually very small (typically of the order of a few nanoseconds), are responsible for introducing skew between signals that travel through different logic layers. Unwanted signal combinations may therefore appear for short periods and be interpreted erroneously.

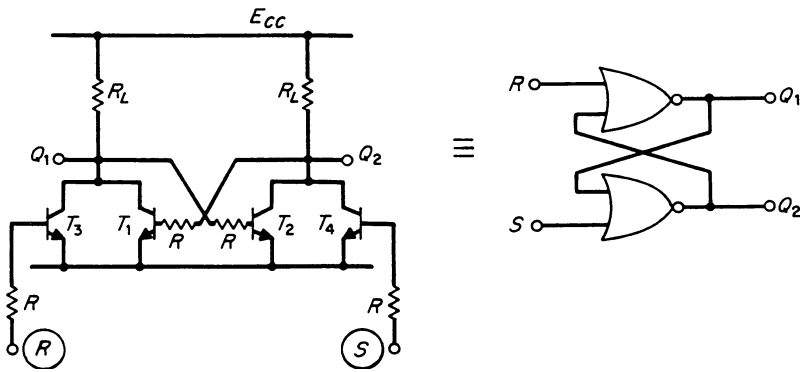

FIGURE 14.3.17 DC-coupled version of flip-flop, customarily used in integrated-circuit versions of this circuit.

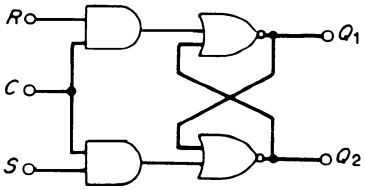

FIGURE 14.3.18 Synchronous flip-flop.

Synchronous circuits do not suffer from this limitation because they conform to the control signals only when the clock pulse is present, usually after the transient spurious combinations are over. A simple synchronous circuit is shown in Fig. 14.3.18. The inhibition action provided by the absence of the clock signal is provided by a pair of input AND circuits. Otherwise nothing is changed with respect to the bistable network.

A difficulty occurs in cascading bistable circuits, to achieve time-division. Instead of each circuit controlling its closest neighbor, when a clock signal is applied, the set and reset signals of the first bistable jump from one circuit to the next, traveling throughout the entire chain in a time which may be shorter than the duration of the clock transition. To prevent this, a time delay must be introduced between the gating NAND circuits and the actual bistable network, so that changes of state can occur only after the clock signal has disappeared.

One approach is to take advantage of storage effects in bipolar transistors, but the so-called *master-slave* association, shown in Fig. 14.3.19, is preferred. In this circuit, intermediate storage is realized by an auxiliary clocked bistable network controlled by the complement of the clock signal. The additional circuit complexity is appreciable, but the approach is practical in integrated-circuit technology.

The master-slave bistable truth table can be found from that of the synchronous circuit in Fig. 14.3.18, which in turn can be deduced from the truth table given in the previous section. One problem remains, however, the forbidden 1,1 input pair, which is responsible for ambiguous states each time the clock goes to zero. To solve this problem, the *JK* bistable was introduced (see Fig. 14.3.20). The main difference is the introduction of a double feedback loop. Hence the *S* and *R* inputs become, respectively, *JQ* and *KQ*. As long as the *J* and *K* inputs are not simultaneously equal to 1, nothing in fact is changed with respect to the behavior of the *SR* synchronous circuit.

When *J* and *K* are both high, the cross-coupled output signals fed back to the input gates cause the flip-flop to toggle under control of the clock signal. The truth table then becomes

J	K	Q_{n+1}	Line
0	0	Q_n	1
1	0	1	2
0	1	0	3
1	1	Q_n	4

Q_{n+1} stands for Q at the clock time $n + 1$ and Q_n for Q at clock time n. Lines 1 to 3 match the corresponding lines of the NOR bistable truth table. Line 4 indicates that state transitions occur each time the clock signal goes from high to low. The corresponding logic equation of the *JK* flip-flop, therefore, is

$$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n \tag{15}$$

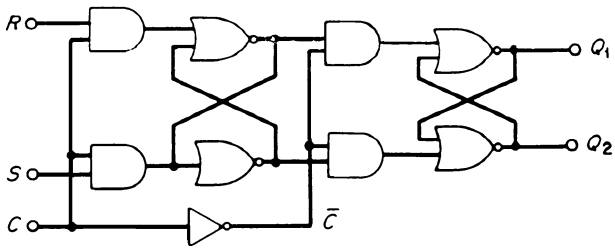

FIGURE 14.3.19 Master-slave synchronous flip-flop.

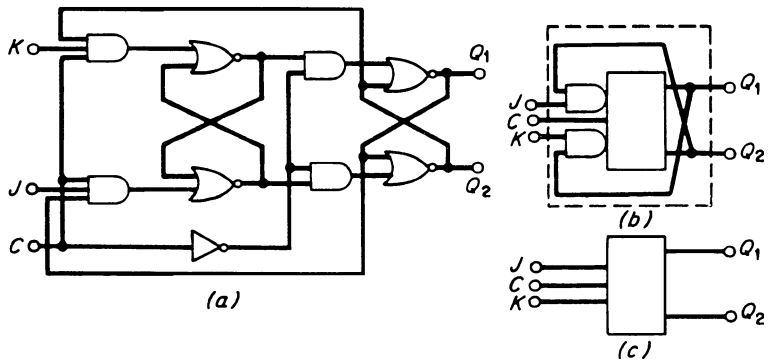

FIGURE 14.3.20 *JK* Flip-flop.

When only one control signal is used, J, for instance, and K is obtained by negation of the J signal, a new type of bistable is found, which is called the D flip-flop. The name given to the J input is D. Since K is equal to J, Eq. (15) reduces to

$$Q_{n+1} = D \tag{16}$$

Hence, in this circuit the output is set by the input D after a clock cycle has elapsed. Notice that the flip-flop is insensitive to changes of D occurring while the clock is high.

D flip-flops without the master-slave configuration also exist, but their output state follows the D signal if changes occur while the clock is high. These bistables can be used to latch data. Several D flip-flops controlled by the same clock form a register for data storage. The clock signal then is called an enable signal.

Bistable Circuits, Emitter-Coupled Bistables (Schmitt Circuits)[6]

In the basic Schmitt circuit represented in Fig. 14.3.21 bistable operation is obtained by a positive-feedback loop formed by the common-base and common-collector transistor pair (respectively T_1 and T_2). The Schmitt circuit can be considered as a differential amplifier with a positive-feedback loop, which is a series-parallel association.

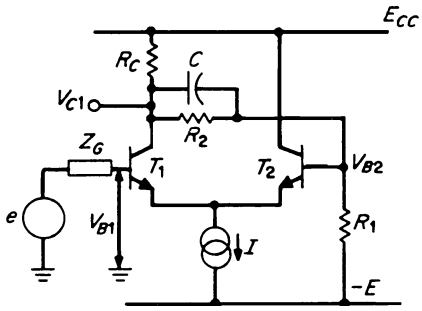

FIGURE 14.3.21 Emitter-coupled Schmitt circuit, showing positive-feedback loop.

Emitter-coupled bistables are fundamentally different from Eccles-Jordan circuits, since no transistor saturates in either of the two stable states. Storage effects therefore need not be considered.

The two permanent states are examined in Fig. 14.3.22. In each state, (*a*) as well as (*b*), one transistor operates in the common-collector configuration while the other is blocked. In Fig. 14.3.22*a*, the collector voltage V_{C1} of T_1 and base voltage V_{B2} of T_2 are given by

$$V_{C1} = E_{cc}\frac{R_1 + R_2}{R_1 + R_2 + R_c}$$
$$V_{B2} = E_{cc}\frac{R_1}{R_1 + R_2 + R_c} = V_h \tag{17}$$

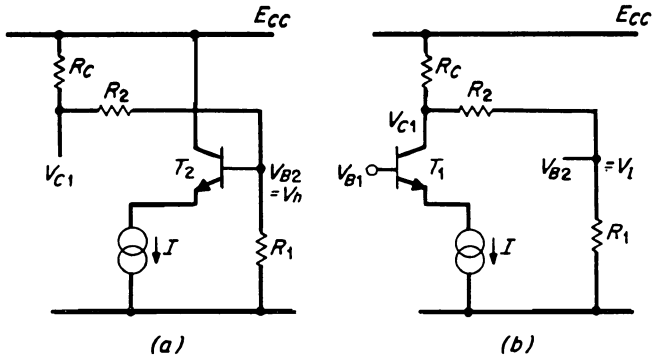

FIGURE 14.3.22 Execution of transfer in Schmitt circuit: (*a*) with T_1 blocked; (*b*) with T_1 conducting.

When the other stable state (*b*) is considered,

$$V_{C1} = (E_{cc} - R_c I)\frac{R_1 + R_2}{R_1 + R_2 + R_c}$$

$$V_{B2} = (E_{cc} - R_c I)\frac{R_1}{R_1 + R_2 + R_c} = V_l \tag{18}$$

The situation depicted in Fig. 14.3.22 remains unchanged as long as the input voltage V_{B1} applied to T_1 is kept below the actual value V_h. In the other state (*b*), T_2 will be off as long as V_{B1} is larger than V_l. A range of input voltages between V_h and V_l thus exists where either of the two states is possible.

To alleviate the ambiguity, let us consider an input voltage below the smallest of the two possible values of V_{B2} so that the transistor T_1 necessarily is blocked. This corresponds to the situation of Fig. 14.3.22*a*. Now let the input voltage be gradually increased. Nothing will happen until V_{B1} approaches V_h. When the difference between the two base voltages is reduced to 100 mV or less, T_1 will start conducting and the voltage drop across R_c will lower V_{B2}. The emitter current of T_2 will consequently be reduced, and more current will be fed back to T_1. Hence, an unstable situation is created, which ends when T_1 takes over all the current delivered by the current source and T_2 is blocked.

Now the situation depicted in Fig. 14.3.22*b* is reached. The base voltage of T_2 becomes V_l, and the input voltage may either continue to increase or decrease without anything else happening as long as V_{B1} has not reached V_l. When V_{B1} approaches V_l, another unstable situation is created causing the switching from (*b*) to (*a*). Hence, the input-output characteristic of the Schmitt trigger is as shown in Fig. 14.3.23 with a hysteresis loop.

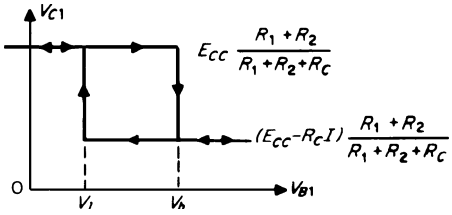

FIGURE 14.3.23 Input-output characteristic of Schmitt circuit, showing rectangular hysteresis.

Schmitt triggers are suitable for detecting the moment when an analog signal crosses a given *DC* level. They are widely used in oscilloscopes to achieve time-base synchronization. This is illustrated in Fig. 14.3.24, which shows a periodic signal triggering a Schmitt circuit and the corresponding output waves. It is possible to modify the switching levels by changing the operating points of the transistors electrically, e.g., by modifying the current delivered by the current source.

In many applications, the width of the hysteresis does not play a significant role. The width can be decreased, however, by increasing the attenuation of the resistive divider formed by R_1 and R_2, but one should not go below 1 V because sensitivity to variations in circuit components or supply voltage may occur.

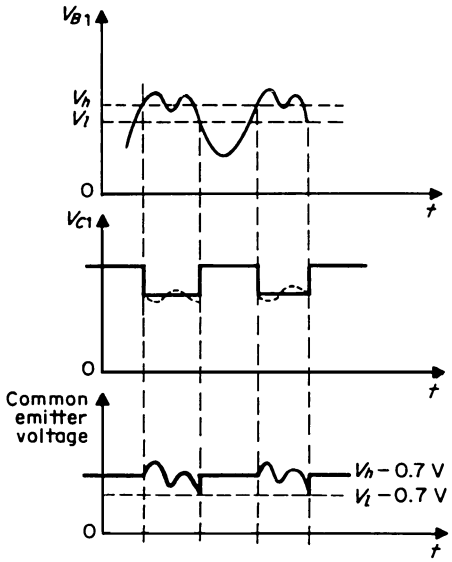

FIGURE 14.3.24 Trigger input and output voltage of Schmitt circuit; solid line delivered by a current source; broken line delivered by a resistor.

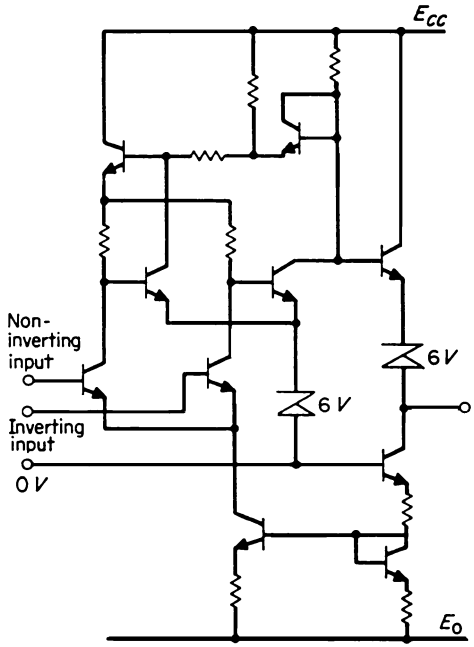

FIGURE 14.3.25 Bipolar integrated version of a comparator.

Furthermore, the increased attenuation in the feedback loop must be compensated for by a corresponding increase in the differential amplifier gain. Otherwise the loop gain may fall below 1, preventing the Schmitt circuit from functioning. A hysteresis of a few millivolts is therefore difficult to achieve.

A much better solution is to use *comparators* instead of Schmitt triggers when hysteresis must be avoided. A typical integrated comparator is shown in Fig. 14.3.25. It is a medium-gain amplifier (10^3 to 10^4) with a very fast response (a few nanoseconds) and an excellent slew rate. Comparators are not designed to be used as linear amplifiers like op-amps. Their large gain-bandwidth product makes them inappropriate for feedback configurations. They inevitably oscillate in any type of closed loop. In the open-loop configuration they behave like clipping circuits with an exceedingly small input range, which is equal to the output-voltage swing, usually 5 V, divided by the gain. The main difference compared with Schmitt triggers is the fact that comparators do not exhibit hysteresis. This makes a significant difference when considering very slowly varying input signals.

In the circuit of Fig. 14.3.21 the common-emitter current source can be replaced by a resistor. This solution introduces some common-mode sensitivity. The output signal does not look square, as shown in Fig 14.3.24 by the dashed lines. If unwanted, this effect can be avoided by taking the output signal at the collector of T_2 through an additional resistor, since the current flowing through T_2 is constant. An additional advantage of the latter circuit is that the output load does not interfere with the feedback loop.

INTEGRATED-CIRCUIT SCHMITT TRIGGERS[7]

Basically a Schmitt trigger can always be implemented by means of an integrated differential amplifier and an external positive-feedback loop. If the amplifier is an op-amp, poor switching characteristics are obtained unless an amplifier with a very high slewing rate is chosen. If a comparator is considered instead of an op-amp, switching will be fast but generally the output signal will exhibit spurious oscillations during the transition period. The oscillatory character of the output signal is due to the trade-off between speed and stability which is typical of comparators compared with op-amps. Any attempt to create a dominant pole, in fact, inevitably would ruin their speed performance.

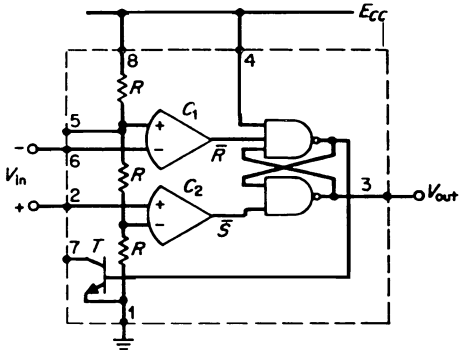

FIGURE 14.3.26 Precision integrated Schmitt trigger.

The integrated-circuit counterpart of the Schmitt trigger is shown in Fig. 14.3.26. It consists of two comparators connected to a resistive divider formed by three equal resistors R. Input terminals 2 and 6 are normally tied together. The output signals of the two comparators control a flip-flop. When the input voltage is below $E_{cc}/3$, the flip-flop is set. Similarly when the input voltage exceeds $2E_{cc}/3$, the circuit is reset.

The actual state of the flip-flop in the range between $E_{cc}/3$ and $2E_{cc}/3$ will depend on how the input voltage enters the critical zone. For instance, if the input voltage starts below $E_{cc}/3$ and is increased so that it changes the state of comparator C_2 but not that of comparator C_1, both S and R are equal to 1 and the flip-flop remains set. The state changes only if the input voltage exceeds the limit $2E_{cc}/3$. Similarly, if the input voltage is lowered, setting the flip-flop will occur only when $E_{cc}/3$ is reached. Hence the circuit of Fig. 14.3.26 behaves like a Schmitt trigger with a hysteresis width $E_{cc}/3$ depending only on the resistive divider $3R$ and the offset voltages of the two comparators C_1 and C_2. This circuit can therefore be considered as a precision Schmitt trigger and is widely used as such.

Monostable and Astable Circuits (Discrete Components)[4]

Figures 14.3.27 and 14.3.28 show monostable and astable collector-coupled pairs, respectively. The fundamental difference between these circuits and bistable networks lies in the way DC biasing is achieved. In Fig. 14.3.27*a*, T_2 is normally conducting except when a negative trigger pulse drives this transistor into the cutoff region. T_1 necessarily undergoes the inverse transition, suddenly producing a large negative voltage step at the base of T_2 shown in Fig. 14.3.27*b*. V_{BE2}, however, cannot remain negative since its base is connected to the positive-voltage supply through the resistor R_1. The base voltage rises toward E_{cc}, with a time constant R_1C. As soon as the emitter junction of T_2 becomes forward-biased, the monostable circuit changes its state again and the circuit remains in that state until another trigger signal is applied.

The time T between the application of a trigger pulse and the instant T_2 saturates again is given approximately by

$$T = \tau \ln 2 = 0.693\tau \tag{19}$$

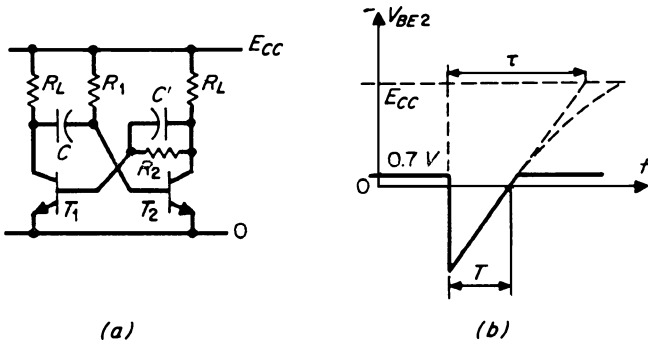

FIGURE 14.3.27 Monostable collector-coupled pair: (*a*) circuit; (*b*) output vs. time characteristics.

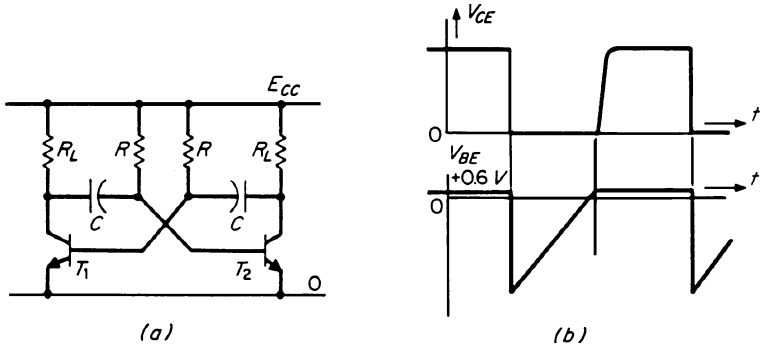

FIGURE 14.3.28 Astable (free-running) flip-flop: (*a*) circuit; (*b*) output vs. time characteristics.

where $\tau = R_1 C$. The supply voltage E_{CC} is supposed to be large compared with the forward-voltage drop of the emitter junction of T_2 for this expression to apply.

The astable collector-coupled pair, or free-running multivibrator (Fig. 14.3.28), operates according to the same scheme except that steady-state conditions are never reached. The base-bias networks of both transistors are connected to the positive power supply. The period of the multivibrator thus equals $2T$ if the circuit is symmetrical, and the repetition rate F, is given by

$$F_r = \frac{1}{2\tau \ln 2} \approx \frac{0.7}{RC} \tag{20}$$

INTEGRATED MONOSTABLE AND ASTABLE CIRCUITS[7]

The discrete component circuits discussed above are interesting only because of their inherent simplicity and exemplative value. Improved means to integrate monostable and astable are shown below.

The circuit shown in Fig. 14.3.29 is derived from the Schmitt trigger. It is widely used in order to implement high-frequency (100 MHz) relaxation oscillators. The capacitor C provides a short circuit between the emitters of the two transistors, closing the positive-feedback loop during the regeneration time. As long as one or the other of the two transistors is cut off, C offers a current sink to the current source connected to the emitter of the blocked transistor. The capacitor thus is periodically charged and discharged by the two current sources, and the voltage across its terminal exhibits a triangular waveform. The collector current of T_1 is either zero or $I_1 + I_2$, so that the resulting voltage step across R_c is $(R_B \,||\, R_C)(I_1 + I_2)$. Since the base of T_2 is directly connected to the collector of T_1, the same voltage step controls T_2 and determines the width of the input hysteresis, i.e., the maximum amplitude of the voltage sweep across C. The period of oscillation is computed from

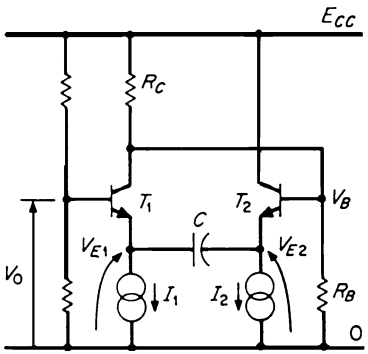

FIGURE 14.3.29 Discrete-component emitter-coupled astable circuit.

$$T = C\left(\frac{1}{I_1} + \frac{1}{I_2}\right)(R_B \,\|\, R_C)(I_1 + I_2) \tag{21}$$

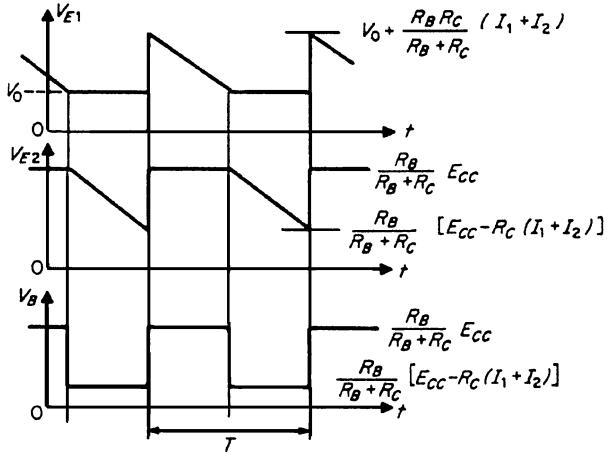

FIGURE 14.3.30 Waveforms of circuit in Fig. 14.3.29.

When, as is usual, both current sources deliver equal currents, the expression for T reduces to

$$T = 4(R_B \parallel R_C)C \tag{22}$$

T does not depend, in this case, on the amplitude of the current because changes in current in fact modify the amplitude and the slope of the voltage sweep across C in the same manner. A review of the waveforms obtained at various points of the circuit is given in Fig. 14.3.30.

Integrated monostable and astable circuits can be derived from the precision Schmitt trigger circuit shown in Fig. 14.3.26. The monostable configuration is illustrated in Fig. 14.3.31.

Under steady-state conditions, the flip-flop is set and the transistor T saturated. The input voltage V_{in} is kept somewhere between the two triggering levels $E_{cc}/3$ and $2E_{cc}/3$. To initiate the monostable condition, it is sufficient that V_{in} drops below $E_{cc}/3$ even for a very short time, in order to reset the flip-flop and prevent T from conducting. The current flowing through R_1 then charges C until the voltage V_C reaches the triggering level

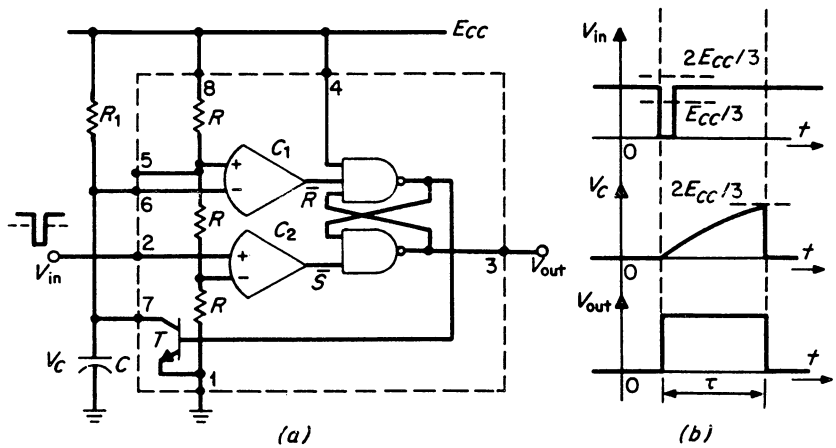

FIGURE 14.3.31 Monostable precision Schmitt trigger: (*a*) circuit; (*b*) waveforms.

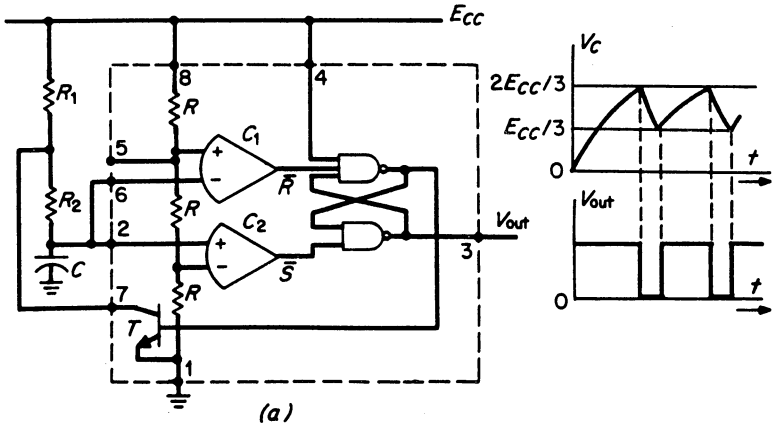

FIGURE 14.3.32 Astable precision Schmitt trigger: (*a*) circuit; (*b*) waveforms.

$2E_{cc}/3$. Immediately thereafter, the circuit switches to the opposite state and transistor T discharges C. The monostable circuit remains in that state until a new triggering pulse V_{in} is fed to the comparator C_2. The waveforms V_{in}, V_C, and V_{out} are shown in Fig. 14.3.31*b*. This circuit is also called a *timer* because it provides constant-duration pulses, triggered by a short input pulse. A slight modification of the external control circuitry may change this monostable into a retriggerable timer.

The astable version of the precision Schmitt trigger is shown in Fig. 14.3.32. Its operation is easily understood from the preceding discussion. The capacitor C is repetitively discharged through R_2 in series with the saturated transistor T and recharged through $R_1 + R_2$. The voltage V_C therefore consists of two distinct exponentials clamped between the triggering levels $E_{cc}/3$ and $2E_{cc}/3$. The frequency is equal to $1.44/(R_1 + 2R_2)C$. Because of the precision of the triggering levels (10^{-3} to 10^{-4}) short-term frequency stability can be achieved.