CHAPTER 21.2
VIDEO SIGNAL SYNCHRONIZING SYSTEMS

Richard A. Kupnicki

TYPES OF SYNCHRONIZATION DEVICES

Video synchronization is the process of aligning or matching two or more dissimilar signals with respect to their timing relationship. In order to fulfill this function, it is first necessary to have a reference video signal such as that produced by a master or a slave sync generator. Then it is necessary to perform the actual signal synchronization using a frame synchronizer.

The three types of synchronization devices which will be discussed herein are the master sync generator, the slave sync generator, and the frame synchronizer. Each fulfills a specific, independent function within the television facility. For each, there are often subgroups which relate to the different video signal formats.

The master sync generator is usually free running and is used as a lock source for all other devices within the facility. The master generator is further characterized by its own high-stability internal oscillator. Frequently two master sync generators will be used together in conjunction with an automatic change over unit in order to minimize the impact of equipment failure. A master sync generator does not need to lock a reference input signal. Sometimes a high stability frequency source may be used as a reference in critical applications.

A slave sync generator will have all the attributes of the master with the addition of circuits to allow the generator to lock to an incoming reference sync signal (generated by a master). Some design savings are generally achieved in the slave generator by relaxing the specifications of the local oscillator circuits. The main purpose of the slave generator is to produce a local sync reference, with timing capability, thus permitting timing offsets with respect to the master generator. Note that as a good practice, color black should be used as the reference video signal due to its constant average picture level (APL) in order to minimize jitter introduced into the phase lock loop.

A video frame synchronizer is used whenever it is necessary to bring an unrelated video source back into timing relationship within a facility. A typical example of this requirement would be a satellite feed or other external source. As well as providing the necessary timing controls, the majority of frame synchronizers will also provide some measure of video conditioning (processing amplifier functions) such as video level control and hue control.

A modern television studio processes audio along with video. Use of frame synchronizers in the signal paths adds considerable delay to the video signal, to the point where video gets delayed more than audio. A human finds it objectionable when audio is more than one video frame ahead or two frames behind its associated video signal. To avoid this problem, audio must be delayed to the same degree as video. To aid in audio synchronization process a suitable reference signal, digital audio reference signal (DARS) needs to be generated by the master or slave sync generators. SMPTE time code is also generated to aid in editing of audio and video streams.

MULTI-STANDARD SLAVE SYNCHRONIZING GENERATOR

Slave sync generators are generally used to provide a local color black reference signal which is locked to a master sync generator system, either directly or via a distribution system.

The use of slave sync generators is an integral part of any television or related facility. They provide a means for timing local devices or groups of devices to a common master reference. Modern slave sync generators will generally always provide an infinite phasing capability, thus allowing the timing outputs of the slave generator to be located anywhere in time relative to the master generator. *Infinite phasing* refers to the capability to adjust vertical phase anywhere within a color frame. "H" phasing refers to adjustments within a line and "fine" phasing refers to adjustment within a subcarrier cycle.

A complete block functional diagram of a slave synchronizing generator (Fig. 21.2.1) should be used as a reference for the following description. The figure shows a multi-standard generator capable of locking to and generating reference NTSC and PAL signals. The implementation differences are summarized in Table 21.2.1, as it is practical to build one piece of hardware with programmable registers to satisfy the requirements of both television systems. In general practice, analog NTSC is used as a reference for all 29.97-frame-per-second-based systems and analog PAL as reference for 25-frame-per-second-based systems.

The reference signal's color burst component is separated using a bandpass filter. The stripped color burst signal is then fed to the complex multiplier. The subcarrier generator block generates two other signals referred to as Sin and Cos since they have a quadrate relationship. The subcarrier generator is composed of an accumulator feeding a set of Sin and Cos ROM look up tables. The ROM outputs are converted to analog via a DAC before feeding the multipliers. The multiplier output is low-pass filtered to retain the difference frequencies, i.e., the frequency error between the crystal oscillator and the input signal. In PAL applications,

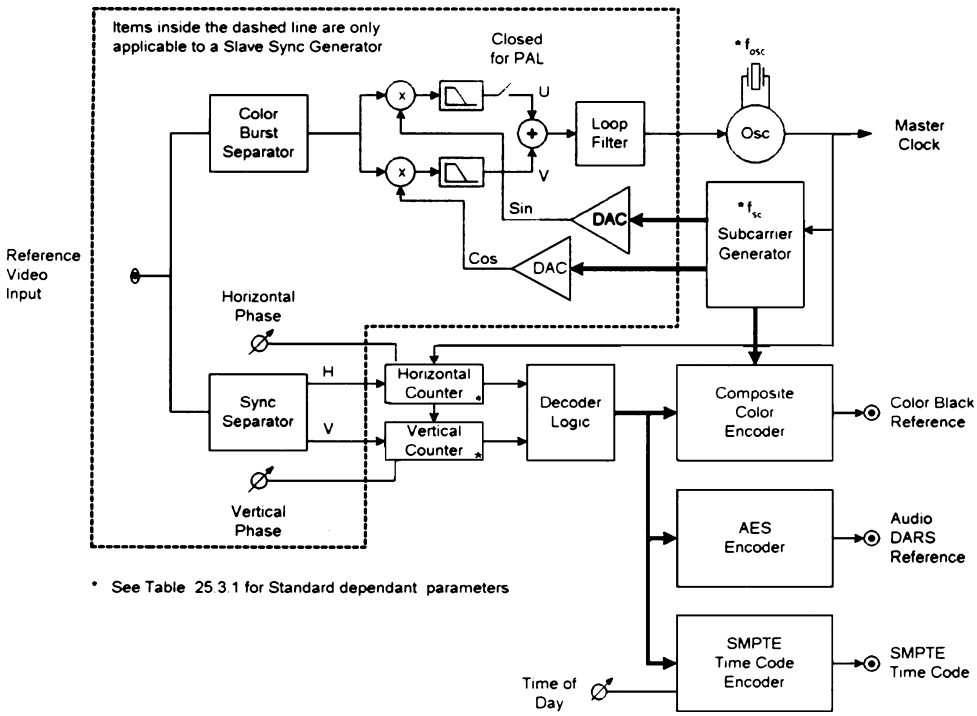

FIGURE 21.2.1 Multi-Standard Sync generator.

TABLE 21.2.1 Standard Related Parameters

Reference video standard	f_{osc}(MHz)	f_{sc}(MHz)	Horizontal counter counts	Vertical counter counts
NTSC	13.5	3.579545	858	525
PAL	13.5	4.43361875	864	625

both filtered axis (U and V) are summed together in order to average the swinging color burst. The resultant error is further filtered by a loop filter before it is applied to the voltage controlled crystal oscillator (VCXO). The oscillator output drives the subcarrier generator as previously described, thus closing the loop. Fine phasing can be implemented by placing an adder between the accumulator and ROM tables in the subcarrier generator. Adding a constant has the effect of statically rotating the sinusoids, thus achieving a phase offset between the input and output and a phasing resolution in the subnanosecond range.

The generation of the blanking interval pulses is performed by two very similar circuits running at horizontal (H) and vertical (V) rates, respectively. The H logic is composed of 858 counter counts for NTSC and 864 counter counts for PAL, which is clocked by the local crystal oscillator running at 13.5 MHz. The output of the counter function is a 10-bit address to a look up table. The H counter is itself synchronized by using the horizontal sync from the reference video input and using the leading edge to preload the counter. The instantaneous load value at the time of initiation of the load defines the relative H timing output to input.

Generation of the vertical pulses is almost identical to the horizontal except that the counter length is 525 for NTSC and 625 for PAL and the clock used is twice the horizontal rate (31.5 kHz) derived from the horizontal counter and look up table decoder.

The respective outputs of both the horizontal and vertical decoders are gated together in a decoder logic block to produce the required final composite outputs of sync, burst flag, and blanking.

Having derived the ingredient signals, the remaining task is to generate the actual output reference signals. In the past, up to the mid-1990s, a reference synchronization generator would generate the basic drive signals (color subcarrier, sync, burst flag, composite blanking), since the process of encoding and decoding was expensive and cumbersome. At the same time one had to deal with routing and timing of multiple signals. With the advancements in silicon, encoding of the drive signals into one composite signal became the norm. When encoding video it is important to remember to transfer the color frame relationship of the input reference signal to the generated reference signal. In addition, generation of audio DARS reference and SMPTE time code are considered to be important functions performed by a sync generator.

The following standards best described the parameters associated with the reference signals mentioned previously.

Reference signal	Associated standard
Video	SMPTE 170M and SMPTE 318M
Audio (DARS)	AES 3, AES 5, and AES 11
Time code	SMPTE 12M

MULTI-STANDARD MASTER SYNCHRONIZING GENERATOR

Master sync generators are generally used in pairs, via an automatic change over device, as the primary reference for a facility. The design of a master generator is in some ways much simpler than a slave since sections of circuitry are simply removed, as can be seen from Fig. 21.2.1. However, the remaining circuits are usually upgraded to meet the tight tolerances required for a master generator, particularly in the case of the crystal oscillator.

Referring to Fig. 21.2.1, it can be seen that the phase lock loop and associated circuit are deleted and the oscillators left to free run. In television plants where interchange of program material extends beyond the plant

boundaries and the production is a live event (e.g., the Olympics), it is desirable to lock the oscillator to an external high stability reference, like an atomic standard or GPS. In this case the internal oscillator is placed in a PLL configuration with an external input. The dividers need to be selected so the comparator sees the same frequency from the forward the feedback paths.

The internal crystal oscillator of a master sync generator is generally of very high quality to maintain the required specification of 3.579545 MHz ± 10 Hz maximum variation over the operating temperature range and in conjunction with the aging of the crystal.

Two methods are used to maintain a consistent environment for the internal crystal oscillator. The first method has the crystal enclosed in an oven, which is maintained at a constant temperature, typically 66°C (high enough such that the ambient temperature is not a factor). This has the associated drawbacks of considerable power consumption and being able to achieve this temperature instantaneously upon power up. The second method uses a temperature compensation network where the temperature is sensed and a control voltage for the VCO is offset.

There is an interesting derivative of the oven approach, which relies on operation of the crystal closer to the ambient room temperature. In this scenario, if the ambient temperature is above the set crystal temperature, cooling is required and vice versa. This is accomplished using a device based on the Peltier Effect for both heating and cooling under closed loop control.

VIDEO FRAME SYNCHRONIZER

A frame synchronizer is a device that accepts video information at one rate and provides an output that is "in time" with respect to a reference. Synchronization is achieved by writing the incoming video into memory at one rate, and then reading it out at a rate locked to the facility reference (master sync generator). The memory, therefore, acts as a buffer, allowing the data to accumulate prior to discharge.

A mechanical example to illustrate this buffering action of memory would be a stream flowing downhill into a reservoir contained by a dam. At the bottom of the dam the water is discharged at a constant rate. The volume of water the stream is supplying can increase or decrease, but the water discharged at the bottom of the dam will remain constant due to the buffering action of the accumulating water in the reservoir.

A complete functional block diagram of a typical frame synchronizer (Fig. 21.2.2) should be used as a reference for the following description.

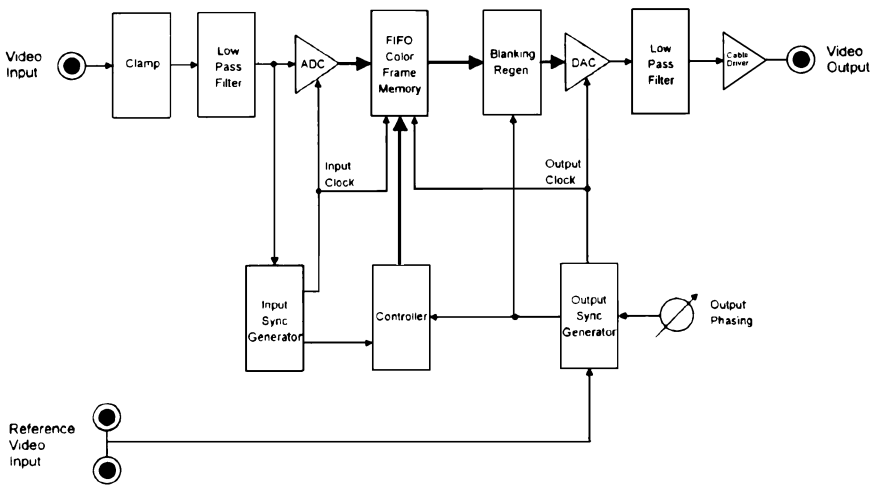

FIGURE 21.2.2 Typical video frame synchronizer.

VIDEO SIGNAL SYNCHRONIZING SYSTEMS

The input video is first clamped in order to establish a known dc level, which is within the window of the analog-to-digital converter. This is followed by a low-pass filter that prevents any harmonics above one-half the sampling frequency (14.31818 MHz in the case of NTSC) from passing through, thus satisfying the Nyquist sampling criteria.

The signal is then digitized using either an 8- or 10-bit converter. The choice of 8 or 10 bits is the determining factor in frame synchronizer classes. Higher end applications will use 10-bit quantization. However, this is a cost versus performance function.

The digital video data are then stored in a FIFO memory where, after a period of time, it is read back out. New blanking is inserted into the signal and the information is then converted back into the analog domain and low-pass filtered.

Information is required for both the input and output processing sections for the purposes of timing. This is produced by the input and output sync generator sections, as illustrated in Fig. 21.2.2.

The input sync generator samples the incoming video signal and locks a local oscillator to the incoming subcarrier at a 4 fsc rate (fsc = the frequency of the subcarrier). The horizontal and vertical portions of the incoming signal are decoded to provide the information required by the controller and subsequent memory.

The output sync generator performs a similar function except that it samples an external video reference in order to establish a timing reference and clock for the output video. The output sync generator also provides phasing capability which permits the positioning of the output video signal anywhere in time with respect to the reference video signal.

MEMORY

The quantity of memory used must be enough to store one complete color frame of video. This is the smallest unit of video, which can be deleted or repeated while still maintaining the proper color relationship. This means four fields of video in the case of NTSC and eight fields in the case of PAL video signals. It is worthwhile to note that some video frame synchronizers store the complete video line, blanking included, while others store only the active portion of the line.

The most common type of memory used is DRAM where the controller provides read and write addressing. The latest trend is to use FRAM (Field RAM) which employs a FIFO structure and only read and write pointer resets need be provided by the controller.

It is necessary to provide a mechanism such that memory addressing is synchronized to the sync structure of the video signal. For example, if pixel 1 of line 1 is written into location X of the memory, at the time that location X is read back, that information must be placed back on line 1, pixel 1 of the output sync structure. In the case where FRAM is used, this is accomplished by generating a write/reset pulse coincident with the leading edge of sync of the first full line in the vertical interval of field 1 in the color frame sequence based on the input sync generator. Similarly, the read/reset is generated in the same manner, except it is based on the output sync generator. In the case of DRAM memory, the controller will contain read and write address counters that are reset with pulses as described in the FRAM implementation.

FRAME SYNCHRONIZERS WITH DIGITAL I/O

The emergence of digital video standards has increased the importance of frame synchronizers because of the increased processing throughout delays associated with digital equipment. The structure of the frame synchronizer is easily adapted to digital interface in either the parallel or serial video domains.

The analog-to-digital and digital-to-analog converter sections are replaced with the appropriate digital interface, and the input sampling clock is derived directly from the incoming video signal rather than having to extract this information (these codes are embedded directly as part of the digital signal's structure). The output sync generator remains the same since the majority of house reference signals are still analog color black. The change over to a digital house reference will likely happen in the future. Once this does happen, the output sync generator will shift in appearance to that of the input sync generator just described.

BIBLIOGRAPHY

Application Note: Field and Frame Synchronizers, Leitch Technology Int.

AES3-1992 AES recommended practice for digital audio engineering—serial transmission format for linearly represented digital audio data. Audio Engineering Society, 1992.

AES5-1984 AES recommended practice for professional digital audio applications employing pulse code modulation Preferred Sampling Frequencies. Audio Engineering Society, 1984.

AESII-1997 AES recommended practice for digital audio engineering—Synchronization of digital audio equipment in studio operations.

EBU Tech. 6267 EBU Interfaces for 625-line Digital Video Signals at the 4:2:2 Level of CCIR Recommendation 601 (2nd ed., 1992).

ITU-R BT.470-6 Conventional Television Systems.

Kano, K., et al. Television Frame Synchronizer, *SMPTE J.*, March 1975.

Kupnicki, R., et al. Digital Processing in the DPS-I, *SMPTE, Digital Video*, Vol. 2, March 1979.

Kupnicki, R., Software Based Digital Signal Processing, *SMPTE, Digital Video*, Vol. 3, June 1980.

SMPTE 12M-1999 For Television, Audio and Film—Time and Control Code.

SMPTE 170M-1999 Composite Analog Video Signal-NTSC for Studio Applications.

SMPTE 259M-1997 10-Bit 4:2:2 Component and 4fsc Composite Digital Signal Serial Digital Interfaces.

SMPTE 318M-1999 For Television and Audio—Reference Signals for the Synchronization of 59.94- or 50-Hz Related Video and Audio Systems in Analog and Digital Areas.