Design Verification and Test of Digital VLSI Circuits - Video course

COURSE OUTLINE

Digital VLSI Design flow comprises three basic phases: Design, Verification and Test. The video course would cover theoretical, implementation and CAD tools pertaining to these three phases. Although there can be individual full courses for each of these phases, the present course aims at covering the important problems/algorithms/tools so that students get a comprehensive idea of the whole digital VLSI design flow.

VLSI Design: High level Synthesis, Verilog RTL Design, Combinational and Sequential Synthesis Logic Synthesis (for large circuits).

Verification Techniques: Introduction to Hardware Verification and methodologies, Binary Decision Diagrams(BDDs) and algorithms over BDDs, Combinational equivalence checking, Temporal Logics, Modeling sequential systems and model checking, Symbolic model checking.

VLSI Testing: Introduction, Fault models, Fault Simulation, Test generation for combinational circuits, Test generation algorithms for sequential circuits and Built in Self test.

COURSE DETAIL

S.No	Details
1.	**Design**
	Module I: Introduction Lecture I: Introduction to Digital VLSI Design Flow Lecture II: High Level Design Representation Lecture III: Transformations for High Level Synthesis
	Module II: Scheduling, Allocation and Binding Lecture I: Introduction to HLS: Scheduling, Allocation and Binding Problem Lecture II and III: Scheduling Algorithms Lecture IV: Binding and Allocation Algorithms
	. **Module III: Logic Optimization and Synthesis** Lecture I,II and III: Two level Boolean Logic Synthesis Lecture IV: Heuristic Minimization of Two-Level Circuits Lecture V: Finite State Machine Synthesis Lecture VI: Multilevel Implementation
2.	**Verification**

NPTEL

http://nptel.iitm.ac.in

Computer Science and Engineering

Pre-requisites:

1. Digital Design
2. Algorithm
3. Automata Theory (Basics)

Coordinators:

Dr. Santosh Biswas
Department of Computer Science and EngineeringIIT Guwahati

Jatindra Kumar Deka
Department of Computer Science and EngineeringIIT Guwahati

	Module - IV: Temporal Logic Lecture-I: Introduction to formal methods for verification Lecture-II: Temporal Logic: Introduction and Basic Operators Lecture-III: Syntax and Semantics of CTL Lecture IV: Equivalence between CTL Formulas
	Module - V: Binary Decision Diagram Lecture-I: Binary Decision Diagram: Introduction and construction Lecture-II: Ordered Binary Decision Diagram Lecture-III: Operations on Ordered Binary Decision Diagram Lecture-IV: Ordered Binary Decision Diagram for Sequential Circuits
	Module-VI: Verification Techniques Lecture-I: Introduction to Verification Techniques Lecture-II and III: Model Checking Lecture-IV and V: Symbolic Model Checking
3.	**Test**
	Module VII: Introduction to Digital Testing Lecture-I: Introduction to Digital VLSI Testing Lecture-II: Functional and Structural Testing Lecture-III: Fault Equivalence
	Module VIII: Fault Simulation and Testability Measures Lecture-I, II and III: Fault Simulation Lecture-IV: Testability Measures (SCOAP)
	Module IX: Combinational Circuit Test Pattern Generation Lecture-I: Introduction to Automatic Test Pattern Generation (ATPG) and ATPG Algebras Lecture-II and III: D-Algorithm
	Module X: Sequential Circuit Testing and Scan Chains Lecture-I: ATPG for Synchronous Sequential Circuits Lecture-II and III: Scan Chain based Sequential Circuit Testing
	Module XI: Built in Self test (BIST) Lecture I and II: Built in Self Test Lecture III and IV: Memory Testing

References:

1. D. D. Gajski, N. D. Dutt, A.C.-H. Wu and S.Y.-L. Lin, High-Level Synthesis: Introduction to Chip and System Design, Springer, 1st edition, 1992.

2. S. Palnitkar, Verilog HDL: A Guide to Digital Design and Synthesis, Prentice Hall, 2nd edition, 2003.

3. G. De Micheli. Synthesis and optimization of digital circuits, 1st edition, 1994.
4. M. Huth and M. Ryan, Logic in Computer Science modeling and reasoning about systems, Cambridge University Press, 2nd Edition, 2004
5. Bushnell and Agrawal, Essentials of Electronic Testing for Digital, Memory & Mixed-Signal Circuits, Kluwer Academic Publishers, 2000