Module 5 (Lectures 21-24) Pipelined processors

1. Pipelining is a processor implementation technique that improves performance by
    a) reducing the amount of time that it takes to execute 1 instruction
    b) increasing the rate at which instructions complete execution
    c) allowing more than one instruction to complete execution at the same time
    d) reducing the likelihood that consecutive instructions are dependent on each other
2. Hazards are undesirable in pipelined processors as they
    a) complicate the design of the instruction set architecture
    b) affect the correctness of program execution
    c) necessitate the use of very high frequency clocks
    d) cause there to be more cycles in which no instruction completes execution
3. What kind of hazard does the sequence of MIPS 1 instructions shown below suffer from?

        ADDI R1, R3, 2
        SUB R2, R1, R3

    a) RAW
    b) WAR
    c) WAW
    d) Control
4. What kinds of hazards does the sequence of MIPS 1 instructions shown below suffer from?

        ADDI R1, R3, 2
        SUB R1, R1, R3

    e) RAW and WAW
    f) WAR and RAW
    g) WAW and WAR
    h) Control
5. The technique of bypassing or forwarding is used to address
    a) control hazards
    b) RAW hazards
    c) WAR hazards
    d) WAW hazards