Module 6 (Lectures 25-31) Cache memory

A computer system has a 32KByte direct mapped cache with 16Byte block size. The processor sends 32bit data addresses to the cache controller for data accesses.

1. The number of address bits used as block offset are
   a) 4
   b) 5
   c) 6
   d) 7
2. The number of address bits used as cache index are
   a) 9
   b) 10
   c) 11
   d) 12
3. The number of address bits used in tag comparison are
   a) 15
   b) 16
   c) 17
   d) 18
4. The number of entries in the cache tag directory are
   a) 1023
   b) 2000
   c) 2047
   d) 2048
5. The extent to which spatial locality of reference is exploited by a cache is determined by the
   a) address size
   b) block size
   c) associativity
   d) replacement policy