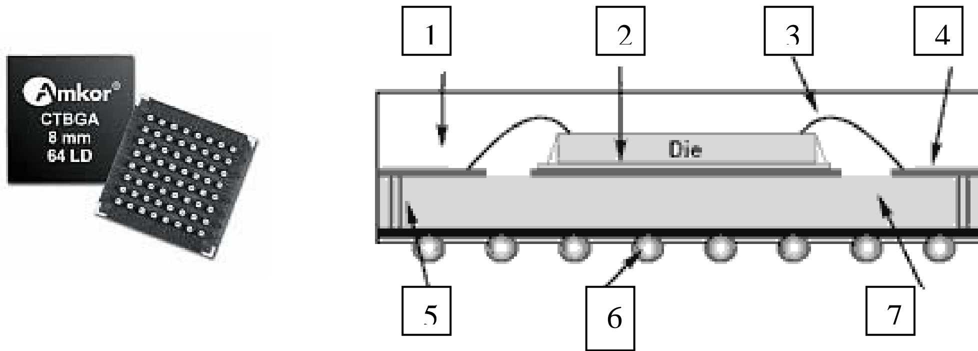
Introduction to Packaging, Semiconductor Packaging, Chip Packages, PWB Design

Max Marks: 30 Time: 1 hour

1. Label the arrowed sections in the figure below which is a cross-section of a CTBGA (ChipArray Thin Core BGA™). (2 marks)



1	
2	
3	
4	
5	
6	
7	

2. An automobile application requires a microcontroller for engine control. List the best option for the different package parameters (substrate, die attach, chip-package interconnection, package-PCB interconnection and encapsulation). Justify your choice, in brief. (2 marks)

Substrate material	
Die attach	
Die-package Interconnection	
Package-PCB interconnection	
Encapsulation	
Name of the Package >> >>>	

3. Write the expansion for the following terms: (any **TEN**)

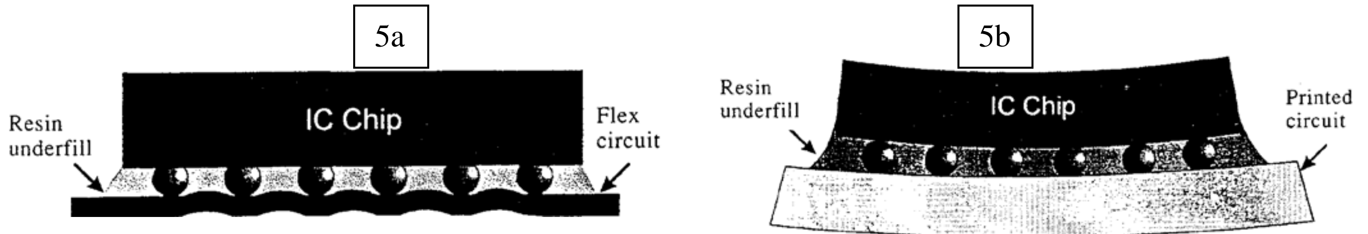
1. SCSP ______________________________
2. LTCC ______________________________
3. OLGA ______________________________
4. PTH ______________________________
5. PSvfBGA ______________________________
6. QFN ______________________________
7. KGD ______________________________
8. PLCCH ______________________________
9. TSV ______________________________
10. COB ______________________________
11. SQFPH ______________________________
12. VTSOP ______________________________
13. CUEBGA ______________________________
14. T^2BGA ______________________________
15. FBGA-PoP ______________________________

(5 marks)

4. IC Packaging efficiency is defined as the *ratio of IC size to package size*. Indicate in increasing order, the packaging efficiency for the following packages: WLP, BGA, DIP, SIP, PGA, QFP, MCM. Give a brief reasoning for your chosen order.

(2 marks)

5. Figure 5a shows a flip chip with underfill on a flexible FR-4 base and the behaviour of the system under thermal load. Figure 5b shows a flip chip with underfill on a rigid FR-4 base and the behavior of the system under similar thermal load. Very briefly discuss both situations and indicate the preferred configuration (*5a or 5b or any other*) for high reliability and enhanced thermal cycling capabilities. (3 marks)



6. Match the following: (any **SIX**) (3 marks)

Column A	Column B	ANSWERS
1. CCGA	a. 183°C	1 =
2. Underfill	b. Surface finish	2 =
3. Eutectic Tin-Lead	c. epoxy polymer	3 =
4. VIP	d. COB	4 =
5. Ni-Au	e. CTE mismatch	5 =
6. Microvia	f. 90:10 / Sn-Pb	6 =
7. Solder Mask	g. 45 deg routing	7 =
8. Glob top	h. BGA	8 =
9. Mitring	i. HDI	9 =

7. Comment on the following: (write in the space provided) (8 marks)
(Draw a pencil sketch where required) *(ANY **FOUR**)*

a. SOC (System on Chip) Vs SIP (System in Package).

b. Aspect Ratio of a Printed Wiring Board.

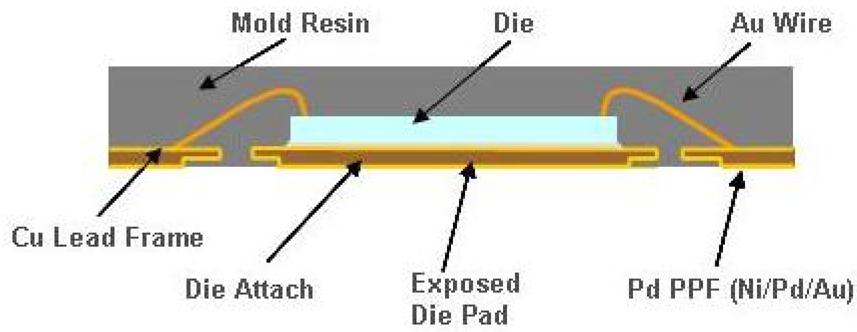
c. Ceramic CGA Vs Ceramic BGA.

d. ILB and OLB in a TAB attachment process.

e. Thermal vias for a PWB with BGAs **(OR)** Anti-pad Design for PWBs.

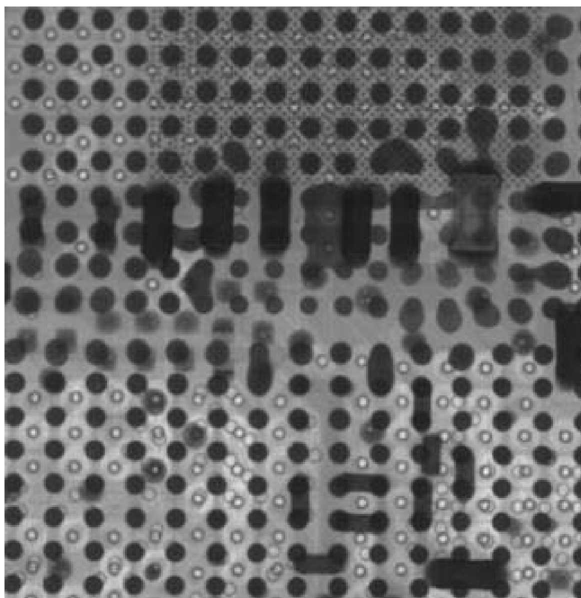
f. Solder reflow process Vs Conductive Adhesive bonding

8. (a) Identify/Name the package illustrated below.



Answer: ___________________________

(b) Identify the defect in the X-ray photograph below of a BGA solder joint.



Answer: ____

(5 marks)