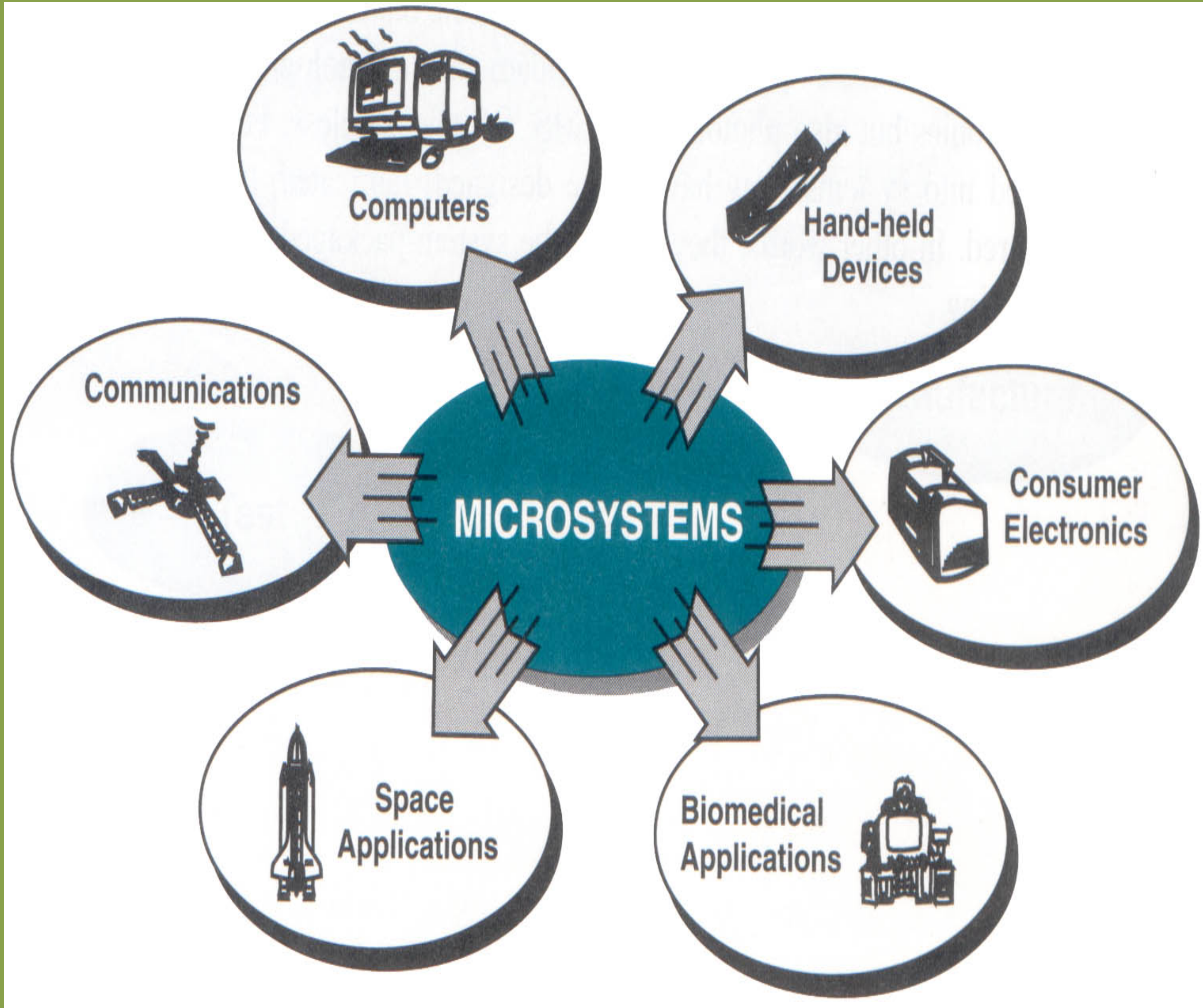
CHAPTER ONE

A general overview of electronics packaging

Content will include:

Electronic systems and needs. Physical integration of circuits, packages, boards and full electronic systems. System applications like computer, automobile, medical and consumer electronics with case studies. Packaging levels.



Computers
Hand-held
Devices
Communications
MICROSYSTEMS
Consumer
Electronics
Space
Applications
Biomedical
Applications

Essentials of every electronic product or system

- Semiconductor devices such as ICs
- Packaging to integrate these ICs and other devices into components
- System-level boards which integrate these components to form the system-level assemblies that provide all functions required of the system.
  - Functions are typically electrical such as analog and digital
  - Components must provide the needed mechanical and chemical functions
  - Systems packaging involves electrical, mechanical and materials technologies

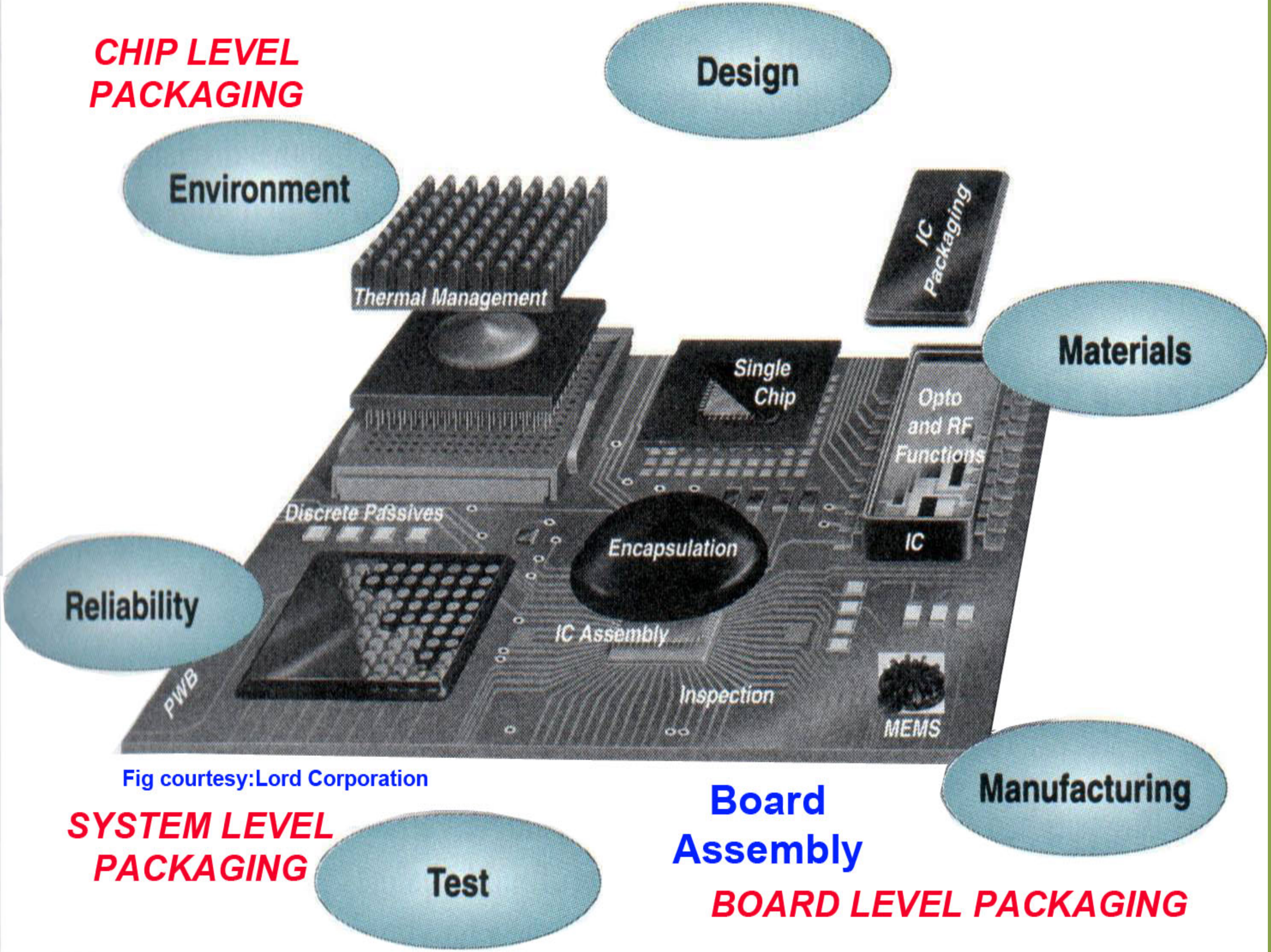


Fig courtesy:Lord Corporation

Why is Microelectronics Systems Packaging important?

- Every IC and Device has to be packaged
- Controls performance of computers
- Controls size of consumer electronics
- Controls reliability of electronics
- Controls cost of electronic products
- Required in nearly every industry such as automotive, communications, computer, consumer, medical, aerospace and military.

Chapter 1 Objectives:

To appreciate the importance and role of packaging (electrical and thermal), material, manufacturing and reliability issues in the design and manufacturing of electronic products.

Learning Objectives:

- ❖ Understand the nature of electronic industry and its evolution
- ❖ Understand the structure of an electronic product

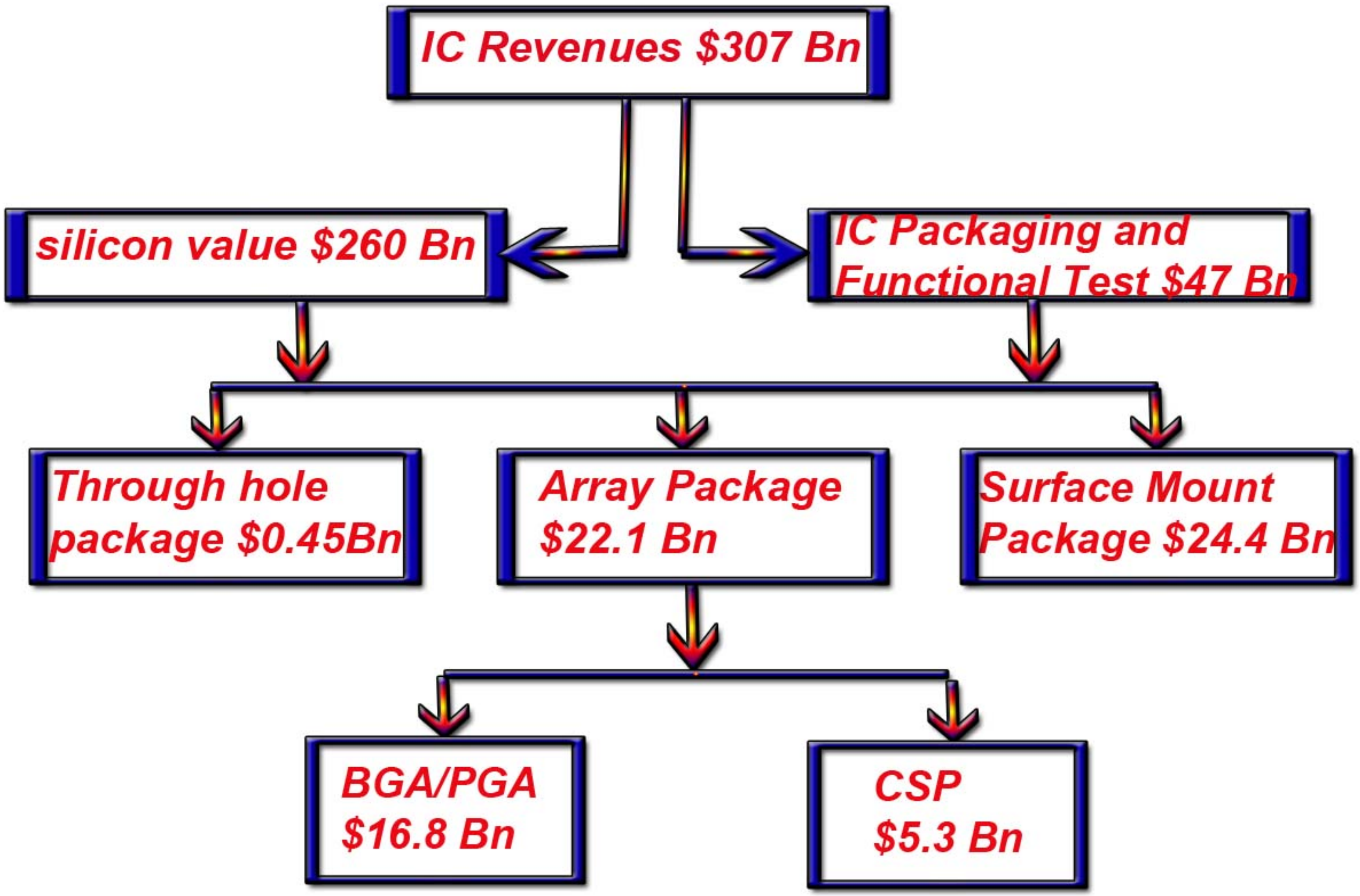
Learning Objectives …

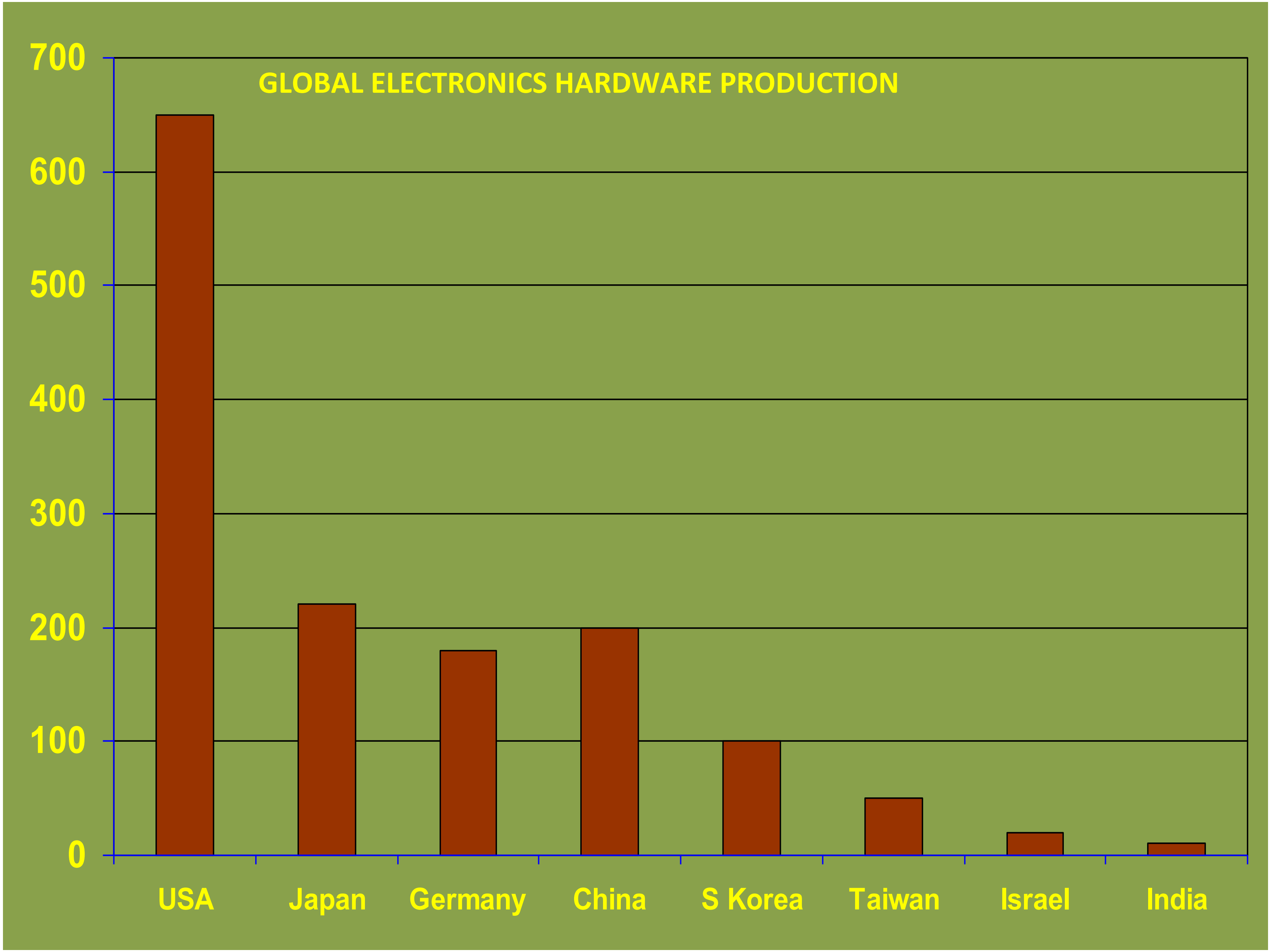
- Appreciate the role and evolution of ICs
- Understand the role of packaging
- Appreciate different issues of packaging
- Identify all the manufacturing technologies
- Appreciate system level issues in different areas of application

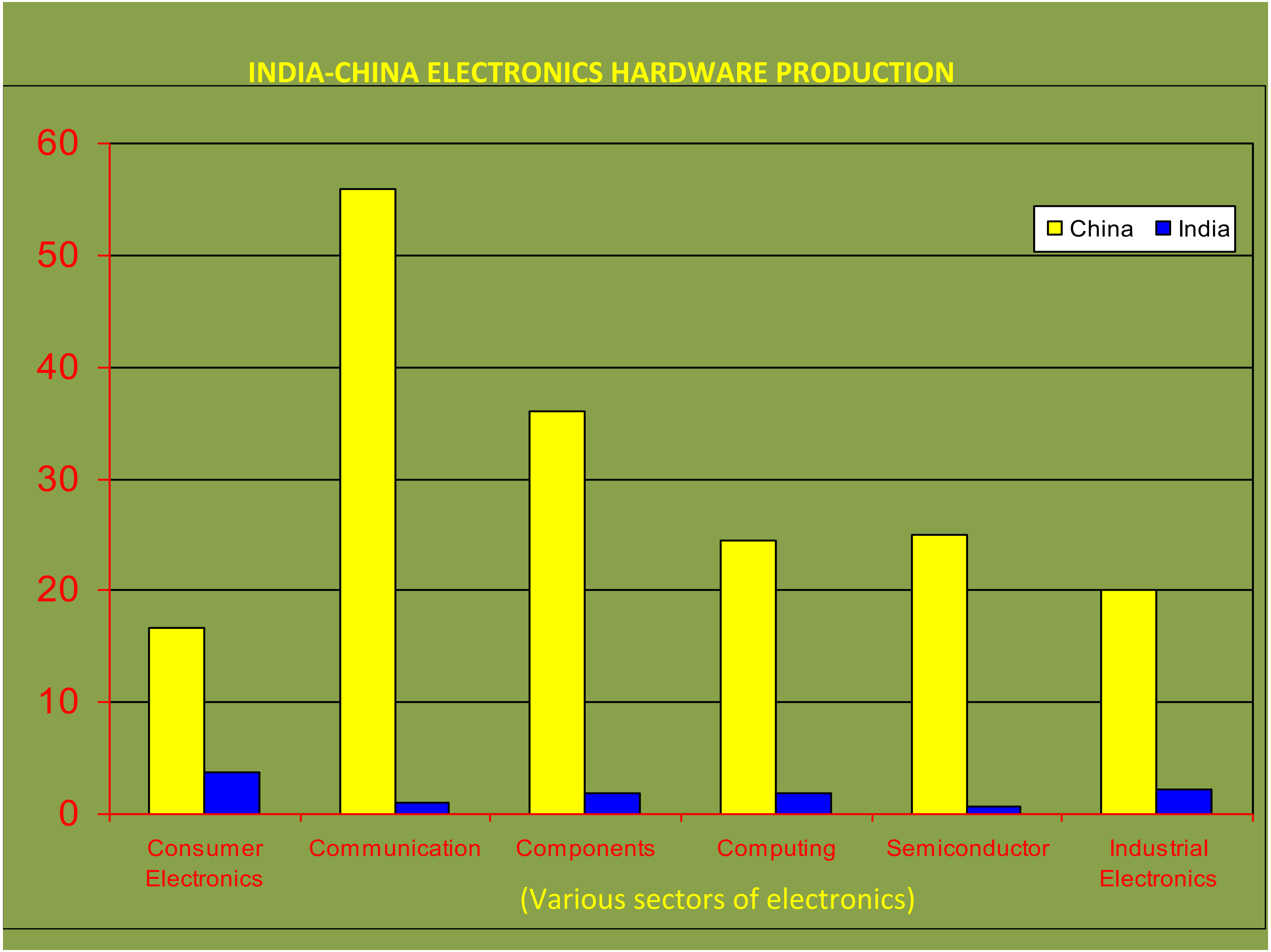
	<u>2009-10</u>
Electronics	> $ 3.0T
Microelectronics & Packaging	> $ 500B
Electronics Packaging	> $ 220B
Indian Electronic Industry (2008-09)	~ $ 20B

To Support the Industry Growth:

- Next-Generation System Technologies
- Skilled Human Resources
  - Globally-Competitive, System-Level Engineers with Complete Product Development Education


IC Revenues $307 Bn
silicon value $260 Bn
IC Packaging and Functional Test $47 Bn
Through hole package $0.45Bn
Array Package $22.1 Bn
Surface Mount Package $24.4 Bn
BGA/PGA $16.8 Bn
CSP $5.3 Bn


GLOBAL ELECTRONICS HARDWARE PRODUCTION
700
600
500
400
300
200
100
0
USA
Japan
Germany
China
S Korea
Taiwan
Israel
India



INDIA-CHINA ELECTRONICS HARDWARE PRODUCTION
60
50
40
30
20
10
0
China
India
Consumer Electronics
Communication
Components
Computing
Semiconductor
Industrial Electronics
(Various sectors of electronics)

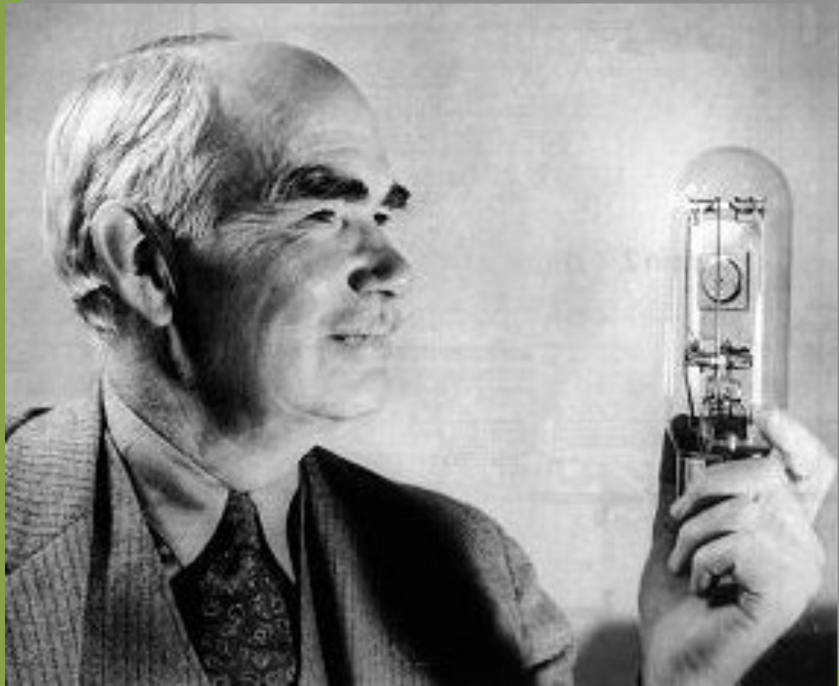
Electronic industry is characterized by

- Technology driving the business
- Rapid technological advances
- Continuous price erosion
- High growth rates
- Large volumes and global markets
- Short life cycles

Technologies of concern

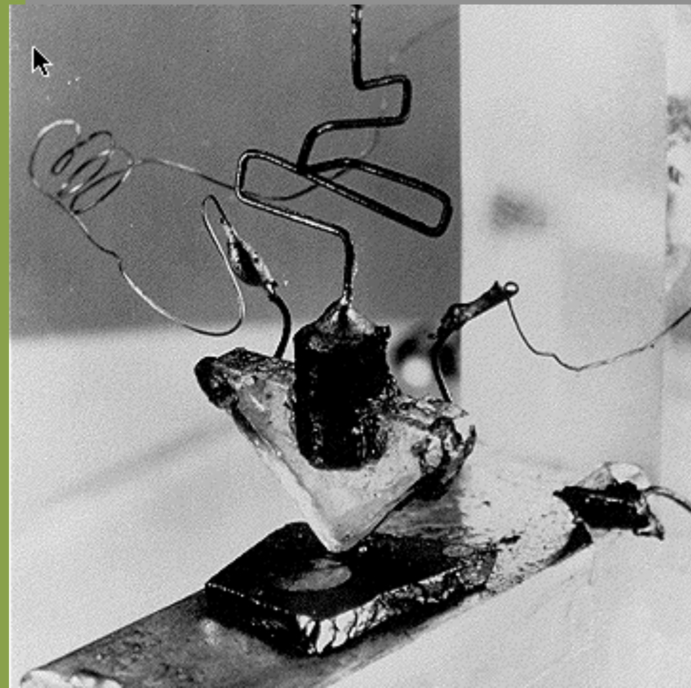
- Silicon
- Packaging
- Magnetic storage
- Display
- Optical ,RF
- Sensor, MEMS and MoEMS
- Material and Nano-materials
- Software- embedded

1906



Audion (Triode), 1906
Lee De Forest

1947

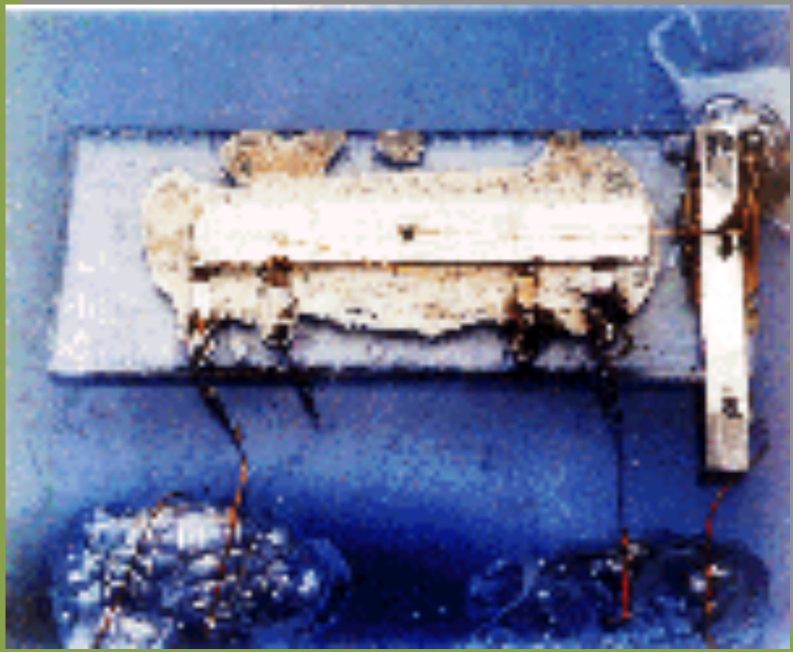


First point contact transistor (germanium), 1947
John Bardeen and Walter Brattain
Bell Laboratories

Figure reproduced from: www.history-computer.com

Figure reproduced from: www.ieee.org

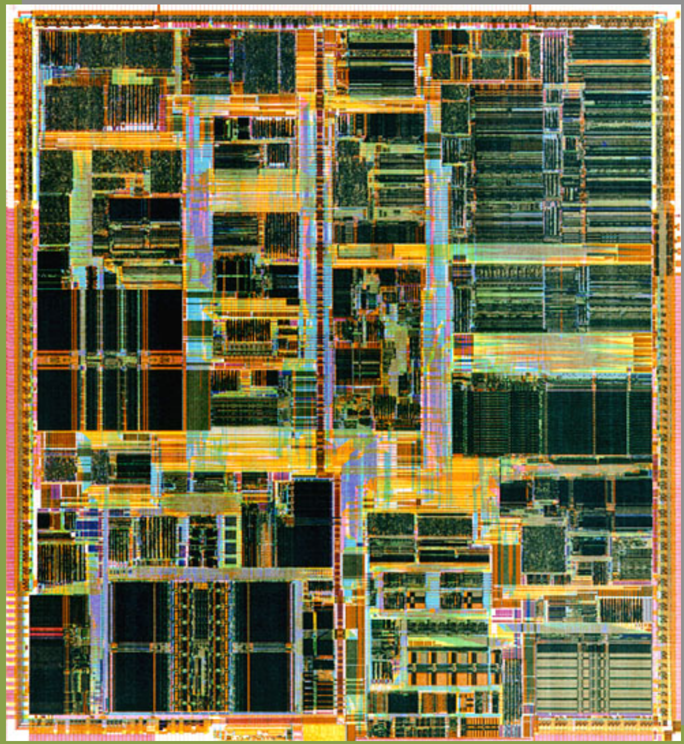
1958



First integrated circuit (germanium), 1958
Jack S. Kilby, Texas Instruments

Contained five components, three types:
Transistors, resistors and capacitors

1997



Intel Pentium II, 1997
Clock: 233MHz
Number of transistors: 7.5 M

Product of Intel

Figure reproduced from: www.texasingenuity.com

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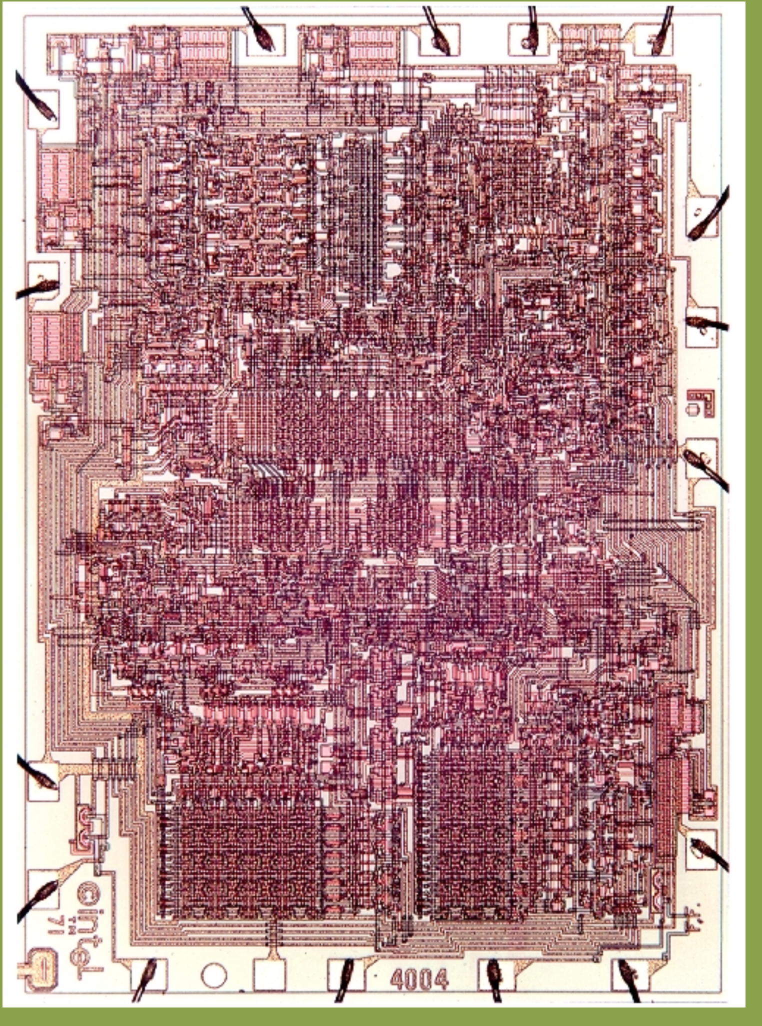
History

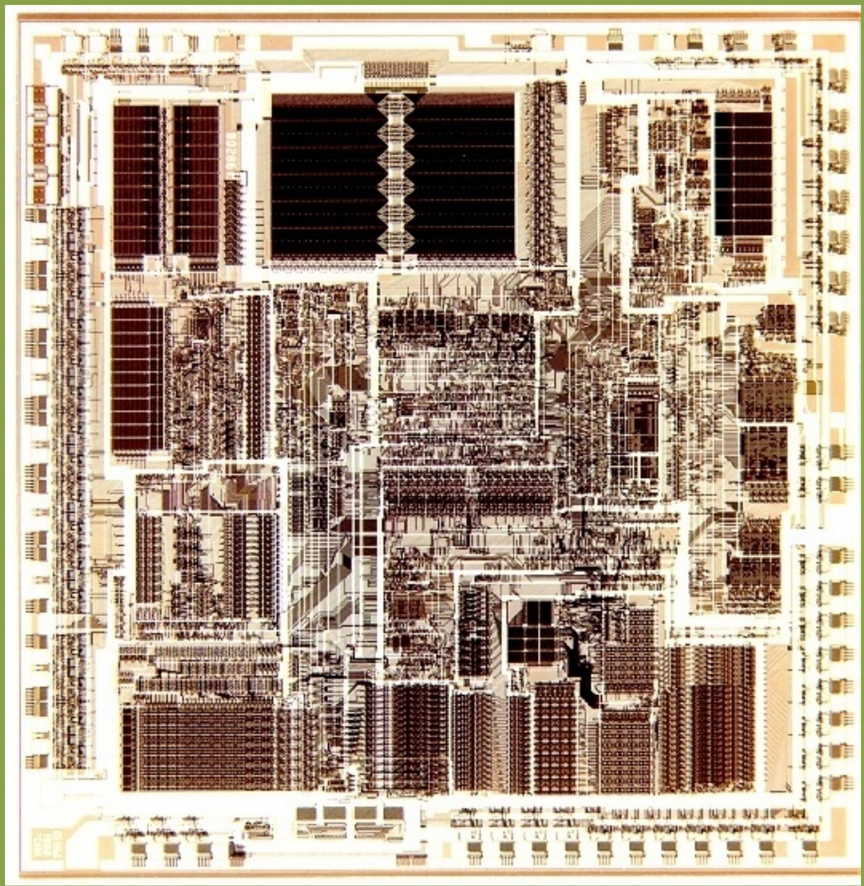


- 1971 Microprocessor invented
  - ❖ Intel produces the first 4-bit microprocessor the 4004
  - ❖ The 4004 was a 3 chip set
    - ➢ 2 kbit ROM IC
    - ➢ 320 bit RAM IC
    - ➢ 4-bit processor
    - ➢ Each housed in a 16- pin DIP package
  - ❖ Processor:
    - ➢ 10 mm silicon gate PMOS process
    - ➢ ~2300 transistors
    - ➢ Clock speed: 0.108 MHz
    - ➢ Die size: 13.5 mm^2

Figure reproduced from: Intel from web and tayloredge.com

Source: Intel

History

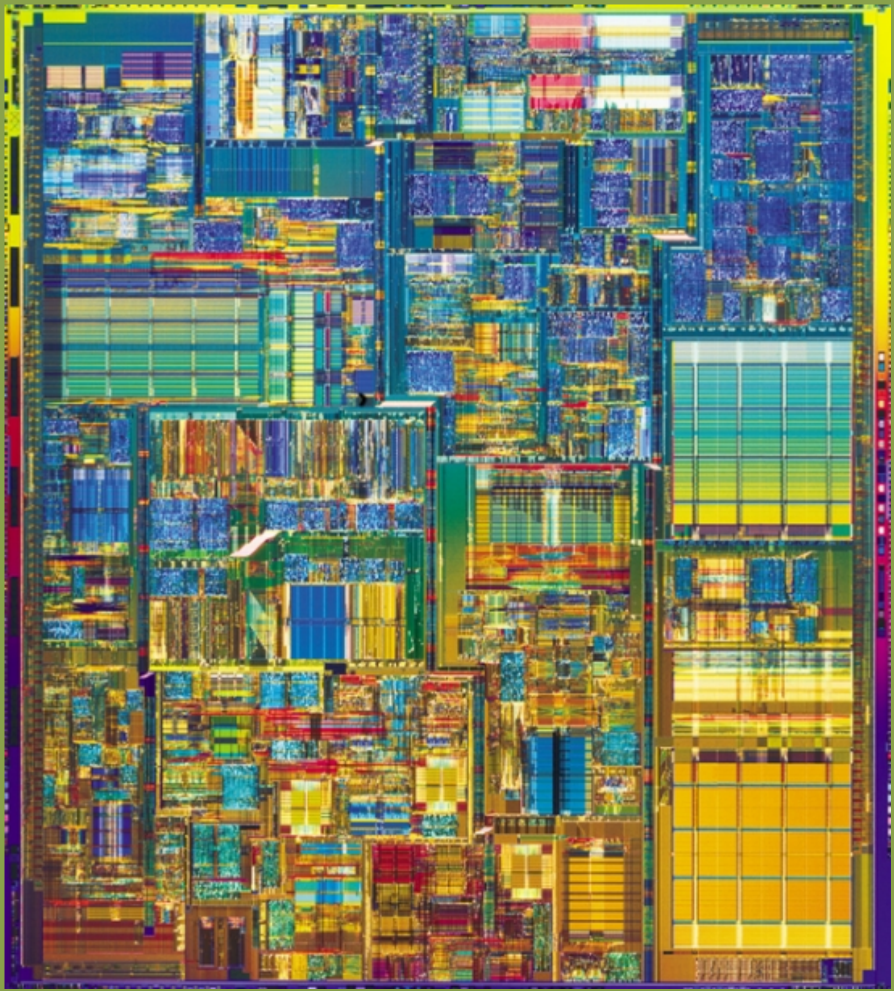


- 1982 Intel 80286
  - ❖ 1.5 mm silicon gate CMOS process
  - ❖ 1 polysilicon layer
  - ❖ 2 metal layers
  - ❖ 134,000 transistors
  - ❖ 6 to 12 MHz clock speed
  - ❖ Die size 68.7 mm^2

Figure reproduced from: Intel from web and tayloredge.com

Product of Intel

History

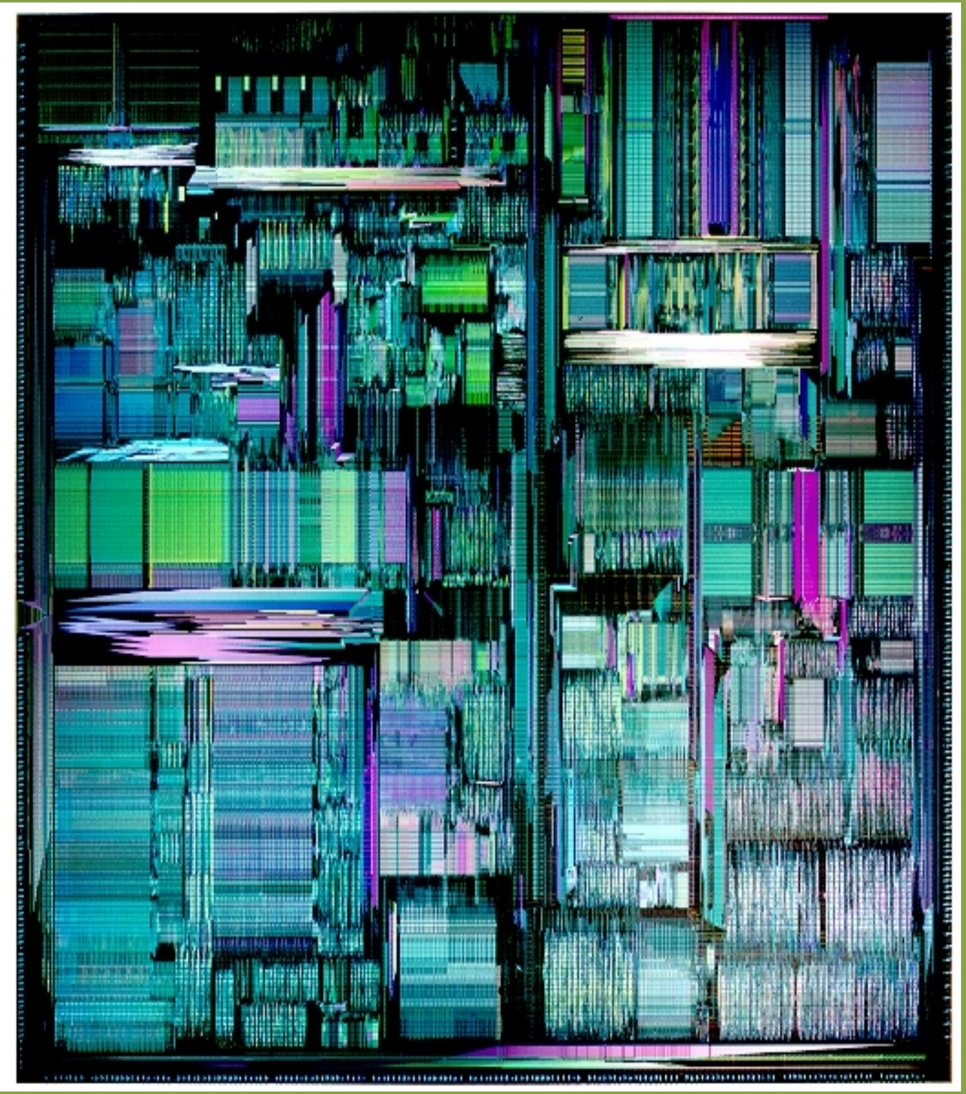


- 2000 Pentium 4
  - 0.18 mm silicon gate CMOS process
  - 1 polysilicon layer
  - 6 metal layers
  - Fabrication: 21 mask layers
  - 42,000,000 transistors
  - 1,400 to 1,500 MHz clock speed
  - Die size 224 mm^2

Figure reproduced from: Intel from web and tayloredge.com

Product of Intel

Current Technology



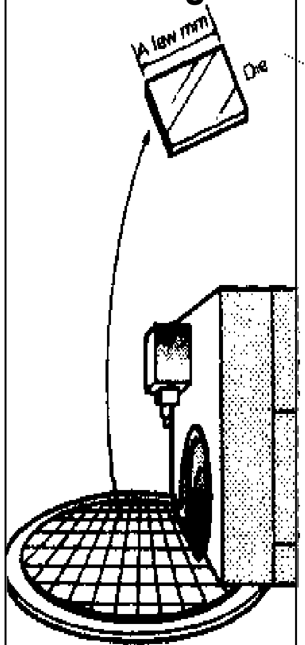
2005 **- Intel Pentium 4TM (65nm)**
Intel introduced a 65nm process in 2005. The single poly-silicon CMOS process has 8 layers of copper metal and requires an estimated 31 mask layers. The 65nm Pentium 4 has 169 million transistors and the die size is 189.9 mm2. Intel soon switched to the new smaller "Core" design.

2007 - **Intel Core 2 Duo (45nm)**
Intel's 45nm debuted in 2007 as the first high-k gate oxide with dual metal gates in production. The 45nm process is a single poly-silicon process with 9 copper layers and requires and estimated 36 mask layers. The 45nm Core 2 Duo die size is 105.78mm2 and packs in 410 million transistors.

Figure reproduced from: Intel from web and tayloredge.com

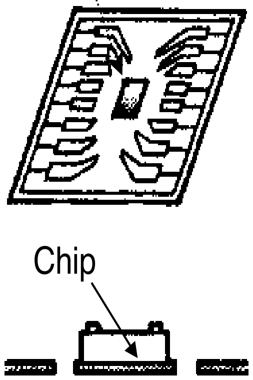
Product of Intel

Dicing



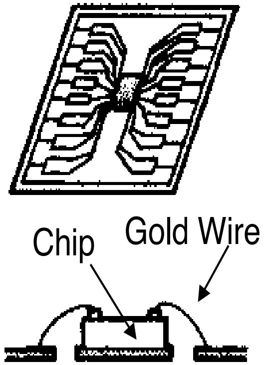
The wafer is separated into chips by a diamond grind-stone. A fully automatic dic-ing saw is used for dicing.

Die Bonding



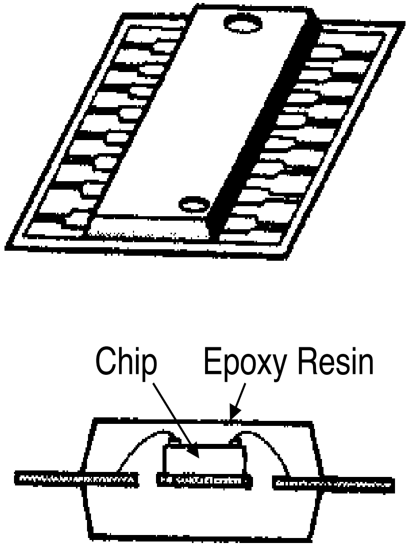
The separated IC chip (die) is bonded into the center of a lead frame or package.

Wire Bonding



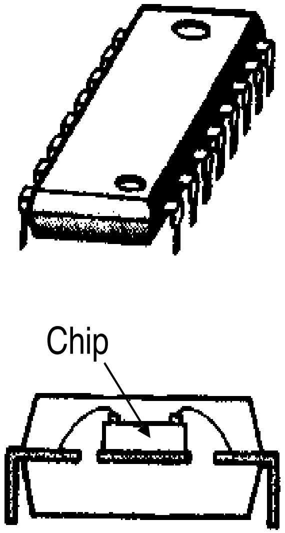
The pads on the IC chip and adjoining terminals on the lead frame are connected, one-by-one, with gold wire.

Molding



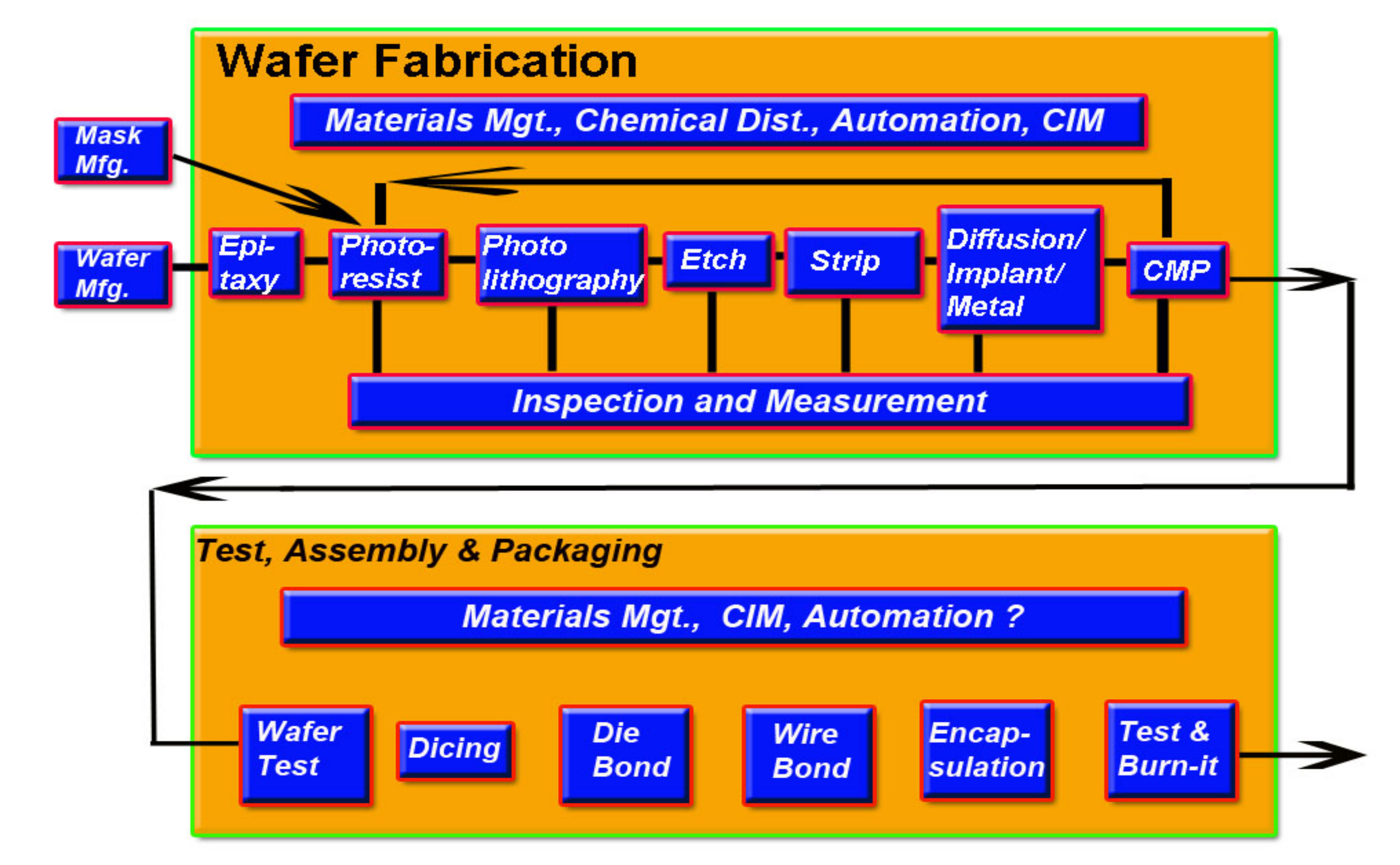
The chip is sealed with a macro-molecule plastic, like epoxy resin, thus finishing the plastic package container.

Forming & Marking



The lead frame is cut, and leads are bent thus forming the package. The manufacturer's name and model number are stamped on top.

The Chip Making Process



"Moore's Law"

- In 1965 Gordon Moore (then at Fairchild Corporation) noted that:
  - ❖ Number of components per chip doubles approx. every 18 months
  - ❖ This statement is commonly know as "Moore's Law"
  - ❖ It has proven to be "correct" till this day
  - ❖ "Integration complexity doubles every three years"

What is behind this fantastic pace of development of the IC technologies?

- ❖ Is it the "technological" will and motivation of the people involved?
- ❖ Or/and is it the economical drive the main force?

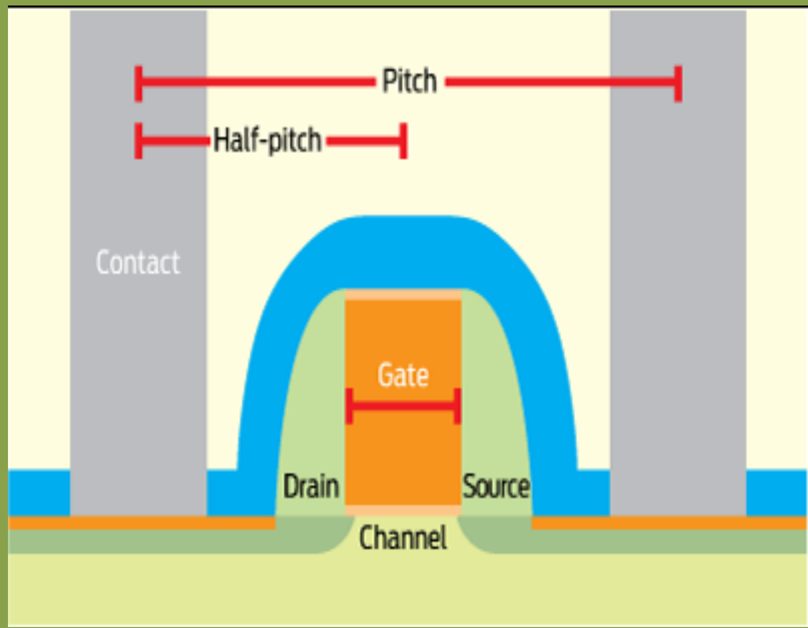
Semiconductor industry sales:

- ❖ 1962, > $1-billion
- ❖ 1978, > $10-billion
- ❖ 1994, > $100-billion
- ❖ 2007, > $2.5-3T

ITRS Roadmap for Semiconductors (2008 summary)

DRAM ½ PITCH Flash Memory (nm)						
2007	2008	2009	2010	2011	2012	2013
68	59	52	45	40	36	32

The common measure of the technology generation of a chip



CHIP SIZE DRAM (mm^2)						
2007	2008	2009	2010	2011	2012	2013
107	81	61	93	74	59	93

DRAM ½ PITCH High performance microprocessor (nm)						
2007	2008	2009	2010	2011	2012	2013
68	59	52	45	40	36	32

Source

ITRS International Technology Roadmap for Semiconductors

ITRS Roadmap for Semiconductors (2008 summary)

Package Pins						
2007	2008	2009	2010	2011	2012	2013
600-2140	600-2400	660-2801	660-2783	720-3061	720-3367	800-3704

Power supply voltage (high performance)						
2007	2008	2009	2010	2011	2012	2013
1.1	1.0	1.0	1.0	0.95	0.90	0.90

Maximum Power (Watts) (high-performance with heat sink)						
2007	2008	2009	2010	2011	2012	2013
102	146	143	146	161	158	149

Source

International Technology Roadmap for Semiconductors

Driving force: Economics

- Traditionally, the cost/function in an IC is reduced by 25% to 30% a year.

    - This allows the electronics market to growth at 15% / year

- To achieve this, the number of functions/IC has to be increased. This demands for:

    - Increase of the transistors count
        - increased functionality
    - Increase of the clock speed
        - more operations per unit time = increased functionality
    - Decrease of the feature size
        - contains the area increase = contains price
        - improves performance

Driving force: Economics

- Increase productivity:
  - Increase equipment throughput
  - Increase manufacturing yields
  - Increase the number of chips on a wafer:
    - reduce the area of the chip:

      - smaller feature size & redesign
  - Use the largest wafer size available (300, 450mm?)

"Is there a limit?"

Much depends on equipment manufacturers

Industry Statistics

- What is the approximate cost of setting up a wafer fab?
- High volume factory:
  - Total capacity: 40K Wafer Starts Per Month (WSPM) (180nm)
  - Total capital cost: $2.7B
    - Production equipment: 80%
    - Facilities: 15%
    - Materials, handling systems: 3%
    - Factory information & control: 2%

Industry Statistics…

- Worldwide semiconductor market (chip market) revenues in 2010: ~$310.3B (up by 35% from 2009)
  - Semiconductor market growth rate ~15% / year
  - Equipment market growth rate: ~19.4% / year
  - By 2011 equipment spending will exceed 30% of the semiconductor market revenues

Year	2002	2005	2008	2011	2014
Low Cost					
Cost (Cents/ pin)	0.34-0.77	0.29-0.66	0.25-0.57	0.22-0.49	0.19-0.42
Power (Watts)	2.0	2.4	2.5	2.6	2.7
I/O count	101-365	109-395	160-580	201-730	254-920
Performance (MHz)	100	100	125	125	150
High Performance			PACKAGING ROADMAP		
Cost (Cents/ pin)	2.66	2.28	1.95	1.68	1.44
Power (Watts)	129	160	170	174	183
I/O count	2248	3158	4437	6234	8758
Performance (MHz)	800	1000	1250	1500	1800

Year	2009	2010	2011	2012	2013	2014
Single-chip Package Technology Requirements						
Chip size mm2						
*Low-cost/hand held	100	100	100	100	100	100
*Cost-performance	140	140	140	140	140	140
*High-performance FPGA	729	766	804	750	750	750
*Harsh	100	100	100	100	100	100
Maximum Power (W/mm2)						
*Hand held and Memory	3	3	3	3	3	3
*Cost-performance	0.9	0.96	1.13	1.11	1.1	1.17
*High-performance	0.46	0.47	0.52	0.51	0.48	0.49
*Harsh	0.2	0.22	0.22	0.24	0.25	0.25
Core Voltage (V)						
*Low-cost/hand held	0.7	0.6	0.6	0.6	0.5	0.5
*Hand held and Memory	0.6	0.5	0.5	0.5	0.5	0.4
*Cost-performance	0.8	0.6	0.6	0.6	0.5	0.5
*High-performace	0.8	0.6	0.6	0.6	0.6	0.5
*Harsh	1.2	1.2	1	1	0.9	0.9
Package Pin Count Maximum						
*Low-cost/hand held	160-850	170-900	180-950	188-1000	198-1050	207-1100
*Cost-performance	660-2801	660-2783	720-3061	720-3367	800-3704	800-4075
*High-performance FPGA	4620	4851	5094	5348	5616	5896
*Harsh	425	447	469	492	517	543
Minimum Overall Package Profile (mm)						
*Low-cost, hand-held and memory	0.3	0.3	0.3	0.3	0.3	0.2
*Cost-performance	0.65	0.65	0.65	0.5	0.5	0.5
*High-performance	1.4	1.2	1.2	1	1	1
*Harsh	0.8	0.8	0.7	0.7	0.7	0.7

Data from ITRS International Technology Roadmap for Semiconductors

Challenges in Packaging for the industry- Roadmap topics

- Process Integration
  - Both front end and back end processes
- Device scaling
- Electrical issues- signal integrity; RF and analog/mixed
- Photolithography- bigger challenge to Moore's law
- Masks and light source for patterning
- New materials- high conductivity and low dielectric permittivity

Challenges in Packaging for the industry-Roadmap topics…

- Manufacturability of the interconnect structures
- Power management for different applications
- Testing complexity
- Equipment challenges (very important!!)
- Manufacturing cost and cycle time
- Performance requirement of the market
- Assembly and packaging
- Resource conservation; environmental concerns

Challenges in Packaging for the industry-Roadmap topics…

- ❖ Yield enhancement for industry; large volume production
- ❖ Thermo-mechanical; Design for Reliability

Challenges are more when the industry progresses towards 22nm technology DRAM pitch. Today production is available for 65nm; designs being tested for 45nm by very few companies. It is expected to be 22nm by 2015 (short term goal) and 11nm by 2022 (long term goal).