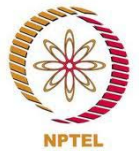




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Final Examination



Max: 50 Marks

Syllabus: ALL modules

Time: 3 hours

SECTION A

(15 marks)

(Questions 1-3)

1. **Relate the items in the two columns below appropriately.** (3 marks)
(Any **SIX**)

<i>Column 1</i>	<i>Column 2</i>	<u>ANSWERS</u>	
A. ENIG	1. Flux type	A	
B. SAC Alloy	2. Etch resist	B	
C. WLP	3. Embedded R	C	
D. RMA	4. Wave soldering	D	
E. Electroless Ni-P	5. CSP	E	
F. CMP	6. Pb-free soldering	F	
G. Dross	7. Wafer thinning	G	

2. *Briefly* discuss the following. **Give an example/sketch where necessary.** (any **FOUR**)
(6 marks)
- a. Tin Whiskers

- b. Meniscus Coating of a liquid dielectric



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c. ‘Popcorning’ in a BGA package

d. Type II-A SMD Assembly process (*brief flow chart/list of steps*)

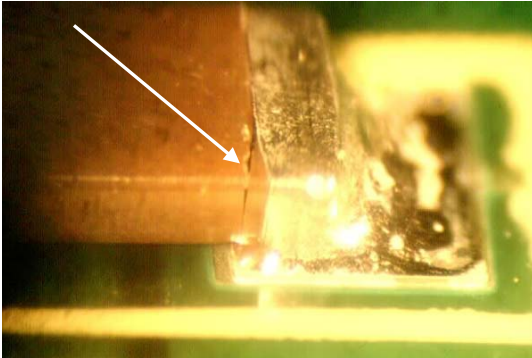
e. ‘Bend Radii’ of flex PCBs

Max: 50 Marks

Syllabus: ALL modules

Time: 3 hours

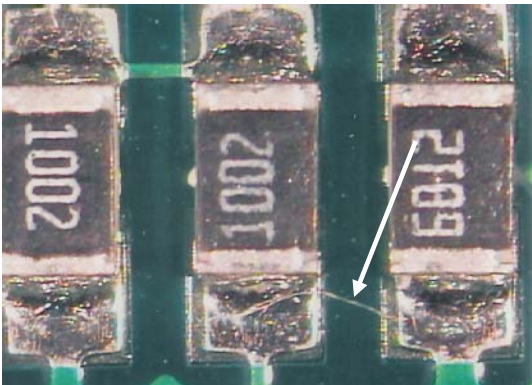
3. Identify the defect(s), give reason(s) for defects and suggest possible remedy in the following cases. These defects shown here are related to board assembly (during or after reflow or wave soldering) only. (6 marks)



A.
Name the defect

Reason for defect to have occurred

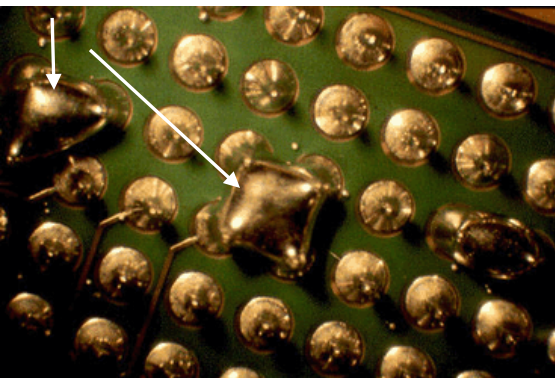
Remedial measure



B.
Name the defect

Reason for defect to have occurred

Remedial measure



C.
Name the defect

Reason for defect to have occurred

Remedial measure



D.
Name the defect

Reason for defect to have occurred

Remedial measure

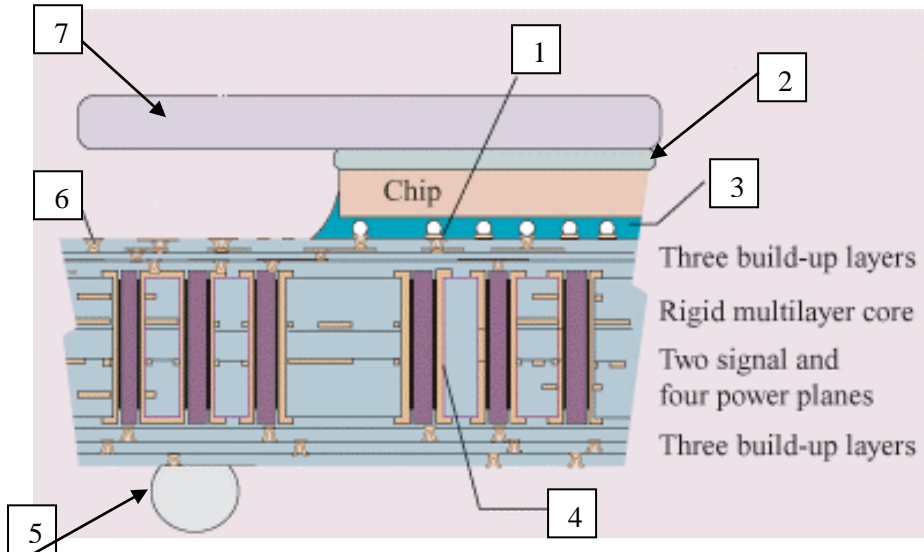
SECTION B

(15 marks)

(Answer ALL)

(Questions 4-8)

4. **Identify the arrowed items in the figure below:** (3.5 marks)



- | | |
|----|----|
| 1. | 2. |
| 3. | 4. |
| 5. | 6. |
| 7. | |

5. For the following applications, which mode of heat transfer will dominate? (2 marks)

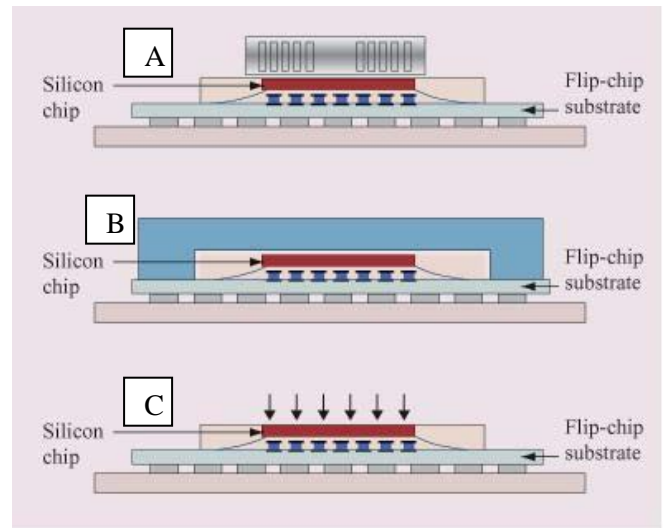
- Space electronics >>
- Desktop computer >>
- Cell phone >>
- Electric Iron >>

Max: 50 Marks

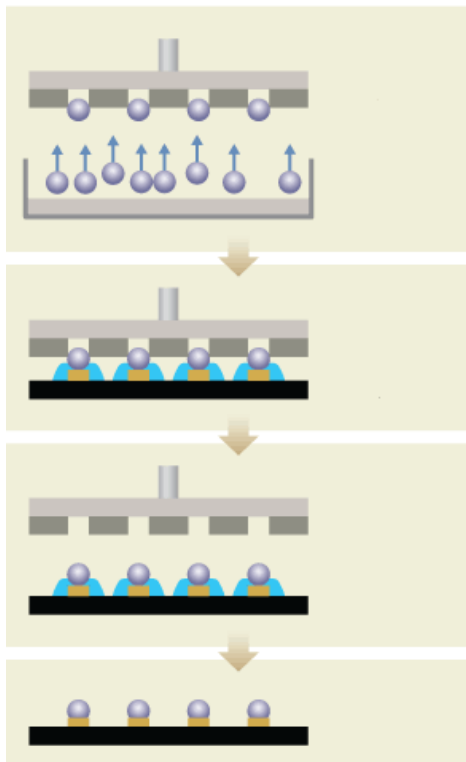
Syllabus: ALL modules

Time: 3 hours

6. Shown in this figure, are three advanced concepts of cooling for organic packages. Identify each of them and suggest which could be more effective. (3 marks)



7. Look at the process flow picture below and identify/name what process is being carried out. (2 marks)



a.

b.

c.

d.

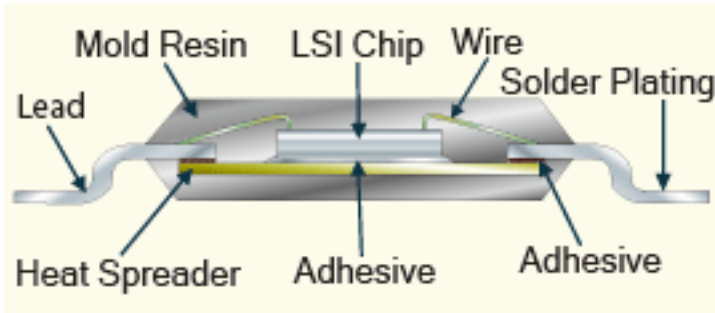
Max: 50 Marks

Syllabus: ALL modules

Time: 3 hours

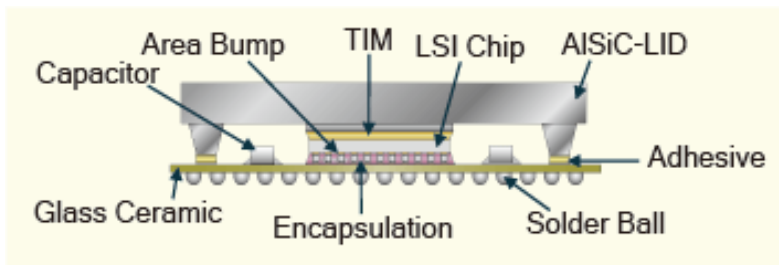
8. Identify the packages below with its complete name. (4.5 marks)

A.



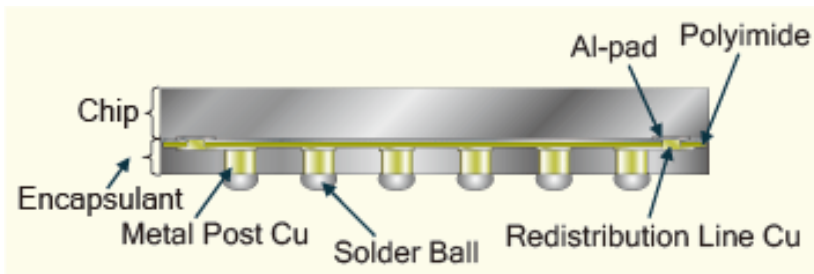
Package size 4.4mm X 6.5mm
Mounting Height 1.20mm max
24 pin with pin pitch 0.5mm

B.

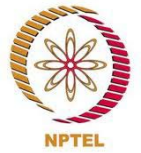


Pin count: 625
Package size (mm): 27 x 27
Pin arrangement: Full Matrix
Ball matrix: 25 x 25
Pin pitch (mm): 1.0

C.



Package size: 6mm x 6mm
Package height: 0.8mm max
Chip thickness 500um typical
Encapsulant thickness 70um
Ball pitch 0.4mm
Ball height 130um typical



Max: 50 Marks

Syllabus: ALL modules

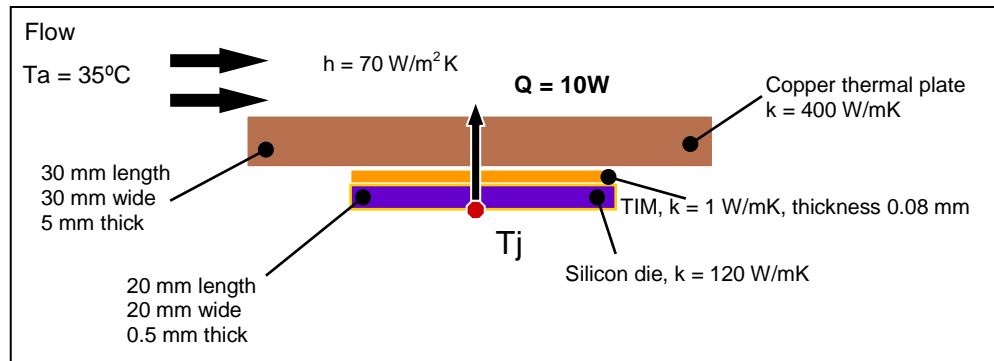
Time: 3 hours

SECTION C: (20 marks) (Answer Any FIVE) (Questions 9-15)

9. In the following chip configuration, a silicon die is attached to a thermal plate with an interface material (TIM). The die is dissipating power and the heat is lost from the thermal plate surface.

Answer the following questions:

- 1) **Make a thermal resistance circuit for the different elements of the chip. Do not forget to include the thermal resistance of the air.**
- 2) **Calculate the individual resistances for the circuit.**
- 3) **What is the die temperature (T_j) at the bottom of the Silicon die?** (4 marks)





Max: 50 Marks

Syllabus: ALL modules

Time: 3 hours

10. An assembly of fine-pitch flip-chip devices using **BOTH** Isotropic Conductive Adhesive (ICA) and Non-Conductive Adhesive (NCA) needs to be carried out for a prototype product. NCA here refers to the underfill material. **The substrate has to undergo curing cycle only once.** Assume all components in this case are flip chip on rigid FR-4. (4 marks)

Questions:

- 1. Write the optimal process flow.**
- 2. Specify typical process temperatures, materials and related equipments to be used.**

Max: 50 Marks

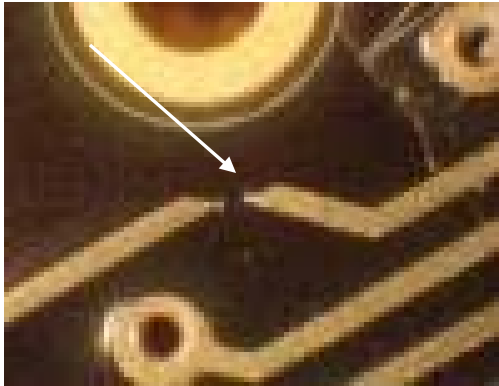
Syllabus: ALL modules

Time: 3 hours

11. Relate the following illustrations of defects with respect to **PCB manufacturing processes** only. All you need to do is identify which manufacturing step has been overlooked (poor quality control) resulting in the unacceptable standards and failures as shown.

Answer the Questions against each slide.

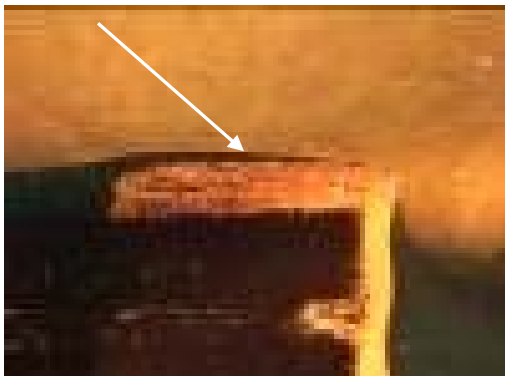
(4 marks)



Type of Defect:

Reason:

Solution:



Type of Defect:

Reason:

Solution:



Type of Defect:

Reason:

Solution:



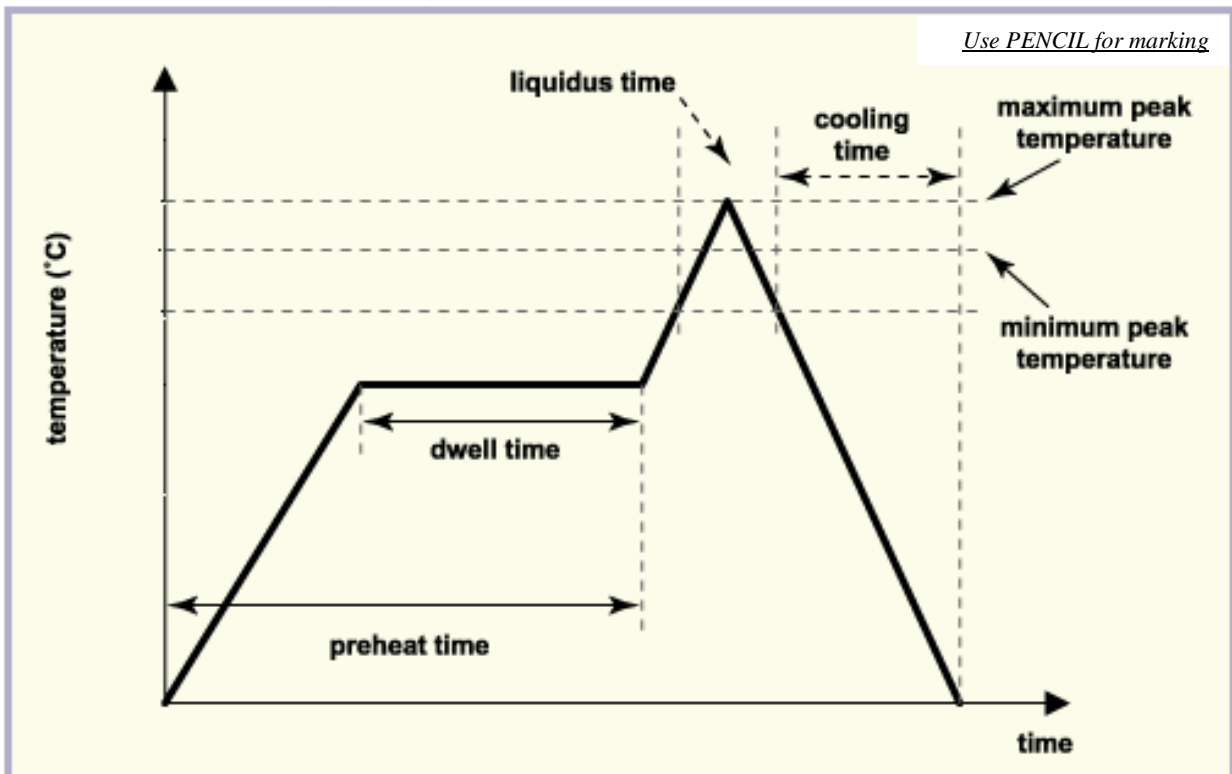
Max: 50 Marks

Syllabus: ALL modules

Time: 3 hours

12. A PCB assembly has to utilize reflow soldering (IR). The following details are available for the process
- a. This process is *NOT* done in N_2 atmosphere. Temperature in reflow zone can be $\pm 1^\circ C$
 - b. High Tg FR-4 substrate used with a Tg of $190^\circ C$ & PCB has Ni-Au finish.
 - c. Solder paste (with RMA flux) is SAC 305 alloy (3% Ag and 0.5% Cu)- MP of $217^\circ C$
 - d. Component type is SMD; 4 high pin-count PBGAs used; others are SOIC, passives etc.
 - e. The most vulnerable component can withstand $225^\circ C$ for 30 seconds.
 - f. It is recommended to have one-step reflow only. BGAs are large area ($43 \times 43 mm$).
 - g. The temperature profile to be used is given below. (4 marks)

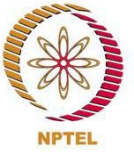
Questions: 1) Suggest start and end temperatures from RT to peak reflow. 2) Mention heating rates in each zone including cooling zone. 3) Indicate board dwell times in ALL zones.



Use the graph above for entering your values. Give VALID reasons for your profile markings in the space provided below.



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Max: 50 Marks

Syllabus: ALL modules

Time: 3 hours

13. From the following instructions, design the construction of a 6-layer PTH multi-layer PWB. Assume very minimal material loss or reduction in prepreg thickness during multilayer press operation. The 6-layer **finished total board thickness should be 1.6mm**. Prepreg type 2116MR to be used. Each 2116 prepreg sheet is 0.12mm thick. The MLB stack sequence should be as follows:

L1: Outer layer electroless Copper plating followed by electroplating build-up

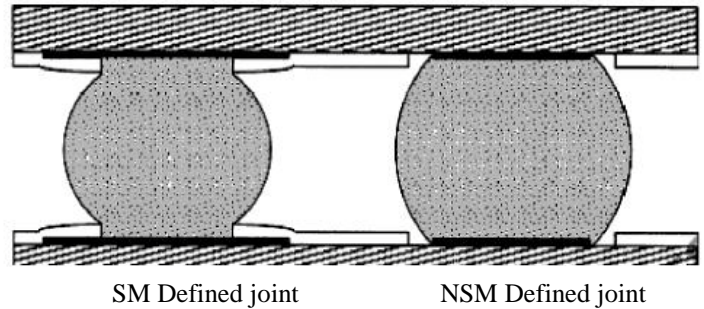
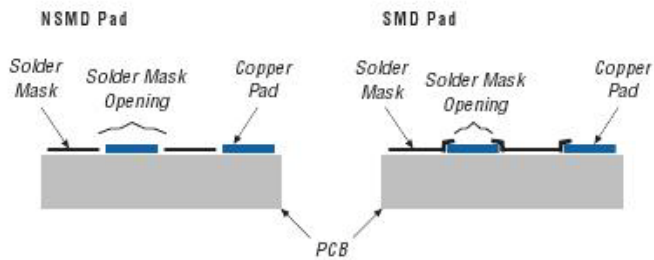
Layer 2 & 5: Copper foil to be used Layer 3/4: Copper/ dielectric rigid FR-4 CORE to be used

L6: Outer layer electroless Copper plating followed by electroplating build-up

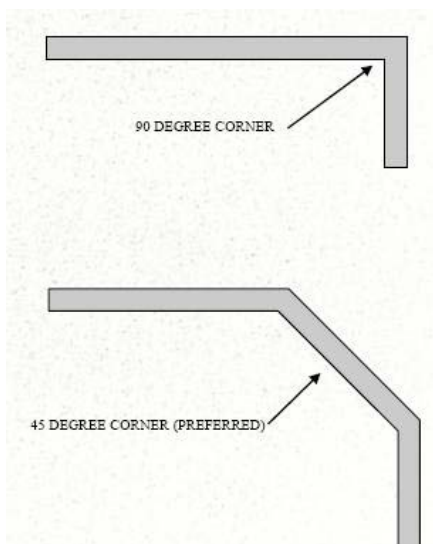
Questions:

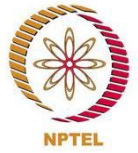
1. Draw a cross-section of the total structure (6-layers). Label all layer constituents thoroughly.
 2. Indicate thicknesses for the following: Core FR4 constituents; Cu foils; Prepreg sheets; electroless and electro copper (4 marks)
-

14. (a) The figure (L) given below illustrates a ‘solder mask defined pad’ and a ‘non solder mask defined pad’ used for BGA design. Alongside (R) is presented a figure of a completed solder joint. Give two reasons why NSMD pads are the most preferred design for BGA/uBGA assembly. (2 marks)

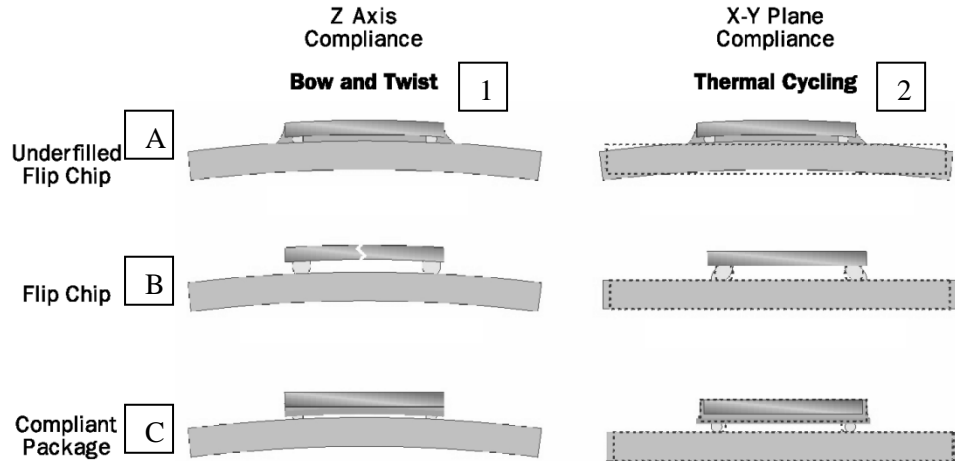


- (b) During PCB routing a 45 degree corner is most preferred. Enunciate two valid reasons for this choice. (2 marks)





15.



Study the figure(s) above carefully. (Figures can be labeled as A1, B1, C1, A2, B2, C2)

Answer the **Questions** below:

1) Describe in brief, the Z-axis and X-Y plane compliance scenarios presented here.

2) Give a definitive statement with reasoning as to which system(s) (among A, B and C) will protect the die effectively and which system(s) (among A, B and C) will give extended solder joint life. (4 marks)

16. Figure A is an example of a sequential build-up technology with microvias applied to a standard multilayer board. Here only a couple of top and bottom layers of a rigid core are SBU. Figure B is an example of a SBU process (like ALIVH) which suggest elimination of rigid cores. **Discuss the merits and demerits of these two methods of manufacture of HDIs from long-term reliability standpoint.**

