Course CONCLUSION & SUMMARY: chapter-wise

NPTEL VIDEO COURSE ON "ELECTRONIC SYSTEMS PACKAGING"

QUICK REVIEW OF TOPICS IN THIS VIDEO COURSE

WHAT IS ELECTRONICS SYSTEMS PACKAGING?

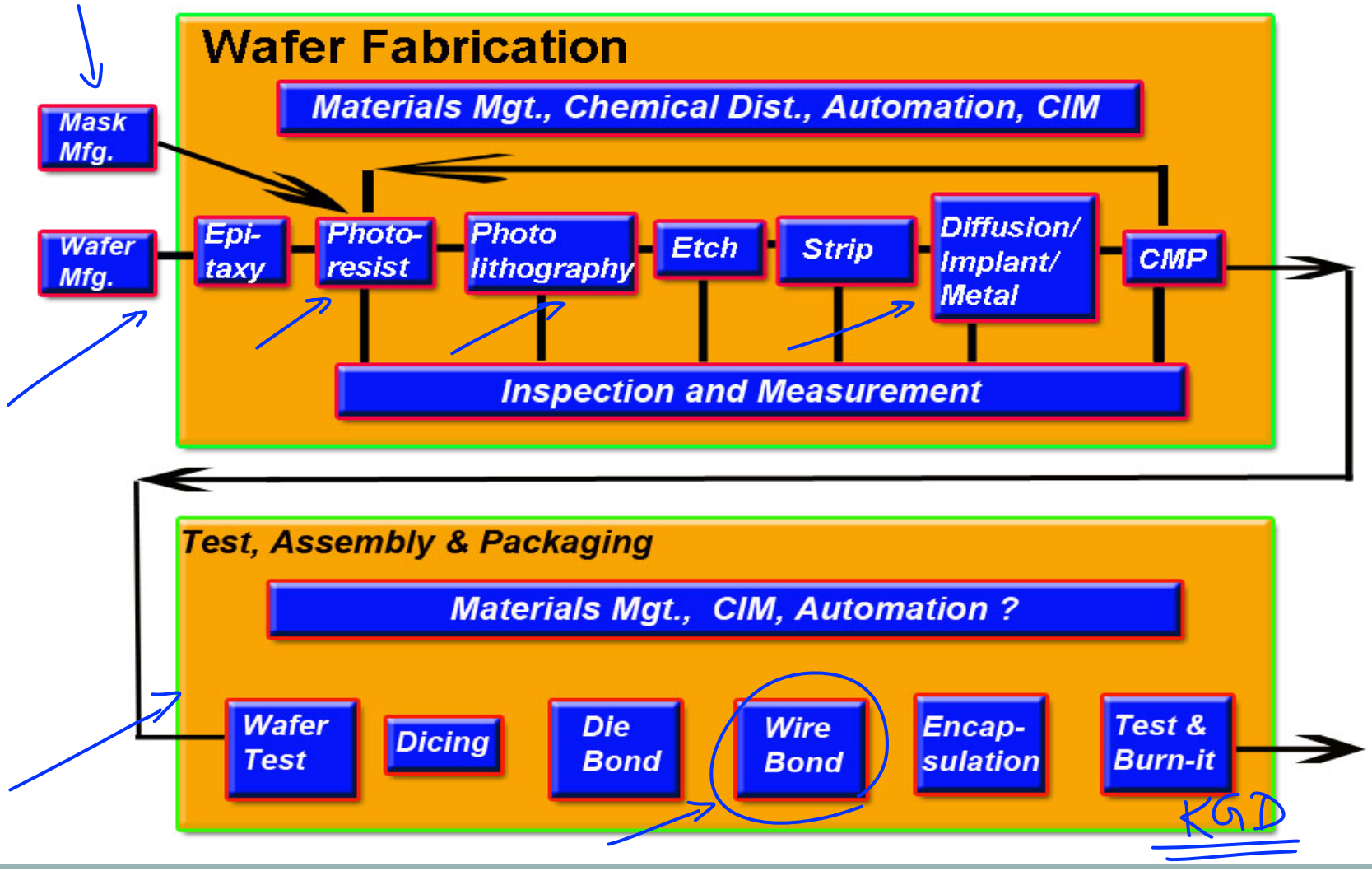
- Packaging is ‘every technology’ required between the IC and the system.
- Packaging is just not a study of ‘interconnections’. It is a lot more than that.
- Without a proper packaging methodology a manufactured die/IC is no good.
- Packaging is basically done at three levels- chip level, board level and system level.

Fig courtesy: Georgia Tech

Why is Microelectronics Systems Packaging important?

- Every IC and Device has to be packaged
- Controls performance of computers
- Controls size of consumer electronics
- Controls reliability of electronics
- Controls cost of electronic products
- Required in nearly every industry such as automotive, communications, computer, consumer, medical, aerospace and military.

The Chip Making Process



Industrial and Medical systems

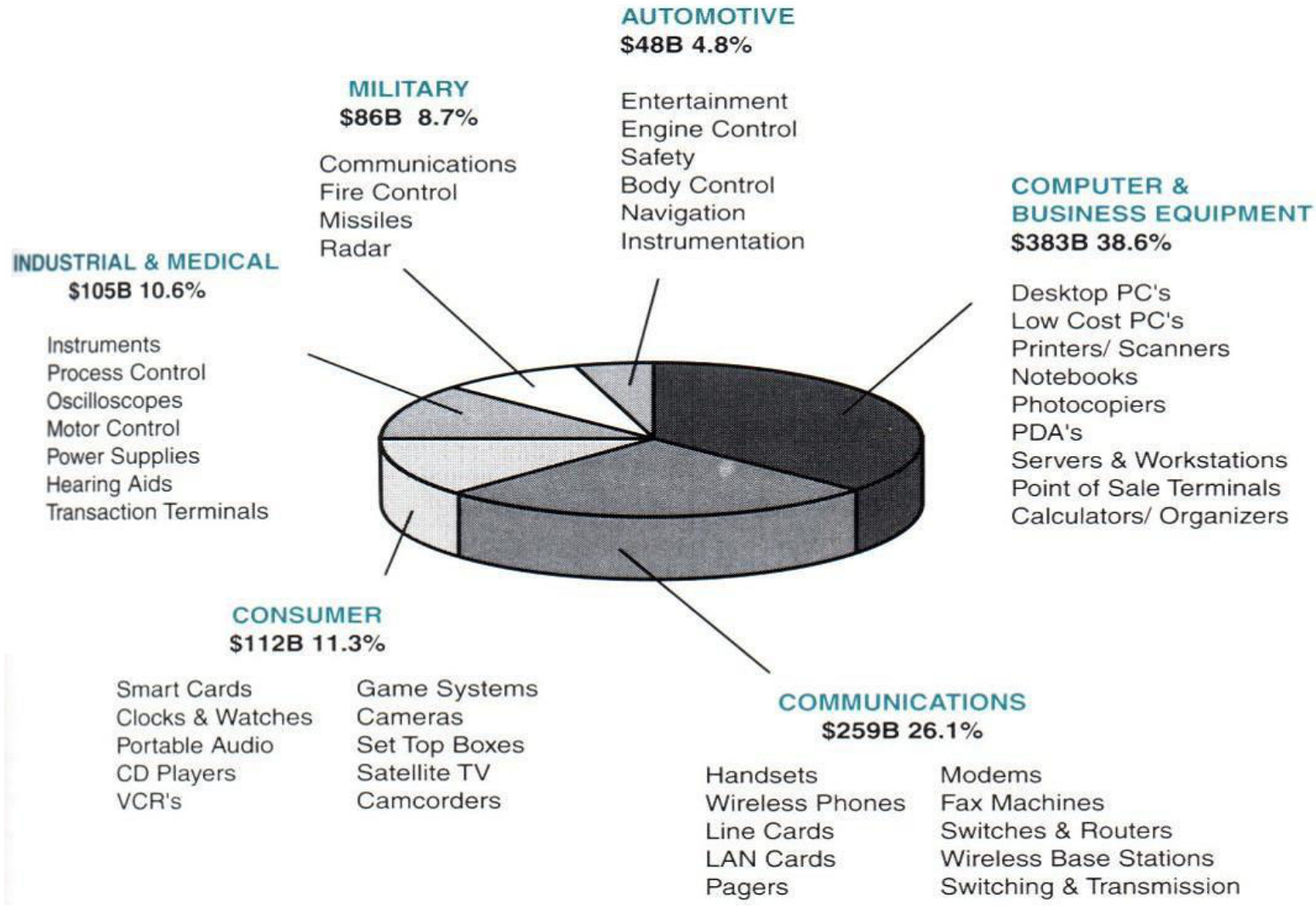


Figure from "Fundamentals of Microelectronics Sys Packaging" Rao Tummala

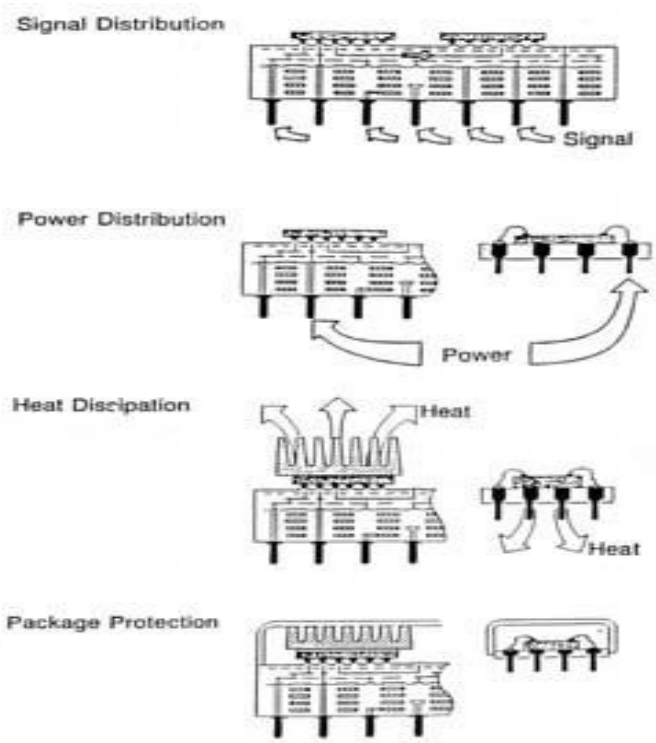
What is Electronics Packaging?

"Science and art of providing a suitable environment to the electronic product as a whole to perform reliably over a period of time"

Major functions of Electronics Packaging

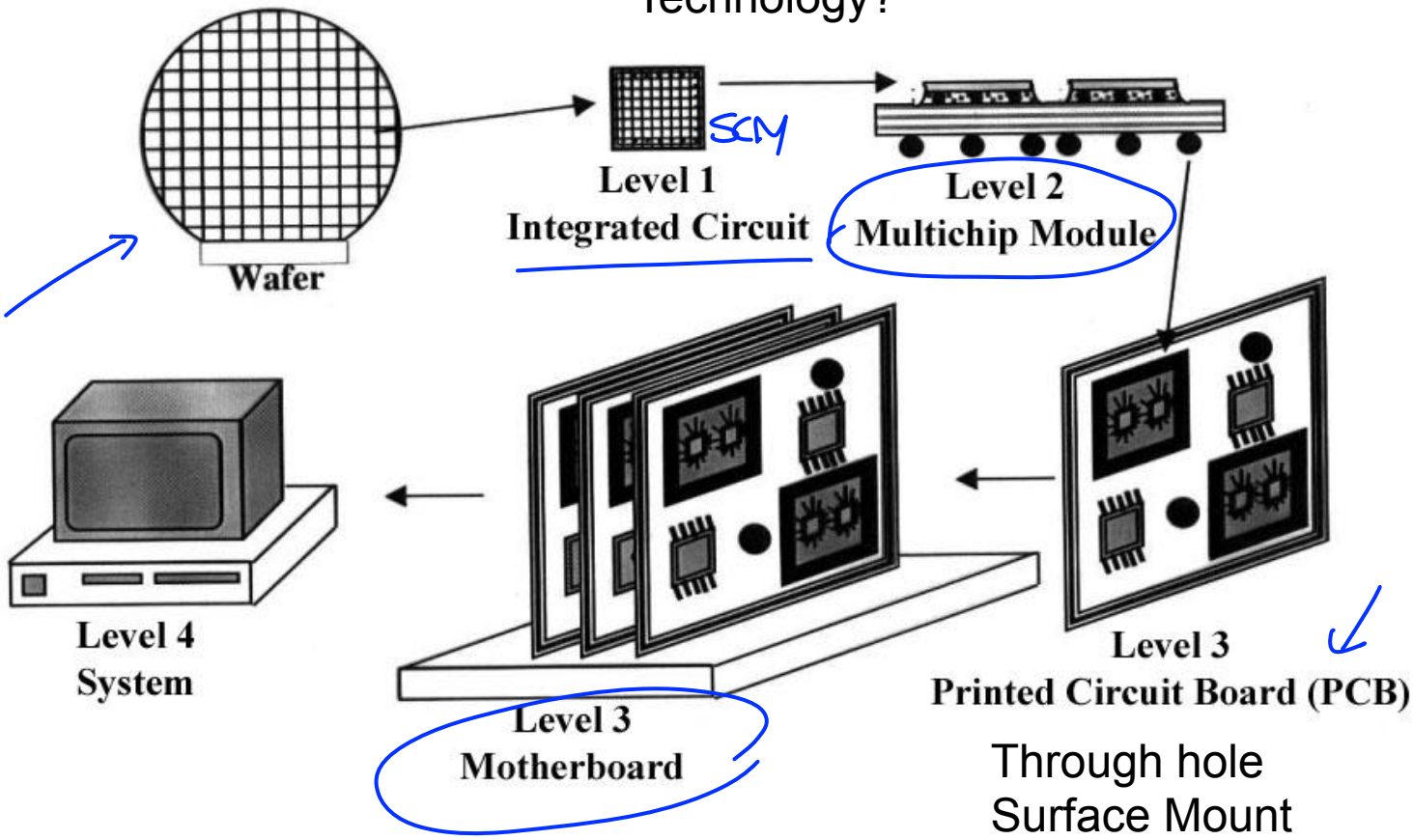
- Signal distribution
- Power distribution
- Heat dissipation (cooling)
- Protection (mechanical, chemical, electromagnetic)

The package must function at its specified performance level

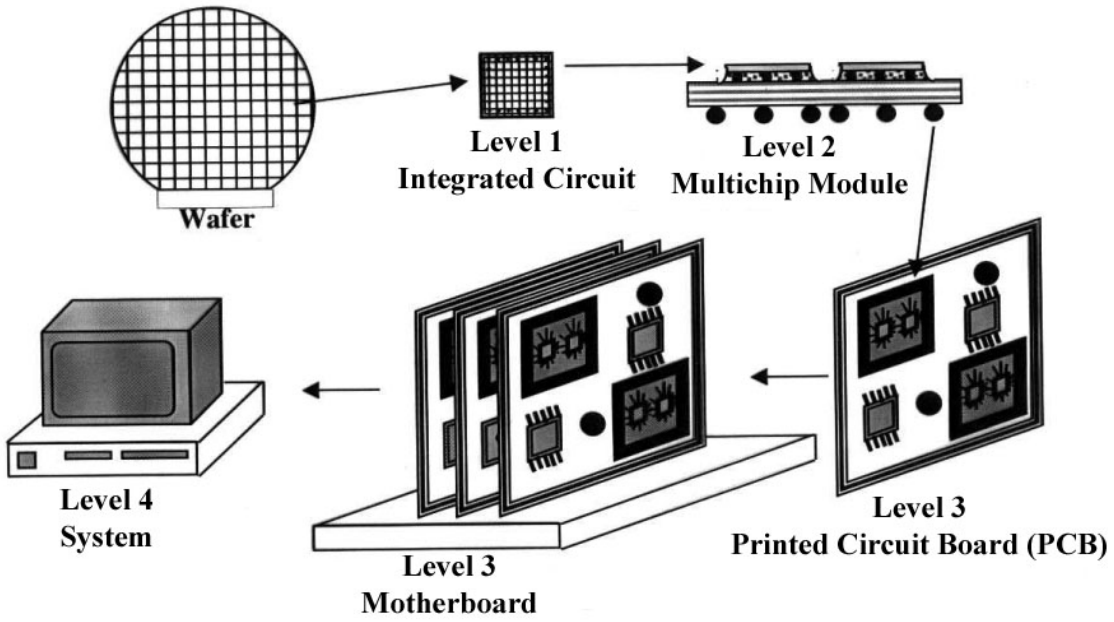


Wafer size?
Wafer fab cost?

Die size?
Technology?



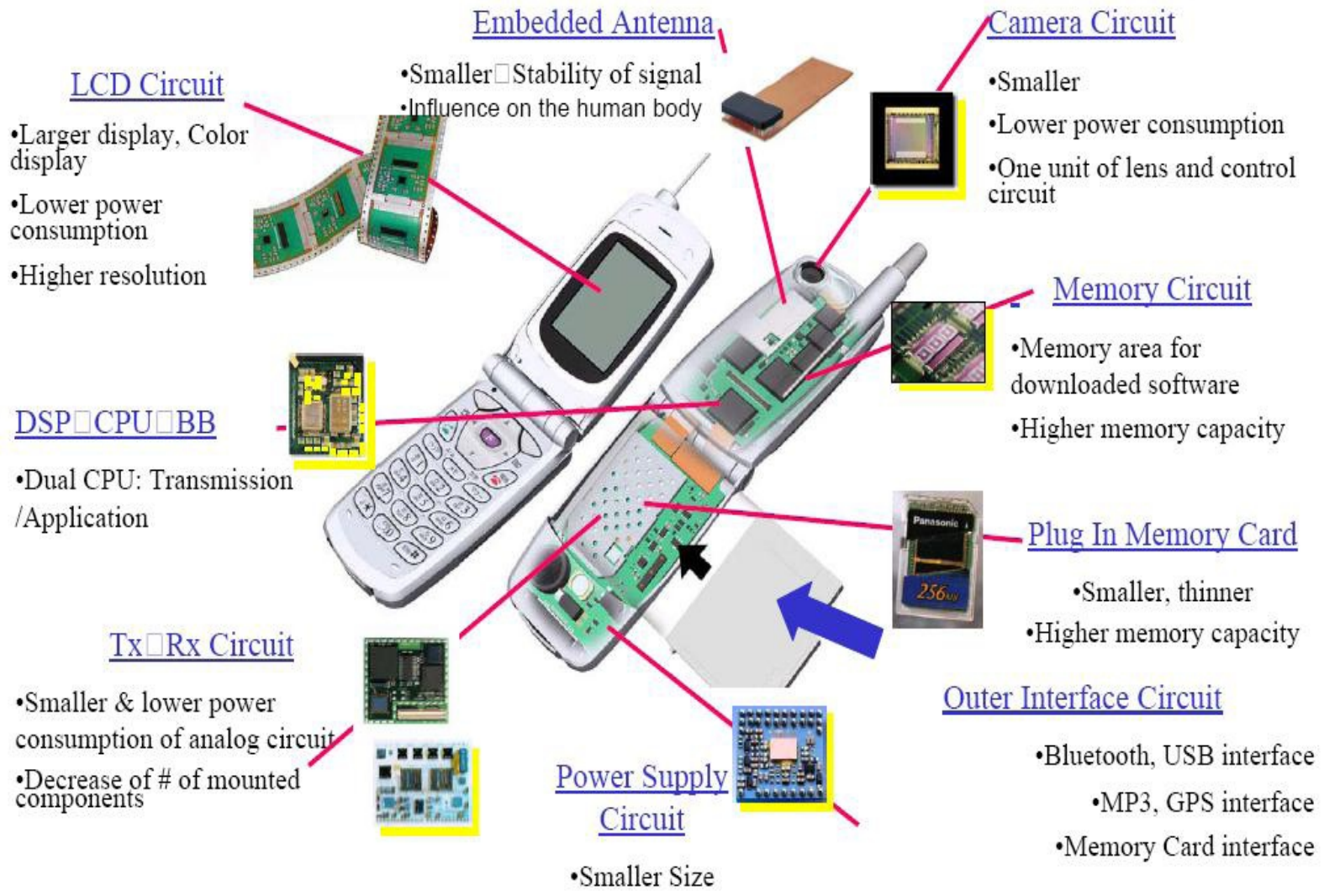
Through hole
Surface Mount
Bare die-direct
chip attach (DCA)



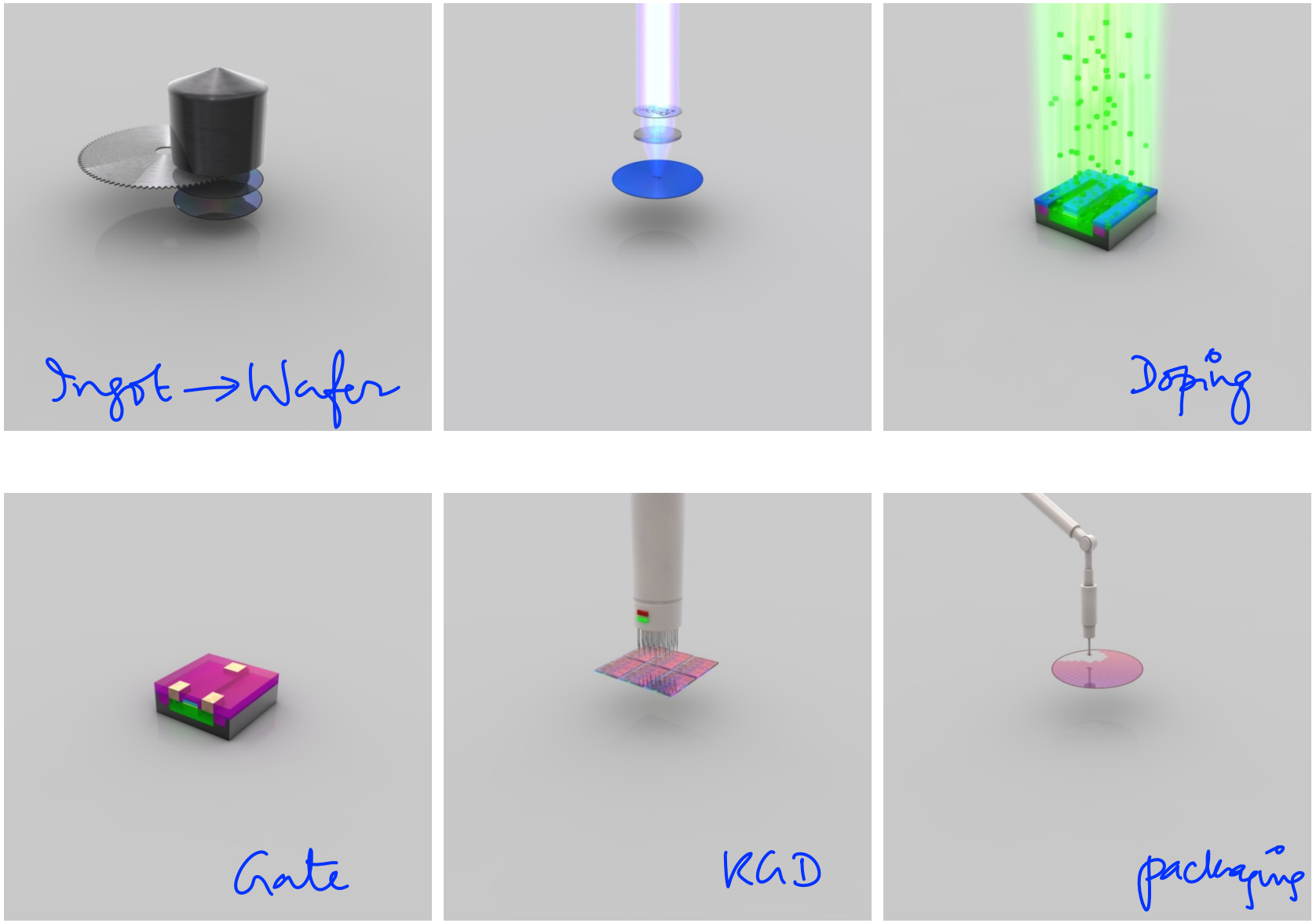
The purpose of a PWB:

- Electrically interconnect all the components
- Mechanical support to the components
- Powers up the circuit
- Dissipates heat generated by the components

An example of system-level integration in a cellular phone



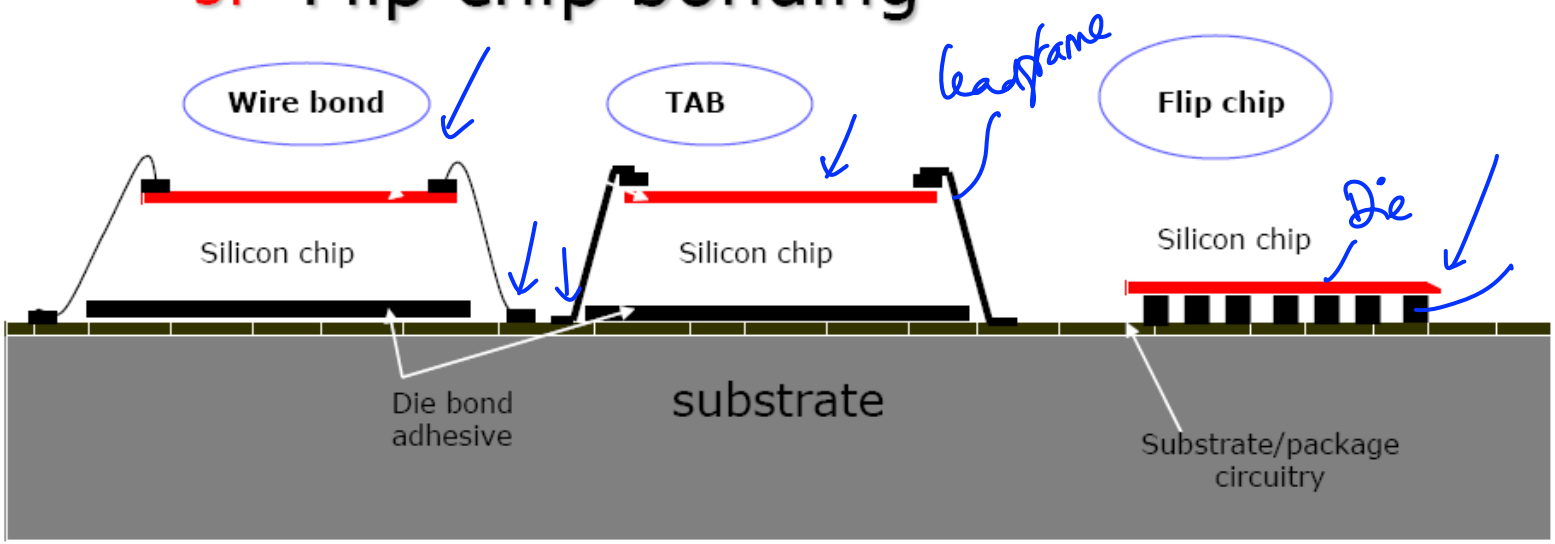
Source: *Portelligent*

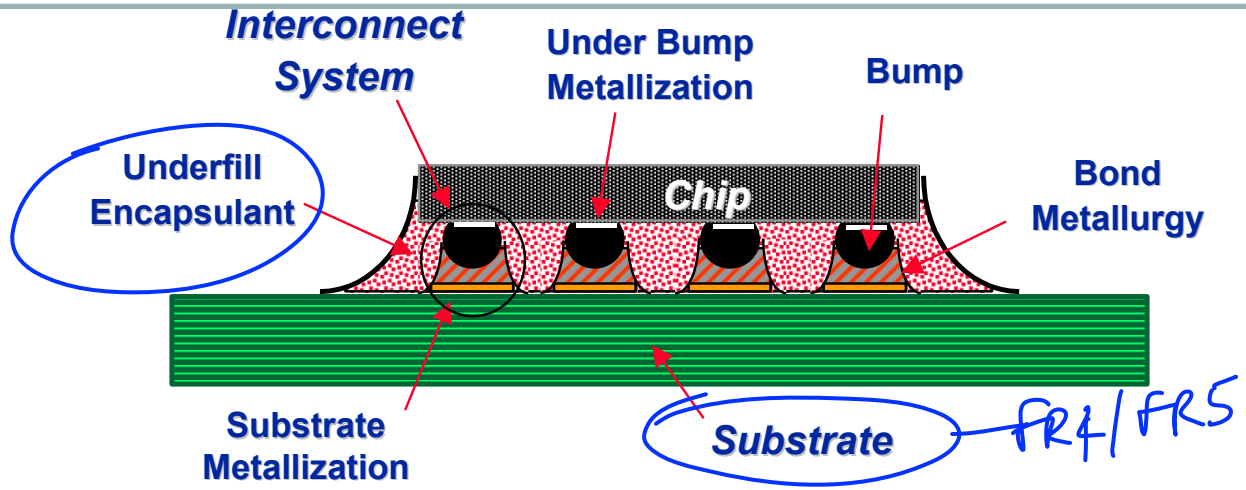


Source: *Intel*

Common 1st level interconnections

1. Wire bonding
2. Tape automated bonding
3. Flip chip bonding



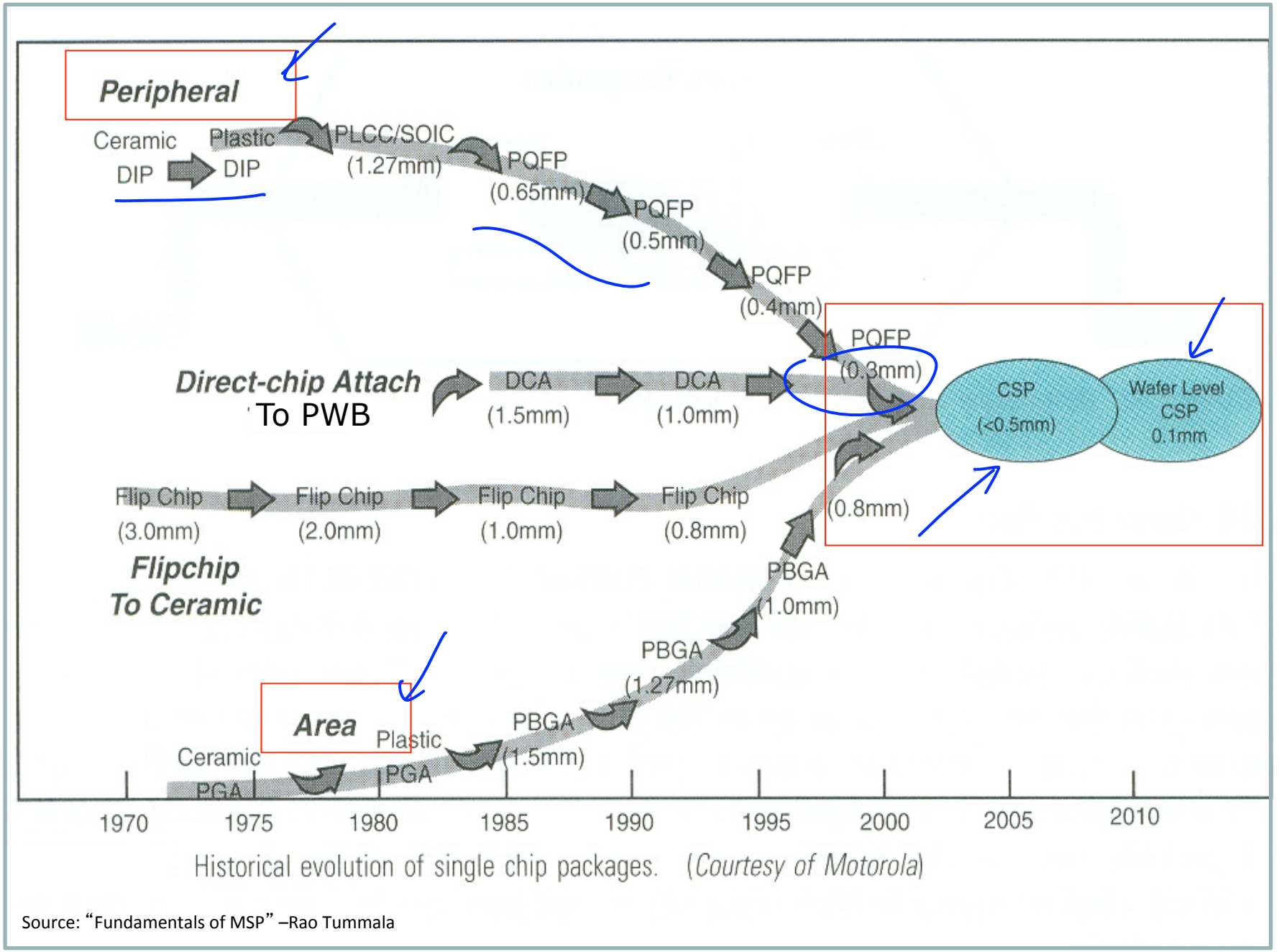


Why Underfill for Flip chip

- Non-Conductive adhesive joining surface of chip to substrate.
- Protects bumps from moisture or other environmental hazards.
- Provides mechanical strength to assembly.
- CTE of silicon is 3 ppm/ °C and typical FR4 material is 17 ppm/ °C - large strain observed in solder bumps due to this thermal expansion mismatch
- Compensates for this mismatch
- Thermally conductive; electrically insulating

CTE mismatch

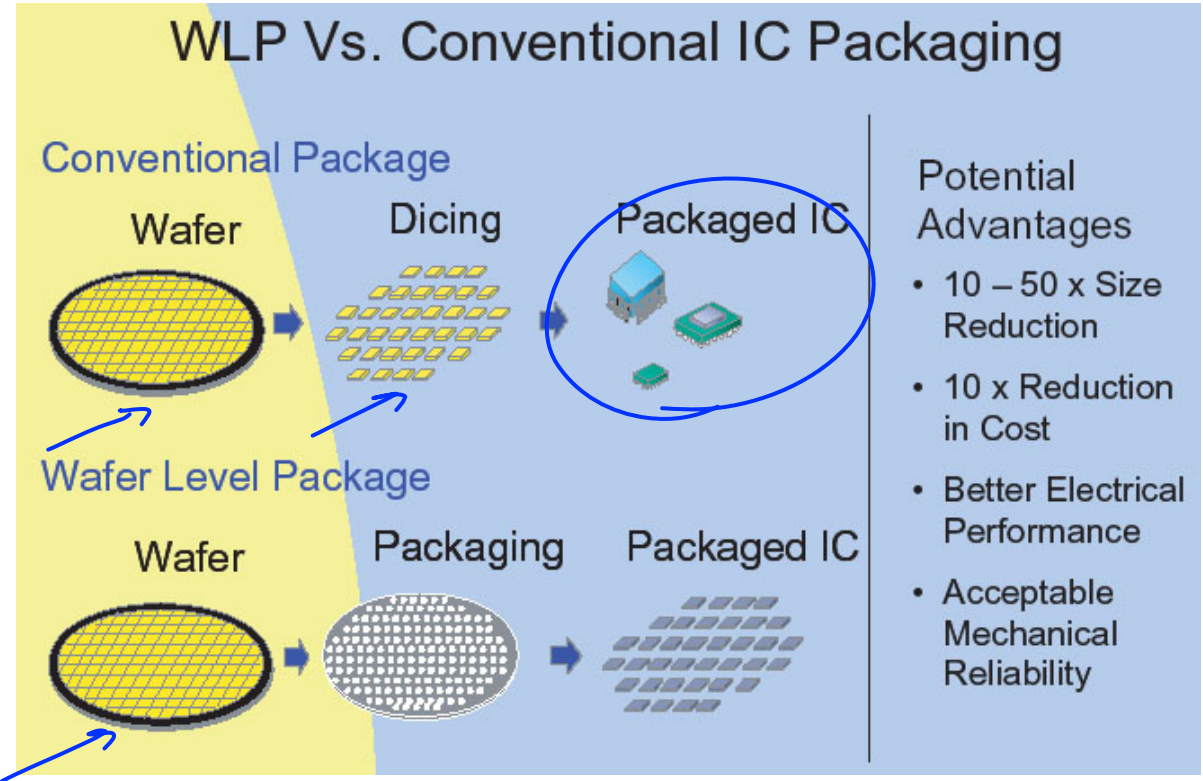
Source: "Fundamentals of MSP" –Rao Tummala



Historical evolution of single chip packages. (*Courtesy of Motorola*)

Source: "Fundamentals of MSP" –Rao Tummala

WLP is essentially a true CSP technology



No single industry standard exists at present

- Power distribution with minimum noise and electromigration
- Better signal integrity
- Lead-free solder bumping possible
- Nano interconnections
- MEMS and MoEMS fabricated interconnects
- Integrates wafer fab, packaging, test and burn-in at wafer level

Types of single chip packages

Package Type	Material	Pin Count (Total I/O)	Min. Pitch (mm)
Through-Hole			
Single In Line (SIP)	Plastic	<48	1.27
Dual In Line (DIP)	Plastic (PDIP)	<84	2.54
	Ceramic (CDIP)	<84	2.54
Surface Mount			
Small Outline (SO)	Plastic (SOP/J)	<84	1.27
Leaded Chip Carrier (LCC)	Plastic (PLCC)	<120	1.27
Quad Flat Pack (QFP)	Plastic (PQFP)	<356	0.30
	Ceramic (CQFP)	<356	
Tape Automated Bonding	Plastic (TAB)	<356	0.25
Area Array			
Pin Grid Array (PGA)	Plastic (PPGA)	<750	1.27
	Ceramic (CPGA)	<750	1.27
Ball Grid Array (BGA)	Plastic (PBGA)	<800	1.00
	Plastic (FC-PBGA)	<1700	1.00
	Ceramic (FC-CBGA)	<800	1.00
Column Grid Array (CGA)	Ceramic (FC-CCGA)	<1700	1.00
Chip Scale Package (CSP)	Plastic (CSP, μBGA)	<356	0.50
	Ceramic (CSP)	<356	0.50

High-Density Packages with Area Array

- BGA- Ball Grid Array
  - PBGA (Plastic BGA)- Summary
    - Routable Laminate Substrate (Many Layers)
    - High Pin Count (Over 2000 pins)
    - ASICs, DSPs, PC Chipsets
    - Wirebond, TAB or Flip-Chip (Build-Up) attach
    - Build-Up Technology Requires Special Via Structures

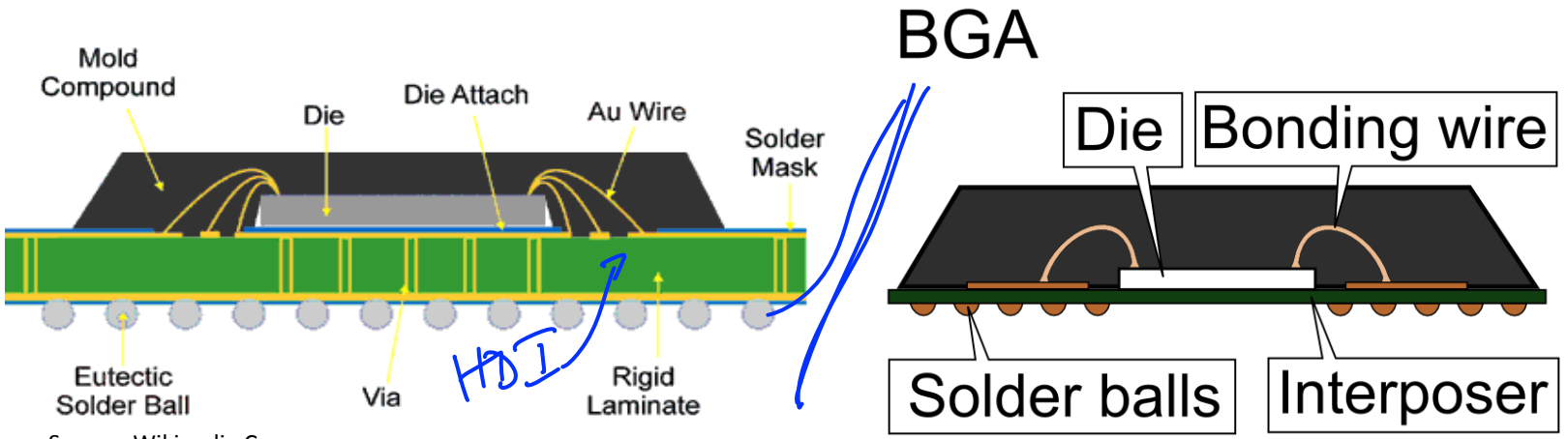


Figure Source: Wikipedia Commons

CSP- Chip Scale Packaging

- Definition: A Package is considered a CSP when the package area is no greater than 1.2 times that of the die area; when the ball pitch is equal to less than 0.5mm
- Usually Flip-Chip Attachment
- Common for Wireless Handsets and Handheld Electronics .
- Stacked die support (S-CSP- Stacked CSP); WL-CSP
- Laminate and Ceramic Substrates

Cross-section of a CSP

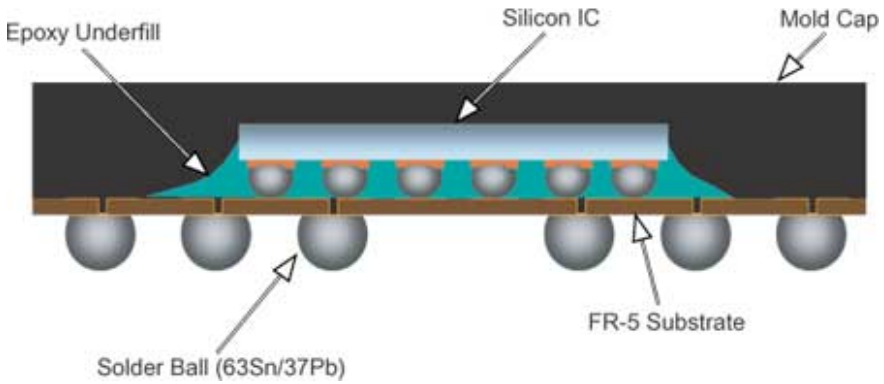
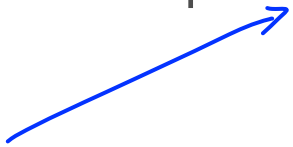


Figure Source: Amkor

Cooling

- Package must transport heat from IC to environment
- Heat removed from package by:
  - Air: Natural air flow, forced air flow improved by mounting heat sink
  - PCB: Transported to PCB by package pins
    - Better substrates for PCB and efficient PCB design
  - Liquid: Used in large mainframe computers



Some Basic Package Physical Parameters..

Substrate Material	FR4 / BT	Ceramic	Polymer	No Substrate
Die-attach	Cavity-up	Cavity-down	Stacked	
Die-package Interconnection	Wirebond	Flip-chip		
Package-PCB Interconnection	Leads	Pins	Balls	No Leads
Encapsulation	Globtop	Overmould	Hermetic	

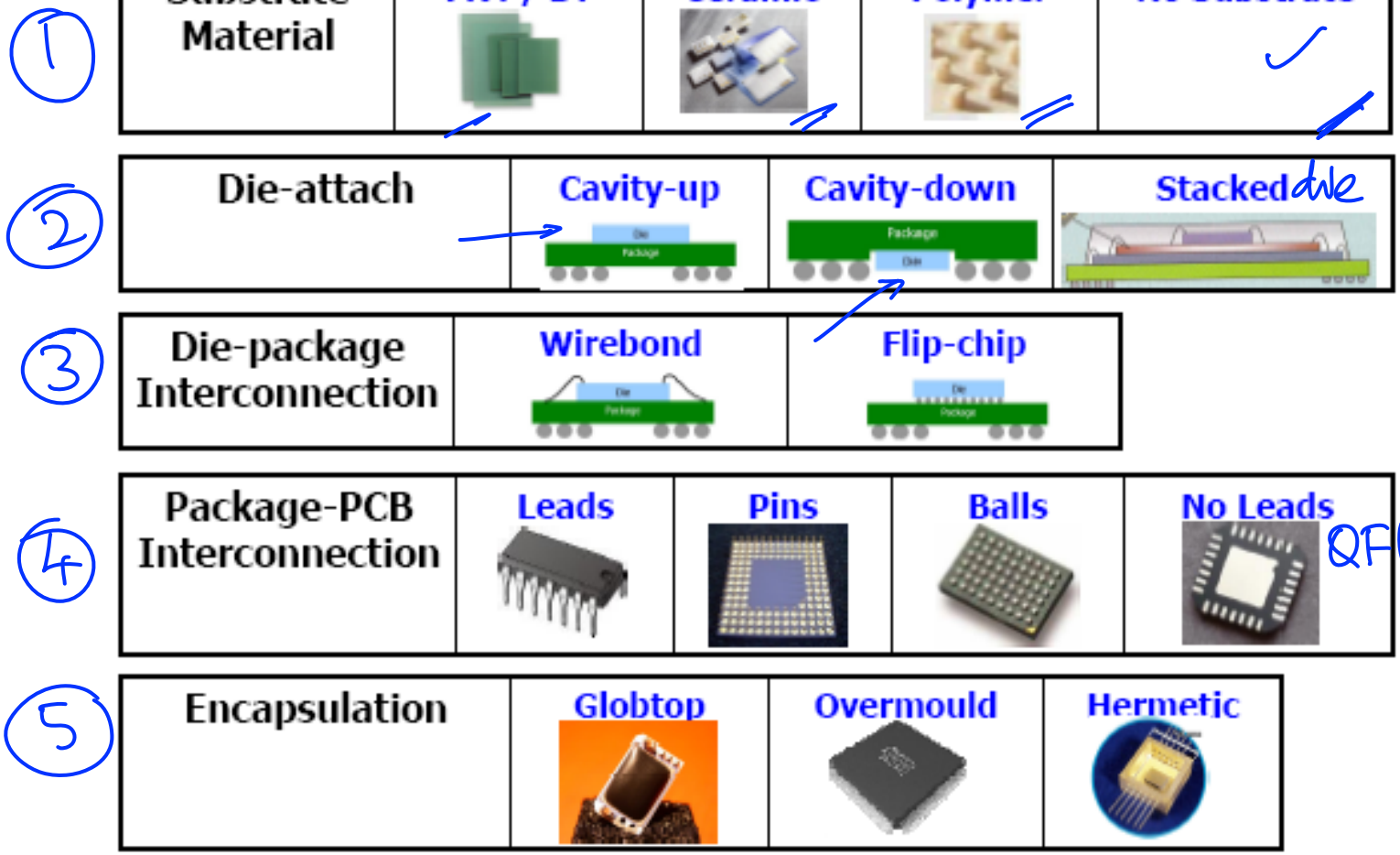
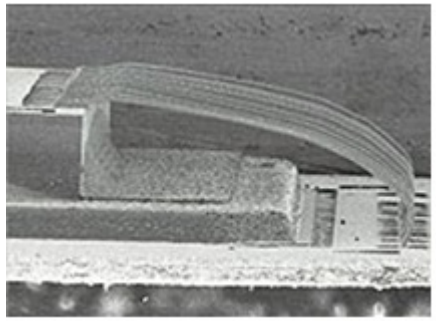


Figure Source: Dr Arun Chandrasekhar, Intel, India.

3D Packaging- Stacked Die

- **Definition:** Packaging Technology with 2 or More DIE
  - Stacked in a Single Package or Multiple Packages Stacked Together
- **Supports**
  - Wirebond Die Attach
  - Flip chip Die Attach
  - Hybrid- Combination of Flip-Chip and Wirebond
- **Packaging Applications**
  - CSP
  - BGA
  - Folded over package (PoP)
- **Benefits of 3D Packaging**
  - Smaller, Thinner and Lighter Packages
  - Reduced Packaging Costs and Components
  - System Level Size Reduction Due to Smaller Footprints and Decrease Component Count (SiP)
- Common for Wireless Handsets, Handheld Electronics and Memory Intensive Requirements.



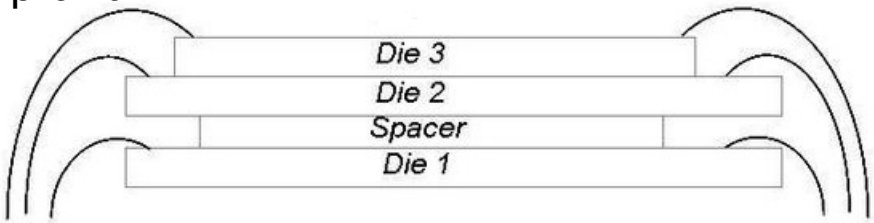
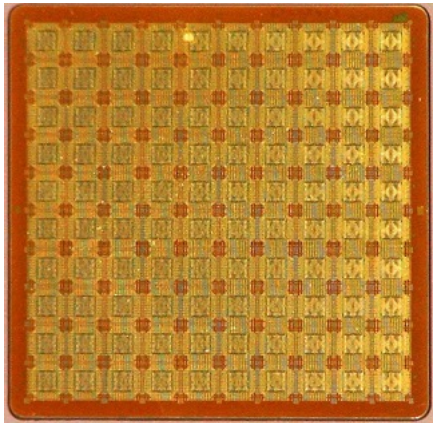


Figure Source: Wikimedia Commons (sketch)

Multi Chip Modules (MCM) or Multi chip packaging

- Industry's first MCM from IBM.
- Generally MCMs are horizontal or two-dimensional modules.

Defined as a single unit containing two or more chips and an interconnection substrate which function together as a system building block.



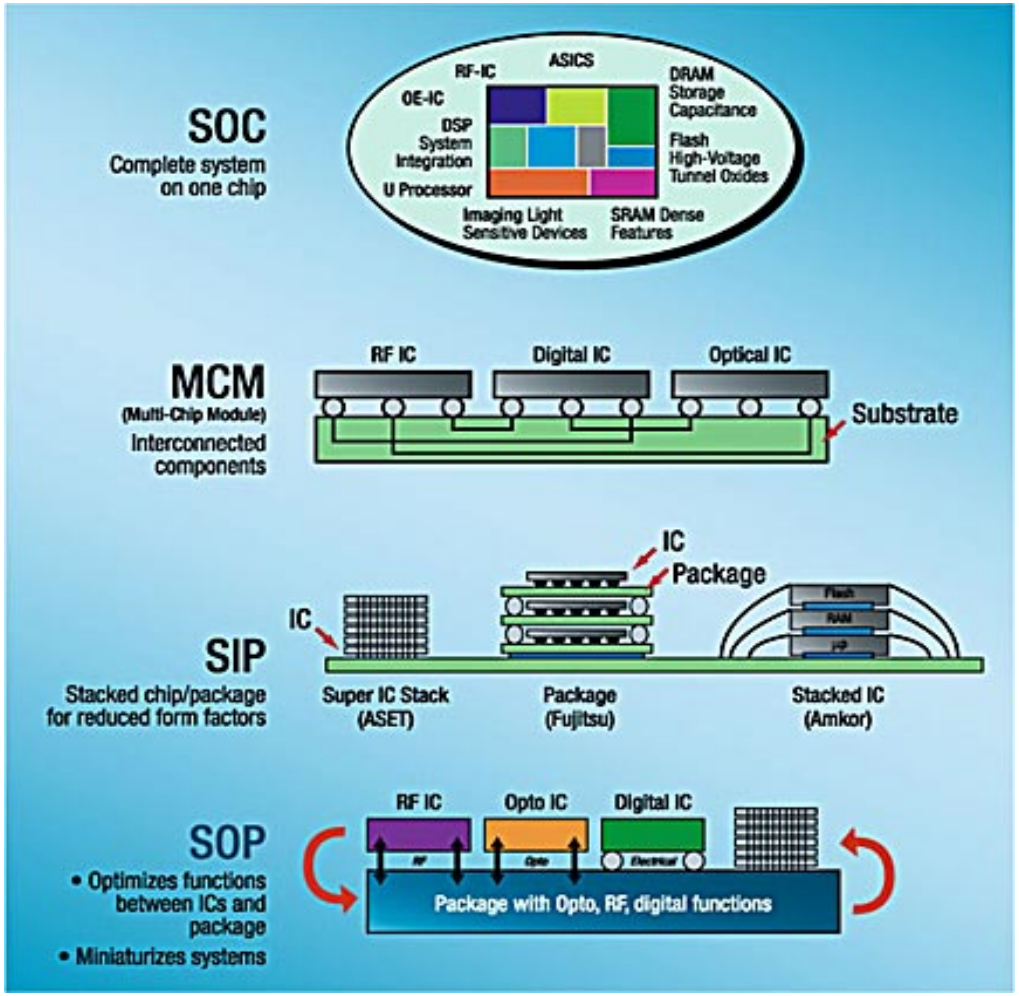
IBM's 61-layer LTCC MCM, 1992

Need for MCM

More functionality in one 'single chip'
Special circuit needs met
MCMs formed from multiple chips on a common substrate / package structure
Do away with individually packaged chips on a PWB

Figure Source: Prof Rao R Tummala, PRC, GTech.

SIP- System in Package



- System in Package is defined as the vertical stacking of similar or dissimilar ICs, in contrast to the horizontal nature of SOC.
- Benefits: simpler design, design verification and process besides minimal time-to-market.
- About 30 IC and packaging companies are producing SIP-based multichip modules.

SiP is a key technology for reducing product size and increasing product functionality in products like digital cameras and mobile phones.

Figure Source: Fundamentals of MSP- Rao Tummala

Current Trends

- 3D Packaging- Stacked Die
- Build-Up Substrates
- Flip-Chip
  - DCA- Direct Chip Attach
- SiP
  - LTCC, Bluetooth Standard
- "Green" Manufacturing
  - Removing Lead (Pb)
  - New Materials (tin, silver, copper) for Die Attach, plating, solder balls
- SOP, POP (package-on-package)

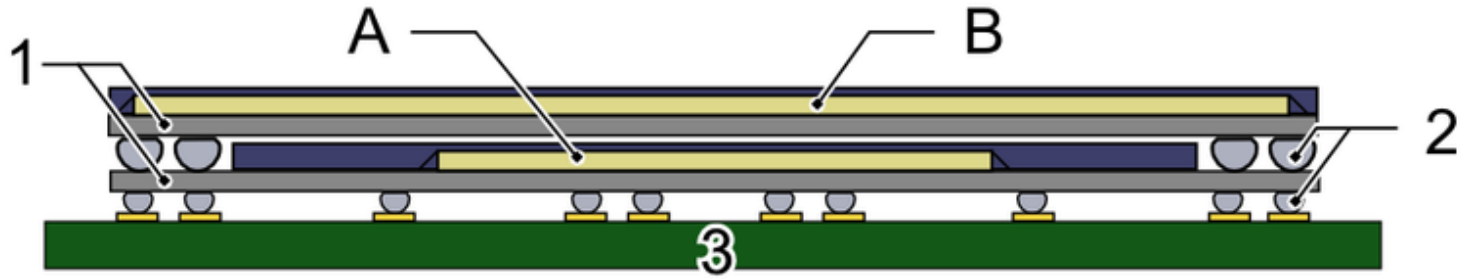


Figure Source: Wikimedia Commons

Design for Manufacturing (DFM)

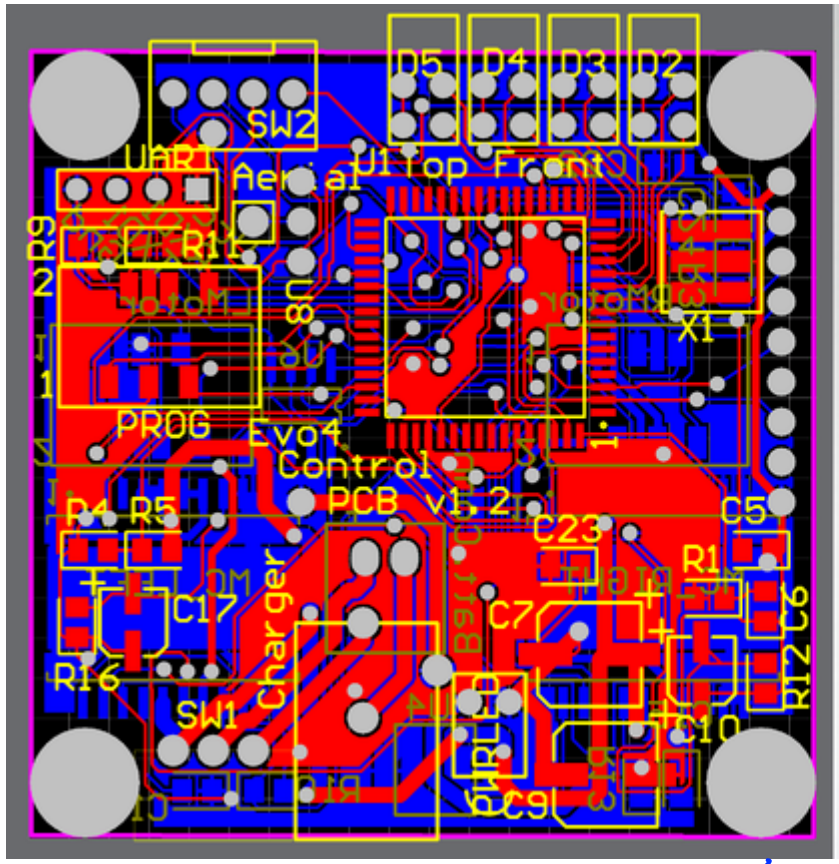
- handshake between designers and manufacturers
- bottlenecks in manufacturing
- impossible specs in manufacturing cannot be designed
- wastage of raw material can be minimised
- high yield at lower costs

Design for Reliability (DFR)

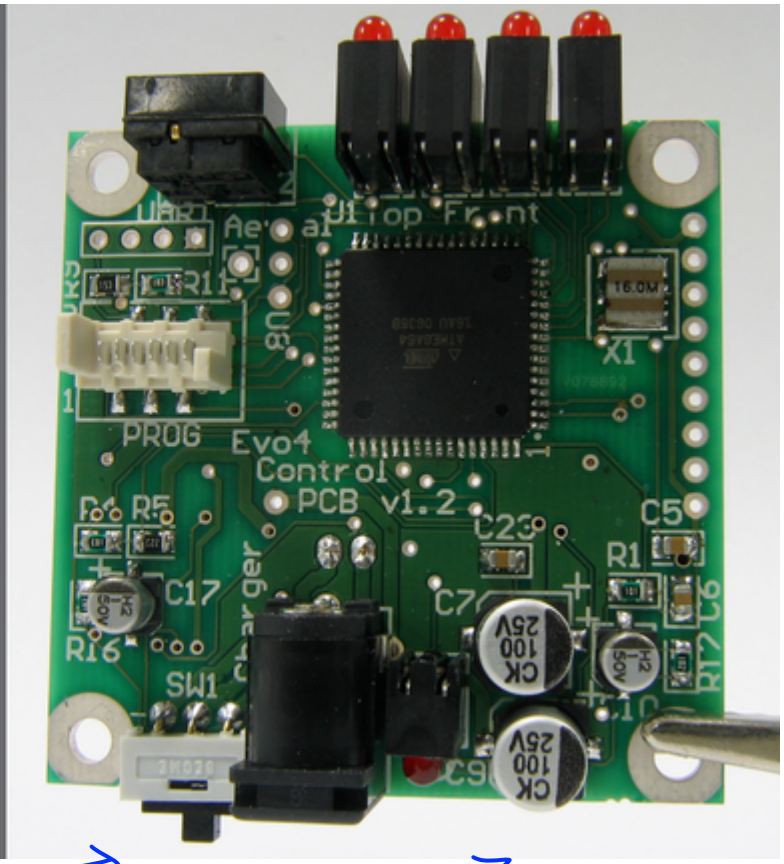
- failures to be predicted by simulation
- materials analysis is a must
- physical properties of materials used in PWBs and inner layers
- design for higher reliability- electrical and thermal
- MTTF and MTBF to be understood (complex though)
- current DFR mechanisms eliminate experimental verification

Design for Testability (DFT)

- ability to test the board efficiently after assembly
- layout of board components become crucial
- good understanding of components sizes, shapes, properties
- efficient usage of electromechanical components, if used



Example of finished layout by CAD



Example of finished board for the same design

Figure Source: Wikimedia Commons

Optimization Operations in CAD

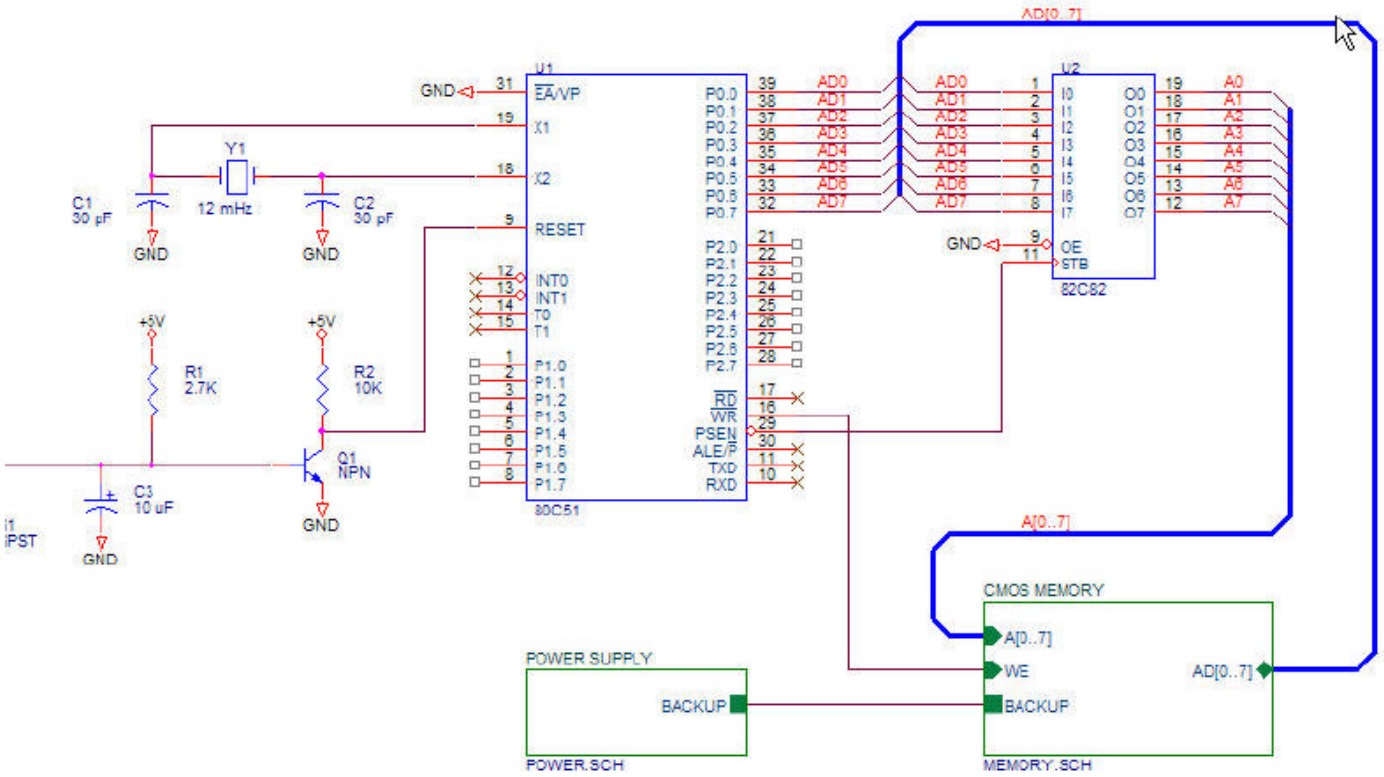
- Creation of components and footprints (THT & SMT)
- Gate & pin swapping
- Manual, interactive & automatic routing
- Clean-up and optimizing the interconnection structure
- Final operations (segments modify, track width modify, miter & fillet corner)
- Copper maximizing
- Transfer between layers

Post processing Operations

- Creating Technology files for sending to manufacturer
- EXCELLON format for NC Drilling operation
- GERBER format for photoplotting operation
  - * Photoplots are necessary for all manufacturing layers of PWB
  - * Masks are from silver halide photo films
- Assembly Drawing to be printed/documented
- Production planning document for manufacturing
- Edit software will be used by manufacturer for including tool holes, logos, batch nos. etc.

Schematic

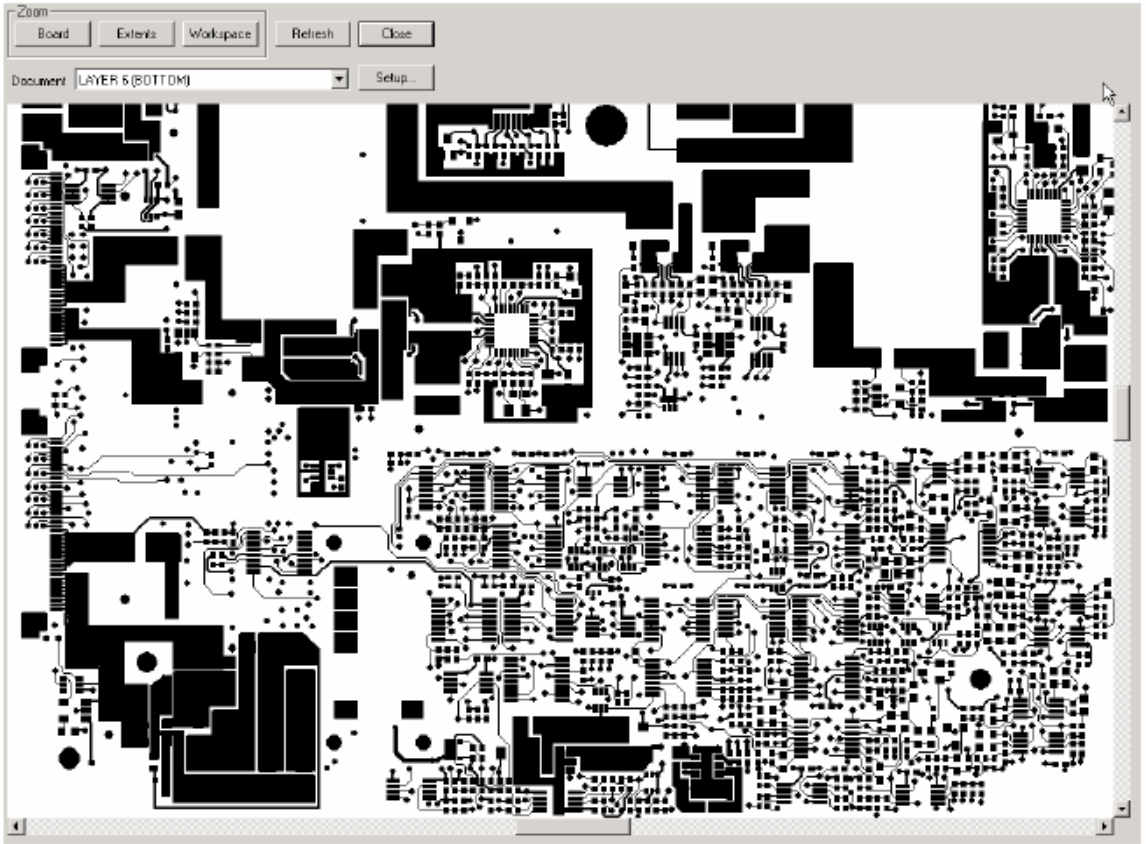
The electrical components are placed in the schematic and net connections established.



Courtesy: PCB3D.COM

Gerber Files: Electrical Layers

These Gerber files are processed to create each electrical layer (internal and external) that will ultimately be finished in copper on the pcb.



Courtesy: PCB3D.COM

Basic approaches for Fabrication

- Subtractive Process

- Additive Process

- Semi-additive Process

Etching

Plating

Double sided board manufacture

- Design
- Photo-tooling (1:1)
- Drill holes (PTH)
- Plate (electroless)
- Image circuit
- Plate (Cu electroplate)
- Plate (Sn or Sn-Pb electroplate)
- Strip
- Etch
- Strip and Protect before assembly

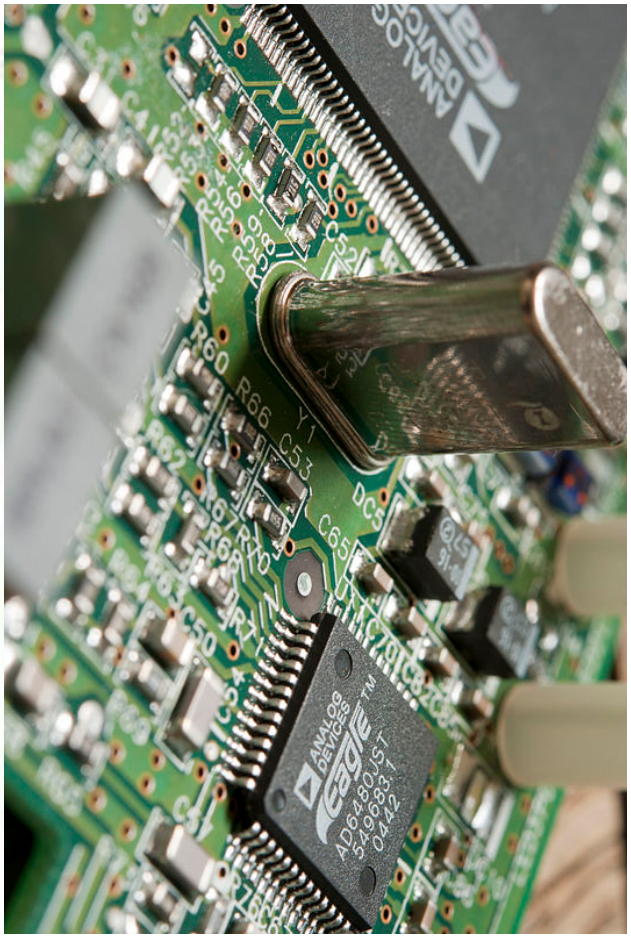


Fig. source: Wikimedia Commons 2011

Multi Layer-Types

1. Laminated Multi layer Structures

Made by stacking separately made layers and Pressing them into to a mono block in a press

Called Conventional MLBs

2. High Density Multi layer Structures

HDI

Made by sequentially adding layer by layer onto a core substrate

Interconnect Hole Formation

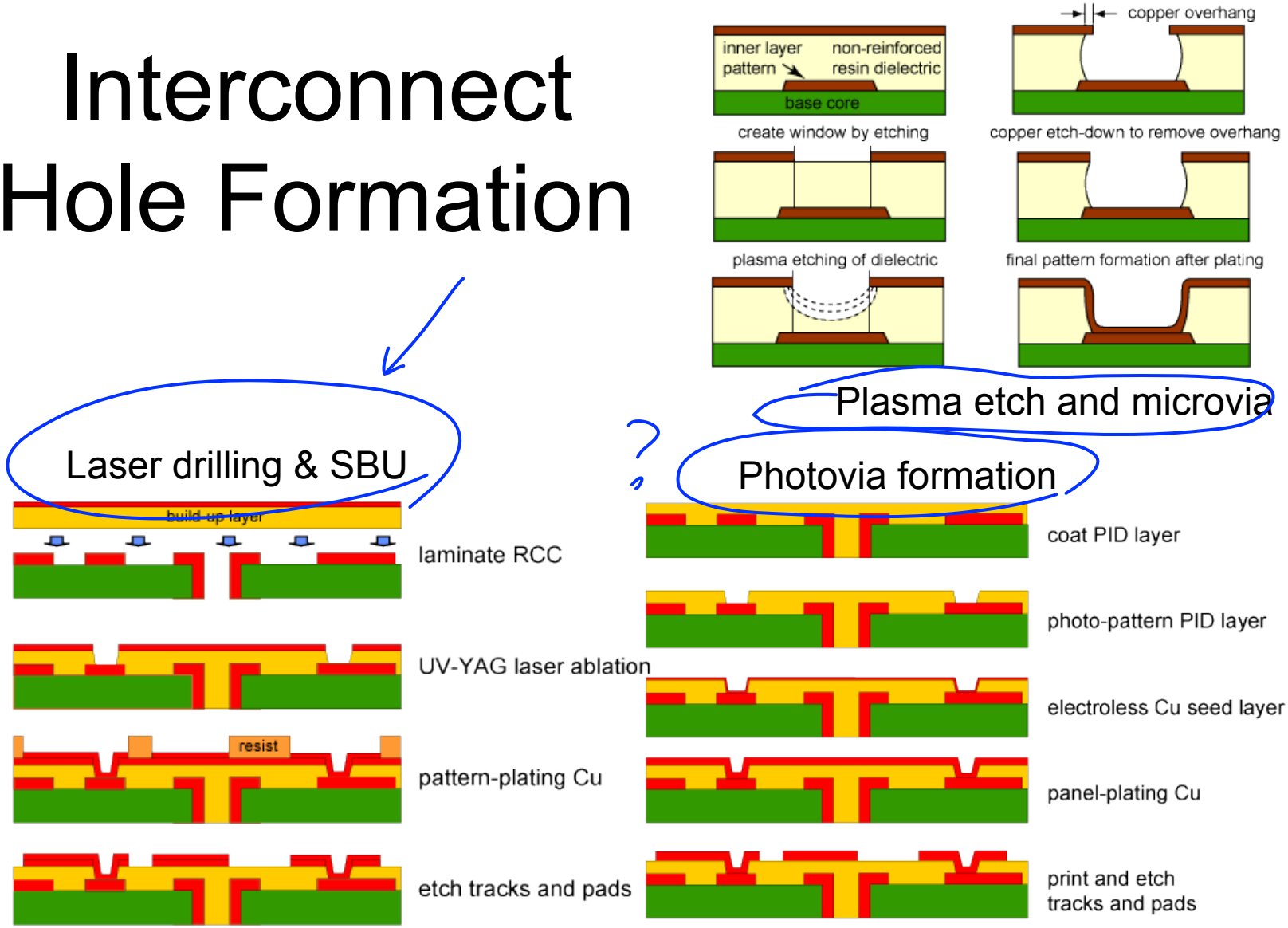
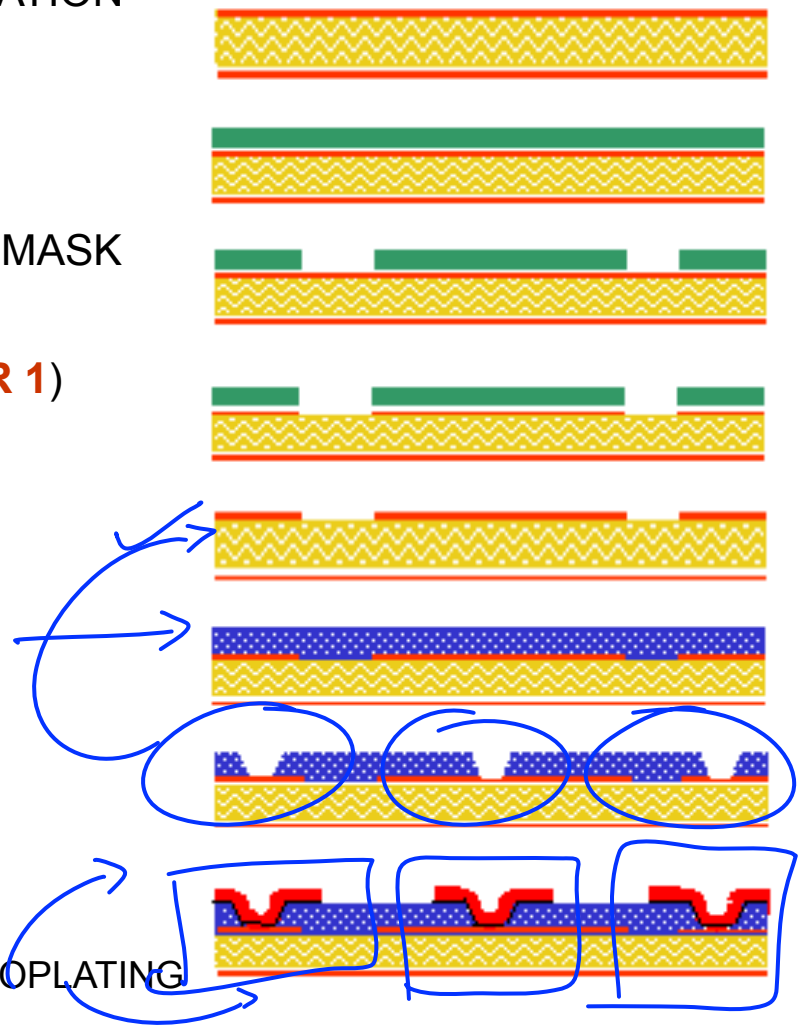


Figure Source: Dr Gerard Edwards, University of Bolton, UK

Sequential Build Up Process Flow

1. CHOOSE SUBSTRATE; SURFACE PREPARATION
2. COAT PHOTORESIST AND PRE-BAKE
3. PHOTO-EXPOSE, DEVELOP, CURE USING MASK
4. SUB-ETCH COPPER LAYER (**LAYER 1**)
5. STRIP PHOTORESIST
6. APPLY PHOTO-POLYMER DIELECTRIC
7. PHOTO-EXPOSE, DEVELOP, FINAL CURE
8. METALLIZATION PROCESS
   - •ELECTROLESS PLATING, ELECTROPLATING

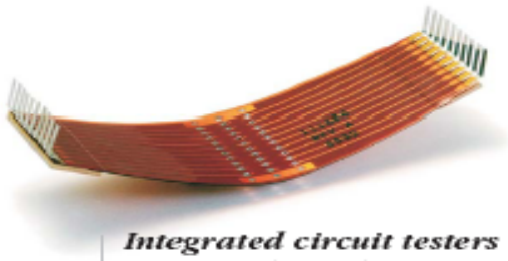
(**LAYER 2**)



Air bag systems, Engine controls, ABS

Cameras

Cardiac pacemakers

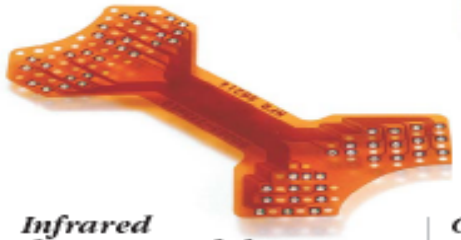


Integrated circuit testers

Bar code equipment

Calculators

Satellites



Infrared detector modules

Clinical analyzers

Military radio

Avionics

Printers

SMT - The Manufacturing Steps

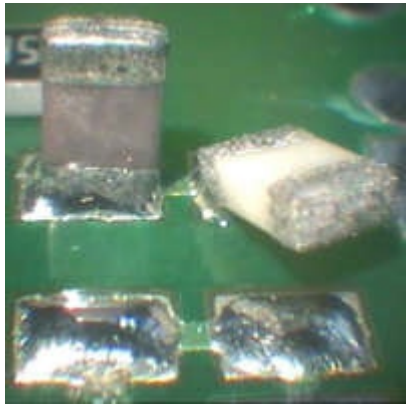
1. Attachment media dispensing
2. Component placement
3. Attachment media curing
4. Soldering- attachment, joining
5. Cleaning the joints
6. Testing

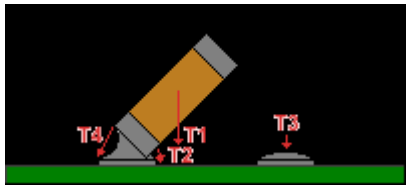
Methods of SMD and mixed boards assembly

- Wave Soldering
  - Adhesive application
    - Screen printing
    - Stencil printing
    - Syringe dispensing
  - Pick and Place component
  - Curing adhesive
    - Curing at specified temperature; ~100C
  - Fluxing
    - Foam
    - Spray
    - Wave
  - Wave Soldering
  - Cleaning and Testing

- Reflow Soldering
  - Application of solder paste
    - Screen printing
    - Syringe dispensing
    - Stencil printing
  - Pick and place component
  - Tacky cure
  - Reflow Soldering
    - IR reflow
    - Thermal convection
    - Vapor phase reflow
  - Clean
  - Test

SMT Failures Library-
Tomb stoning and Skewing



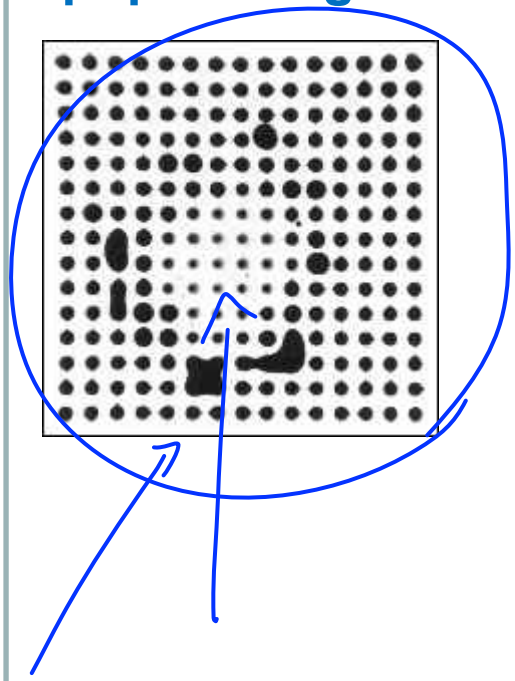


- Also called Manhattan effect, can be observed during reflow process where the chip components are lifted and stand on one end terminal.
- A variation of this is skewing.
- Caused by unequal soldering conditions on the two solder joints, either due to different melting temperatures and times, or due to volume of solder paste dispensed. Reflow in nitrogen atmosphere has seen an increase in this phenomenon.
- Ensure that the pad layout is correct and check the thermal profile for reflow soldering. Check the dispensing volume of solder paste on the pads.
- T4> T1+T2+T3 (force)

Figures courtesy: www.smt.cn

SMT Failures Library-

BGA joint failure due to delamination or popcorning effect



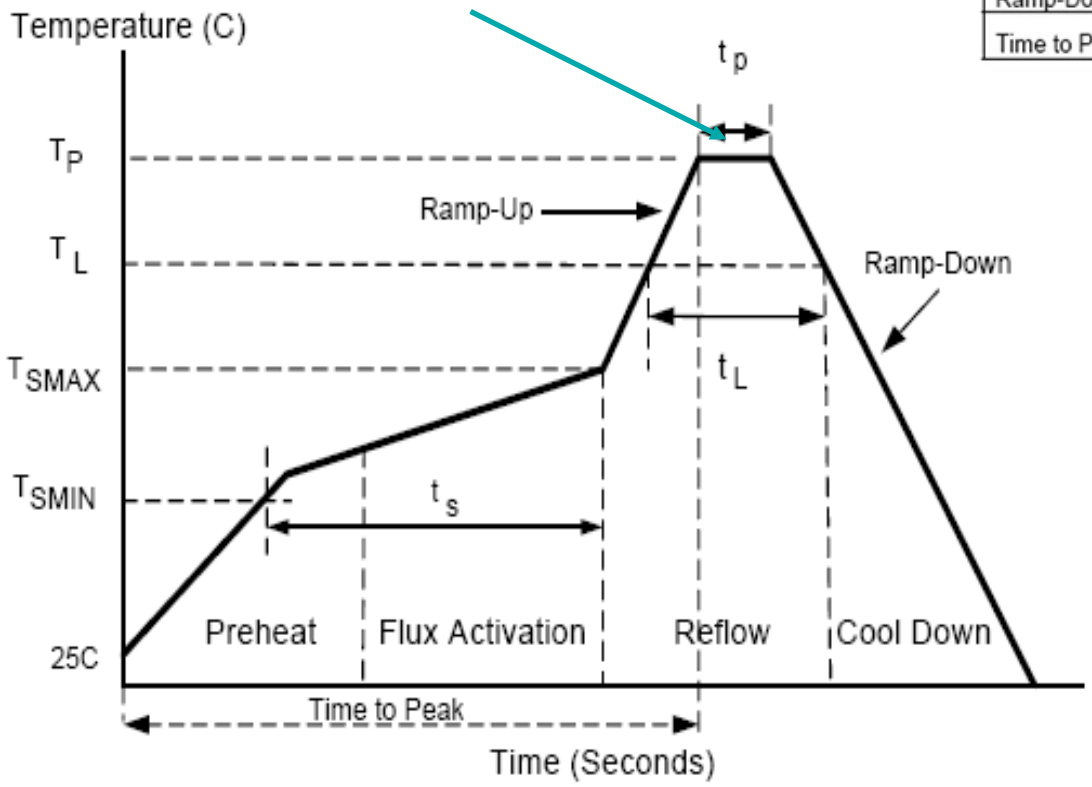
- This is an X-ray picture of a soldered BGA device.
- Some areas are soldered well, some (centre) are poorly soldered, some are shorted too.
- Causes could be insufficient solder paste dispensing for all the BGA pads.
- If additional solder paste is not used, then the defect could be due to BGA popcorning effect (delamination) caused by trapped moisture in BGA outgassing during reflow process.
- Check solder paste material, BGA ball material, remove moisture by pre-baking, or setting your thermal profile for more pre-heating times.

Figures courtesy: www.smt.cn

Temperature Profile in Reflow soldering (IR soldering)

N_2 atmosphere Reflow

30-60s typically



Ramp-Up	Average Ramp-Up Rate (T_{SMAX} to T_p)
T_{SMIN}	Preheat Peak Min. Temperature
T_{SMAX}	Preheat Peak Max. Temperature
Tp	Max. Reflow Temperature
T_s	Time between T_{SMIN} and T_{SMAX}
T_L	Solder Melting Point
t_L	Time Maintained above T_L
t_p	Time within 5C of Peak Temperature
Ramp-Down	Ramp-down Rate
Time to Peak	Time from 25 °C to Peak Temperature

Typical times for

Pre-Heat is 90s (2°C/sec)
Soaking is 90-120s (0.5°C/sec)
Reflow is 30-60s (1.5-2°C/sec)
Cool gradually (3°C/sec)

Flux based soaking times

1. Low activated paste: 90sec
2. Standard: 60sec
3. Highly activated:30 sec

Best Alternatives for Lead

96.5% Tin; 3.0% Silver and 0.5% Copper adopted by Japanese
95.5% Tin; 3.9% Silver and 0.6% Copper adopted by NEMI

SAC 305 alloy

SAC 405 alloy

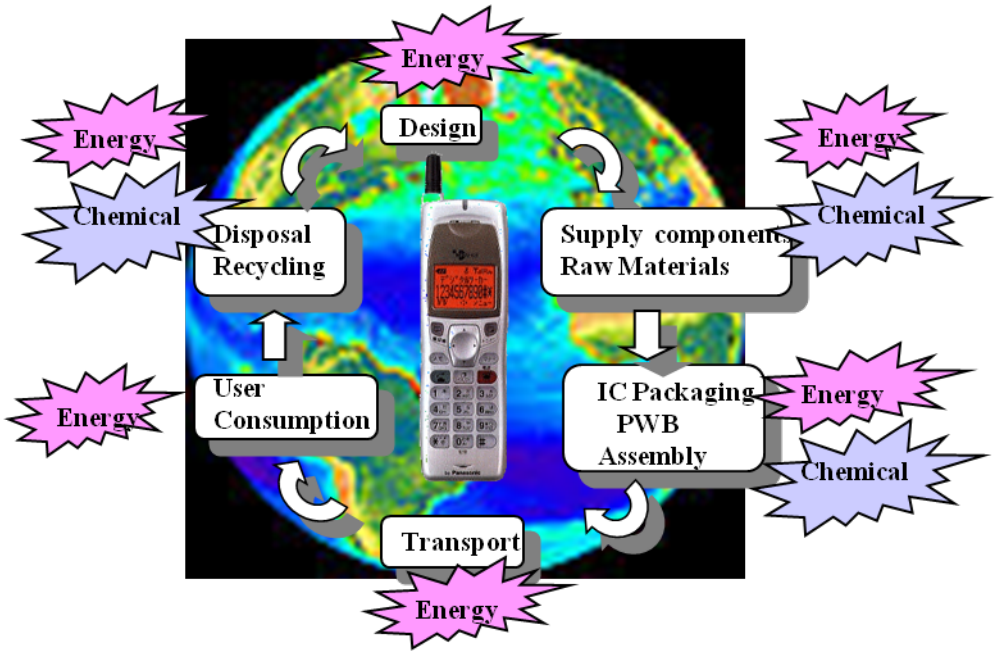
- Silver provides mechanical strength; improves resistance to fatigue from thermal cycles.
- Copper lowers the melting point, improves resistance to thermal cycle fatigue and improves wetting properties of solder
- Bismuth lowers the melting point and improves wettability
- Indium lowers the melting point and improves ductility
- Zinc lowers the melting point and is low-cost. But is susceptible to corrosion.
- Antimony is added to increase strength.

GREEN ELECTRONICS

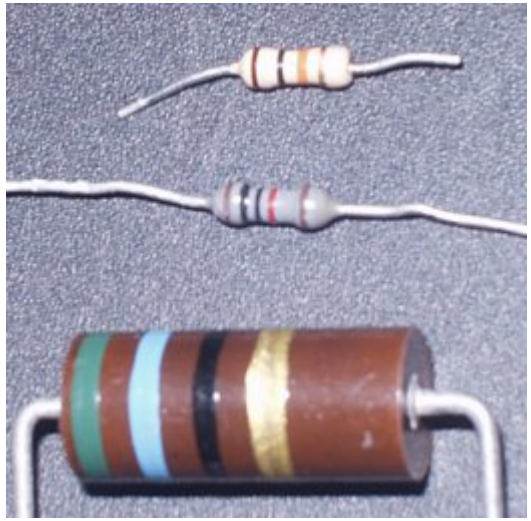
WHAT IS THE ISSUE AS FAR AS ELECTRONICS PACKAGING IS CONCERNED? SOME BASICS TO UNDERSTAND!

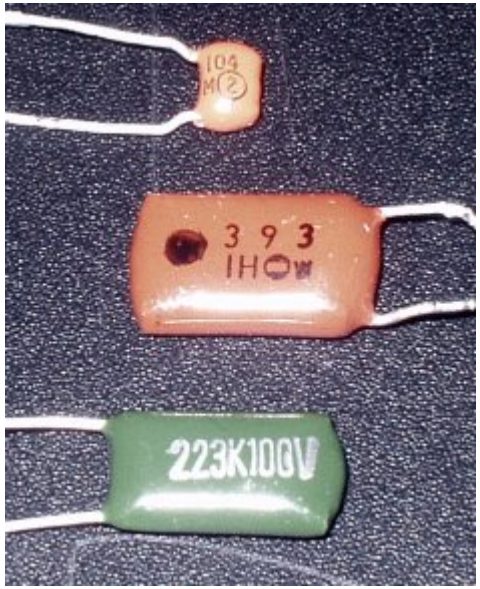
Firstly, let us understand the life cycle of an electronic product:

- Electrical, mechanical and chemical design
- Raw materials, production of IC and passive components, organic board fabrication, involving a variety of chemicals
- Assembly of components using a variety of harmful materials such as Lead.
- Assembly of the resulting electronic boards into end products such as cellular phones, laptops or camcorders etc.
- Transportation of these products to the customers
- Usage and consumption of products
- Disposal and recycling

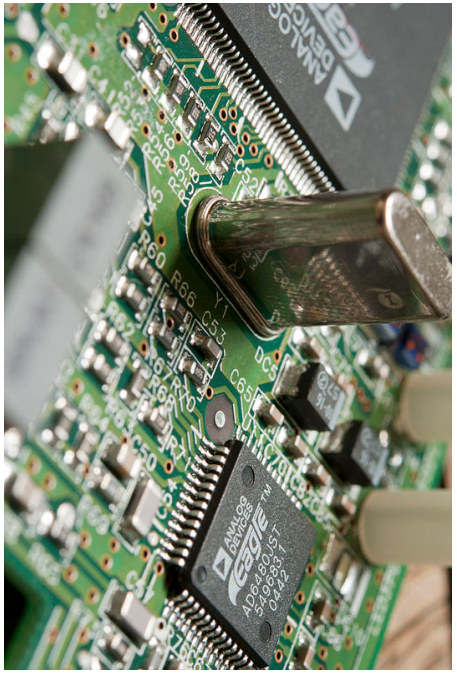


Courtesy: "Fundamentals of Microsystems Packaging": Rao Tummala



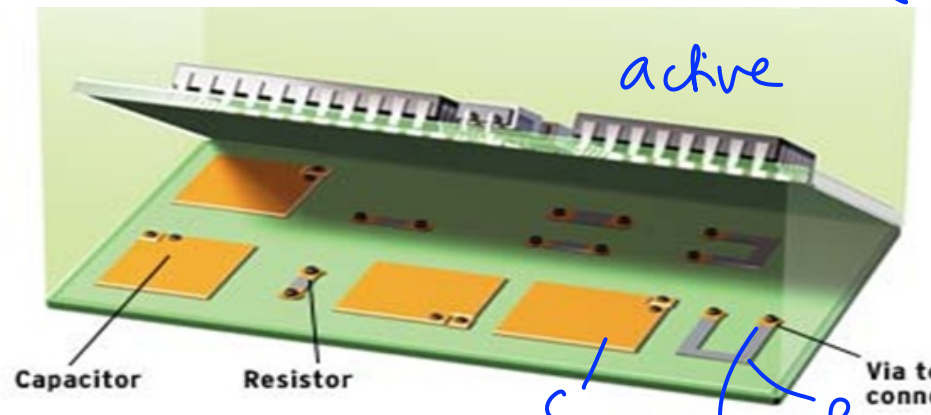


Through-hole resistors and capacitors



Surface mount devices

SMD



active

Embedded Passives

C

R wires

Embedded concept

Source: Wikimedia Commons

Electrical and Thermal Issues in Packaging

- Electrical Issues
  - Interconnections
  - Parasitic effects
    - Resistance
    - Capacitance
    - Inductance
  - Effect of temperature, current flow
  - Conductor width assessment
  - Issues in HF and fast-switching systems
  - High-speed digital circuits design
- Thermal Issues
  - Basic heat transfer concepts
  - Modes of heat transfer
  - Cooling techniques
  - Concept of thermal resistance
  - Failure modes in electronic equipment
  - Heat sinking methods
    - Passive and active

Materials and Process Issues in Packaging

- Materials Issues
  - Integrated Circuit Packaging
    - IC Packages
  - IC Assembly
  - System-level packaging
    - Boards
    - Board Assembly
    - Interconnections
- Properties
  - Electrical
  - Thermal
  - Mechanical
  - Chemical
- Processes
  - Thick-film
  - Thin-film
  - PWB

Finally, is packaging an academic subject?

FAQ's

- What are the expected benefits from this course?
- Does industry consider packaging in its product design?
- How can I get into specific topics in packaging, after this introductory course?

Thanks to NPTEL for supporting this course.

- Thanks to the participants in this course
- Assignments are posted
- Glossary of packages is posted
- Other relevant reading material posted
- Queries on specific topics can be sent by email to instructor

G V Mahesh
Faculty Member, DESE
Indian Institute of Science
Bangalore 560012

mahesh@dese.iisc.ernet.in