Review

IC

Die
KGD - Known Good Die

Chip
└ Singulated die
active device
Wafer
Wafer fab (fabrication)

→ first level packaging

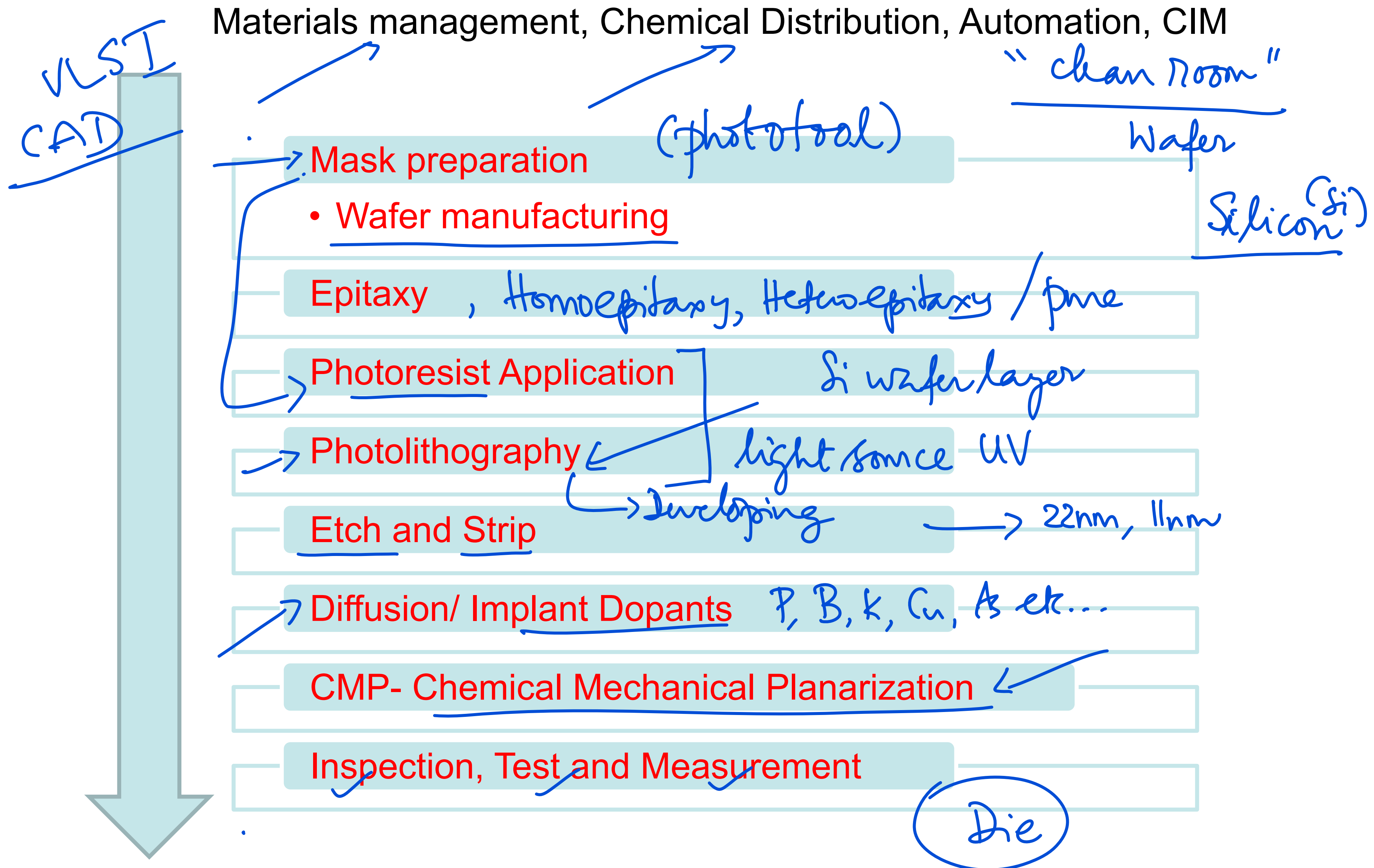
PCB (PWB)

Printed Circuit Board
Printed Wiring Board ✓
Printed Circuit Board Assembly (PCBA)
└ Types
└→ 2nd level package

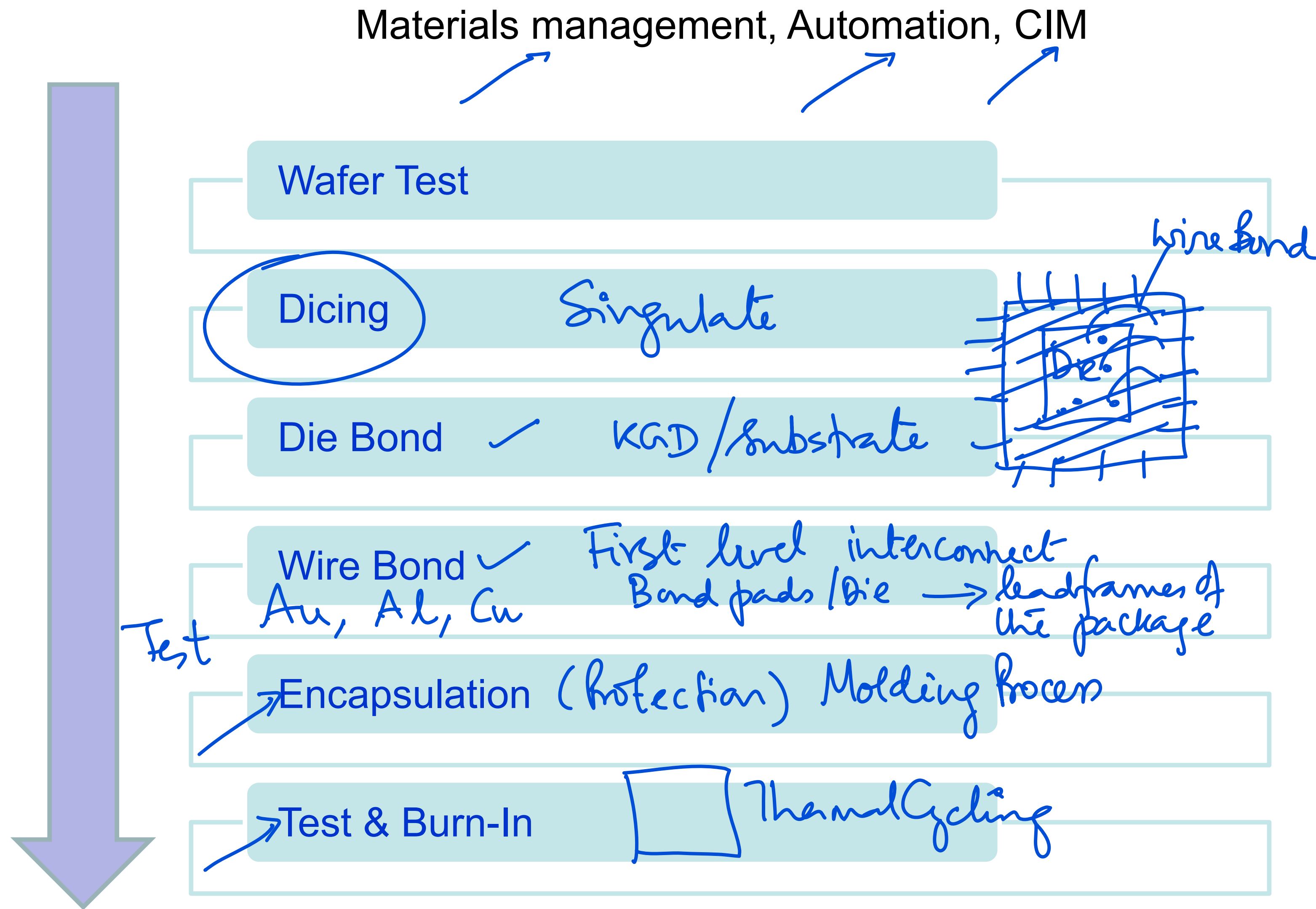
→ organic (plastic)
inorganic (ceramic)

CHAPTER/MODULE 2:
SEMICONDUCTOR FABRICATION AND PACKAGING

Fabrication overview: Front-end



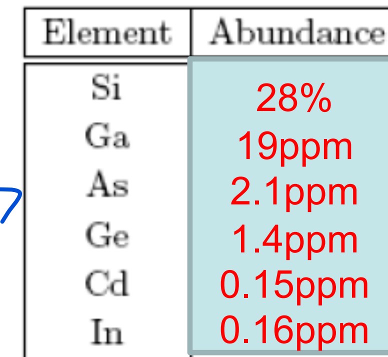
Test, Assembly & Packaging :Back-end



Some Basics

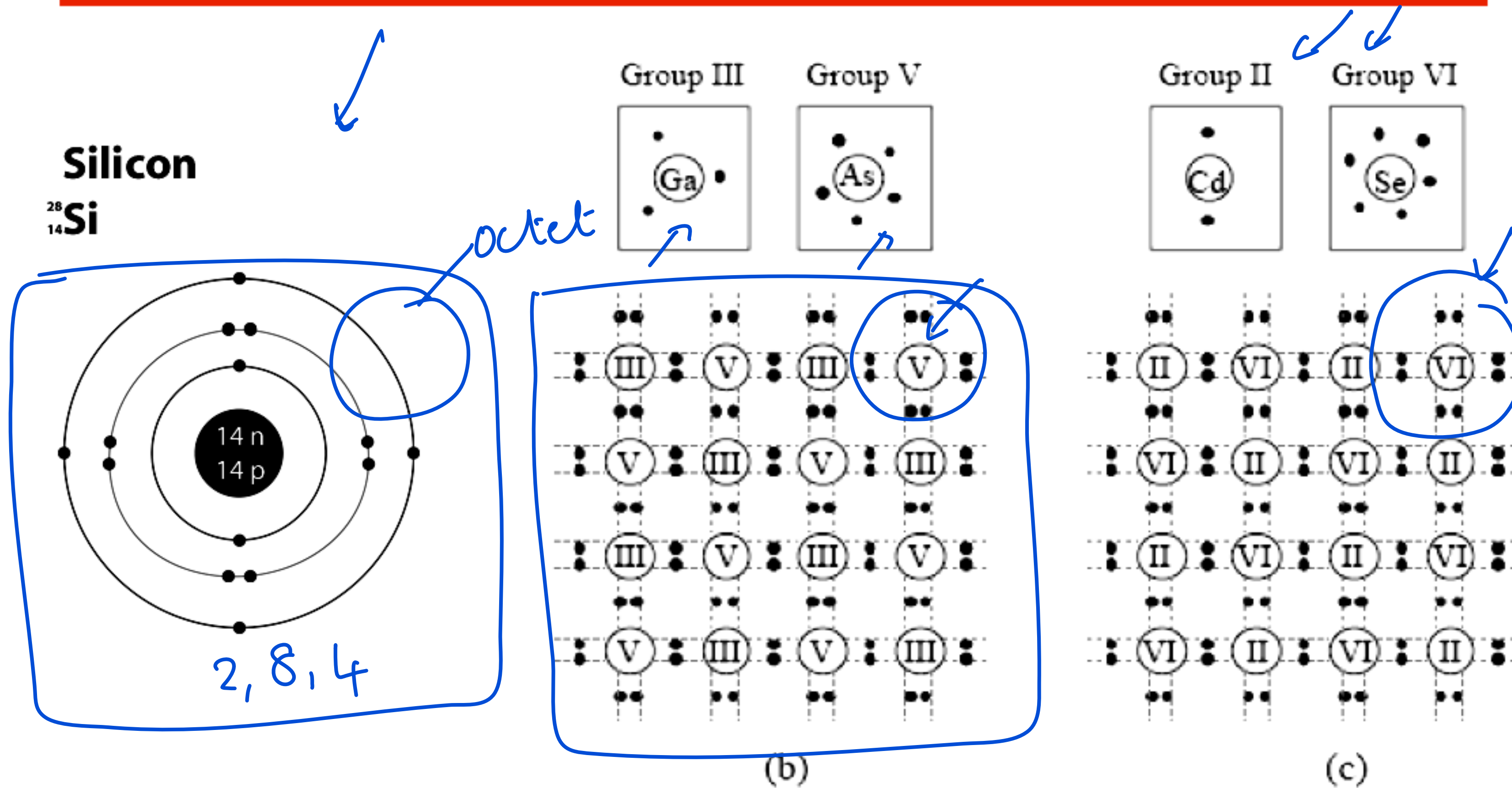
- Semiconductor has resistivity lying between that of conductor and insulator
- It establishes its conduction properties through a complex quantum mechanical behaviour within a periodic array of semiconductor atoms.
- The resistivity is proportional to the free carrier density and this can be changed widely by doping different atomic species.
- Some dopants establish electron carrier density (n-type) and some establish hole carrier density (p-type).
- Electric fields enable electric switching between a conducting state and a non-conducting state. (carrier transport)
- Group IV elements: Ge, Si, C and Sn;
- Si is the most commonly used because of its abundance on earth.

Periodic Table



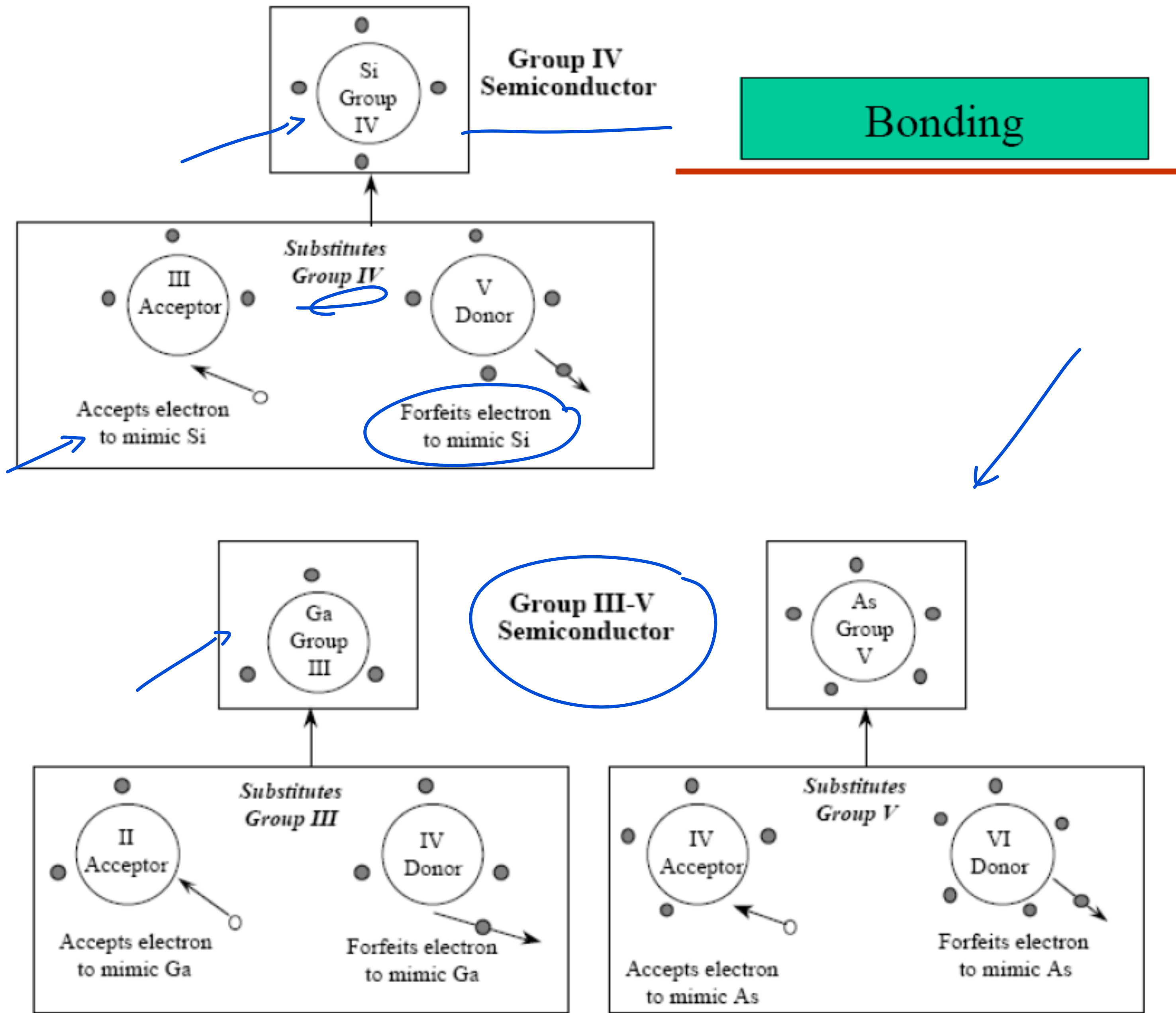
Element	Abundance
Si	28%
Ga	19ppm
As	2.1ppm
Ge	1.4ppm
Cd	0.15ppm
In	0.16ppm

Formation of Semiconductor crystals



Bonding arrangements of atoms in semiconductor crystals. (a) Elemental semiconductor such as silicon. (b) Compound III-V semiconductor such as GaAs. (c) Compound II-VI semiconductor such as CdSe.

Bonding



Everything starts with sand...

Metallurgical-Grade Silicon (MG-Si)

SiO_2 + 2C → (2000 °C) Si + 2 CO

quartz sand, carbon, silicon, carbon monoxide

Purity: 97% but we need: 99.99999%

Quartz

99.99999

Eleven Nines Purity of Si

Purity

Manufacturing: A Lithographic Process

- Photographic glass plate (mask)
- Each layer is projected to the silicon die

Fabrication

Si - Ingot → Si - Wafers → Wafer Processing (Oxidation, Masking/Patterning, Etching) → Encapsulated IC → Wire Bonding → Die Attach → Processed wafer

Source: Peter Nilsson, LTH, Sweden

Wafer

Intel use 30cm wafers in 90nm technology

300mm 450mm

Each mask is repeated with a stepper

For us: MPW - many designs share the same reticule

Reticule

Silicon dies (chips) after die sawing

Clean Room classifications

class 1	1/cuft	= 70.5μm
class 10	10/ft³	"
class 100	100	"
class 1000	1000	
class 10000	10000	

Wafer Stepper

UV

Light goes through the mask, lens and the objective

Clean room

clothing

particles in the air

- air in a city: 15 million -100 million particles per ft³
- air in the mountains: up to 10 million particles per ft³
- air in a clean room for ICs: 1 - 100 particles per ft³

AIR SHOWER

Source: Peter Nilsson, LTH, Sweden

Transport and Mobility of electrons or holes

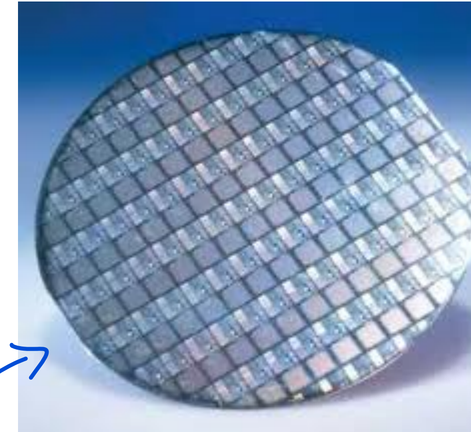
Electron mobility of semiconductors is used to describe the relation between the drift velocity of electrons or holes in a solid material or electrons/ions in a gas in an applied electric field.

Unit $cm^2/V.s$

Strongly dependant on impurities and dopants. The conductivity of the semiconductor is dependant on the mobility of the dominant charge carrier.

Typical electron mobility of
GaAs at 300K is ~9000 cm2/V.s
Si at 300K is ~1400
Ge at 300K is ~4000

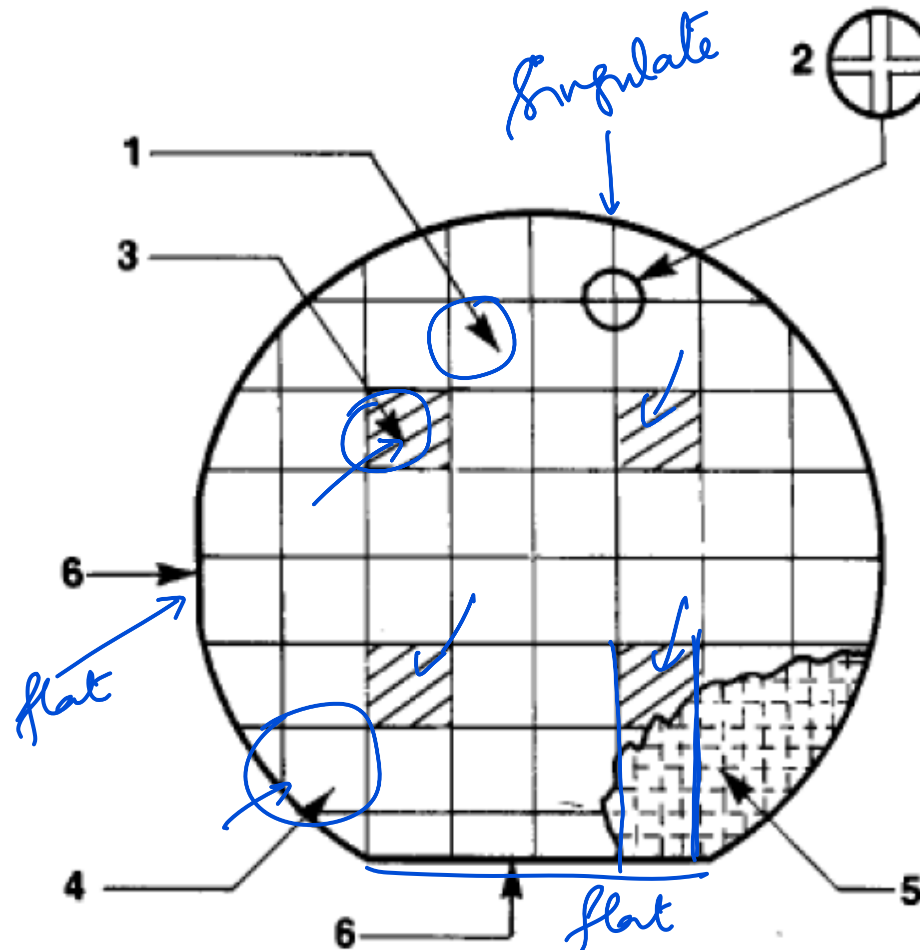
Making the Wafer



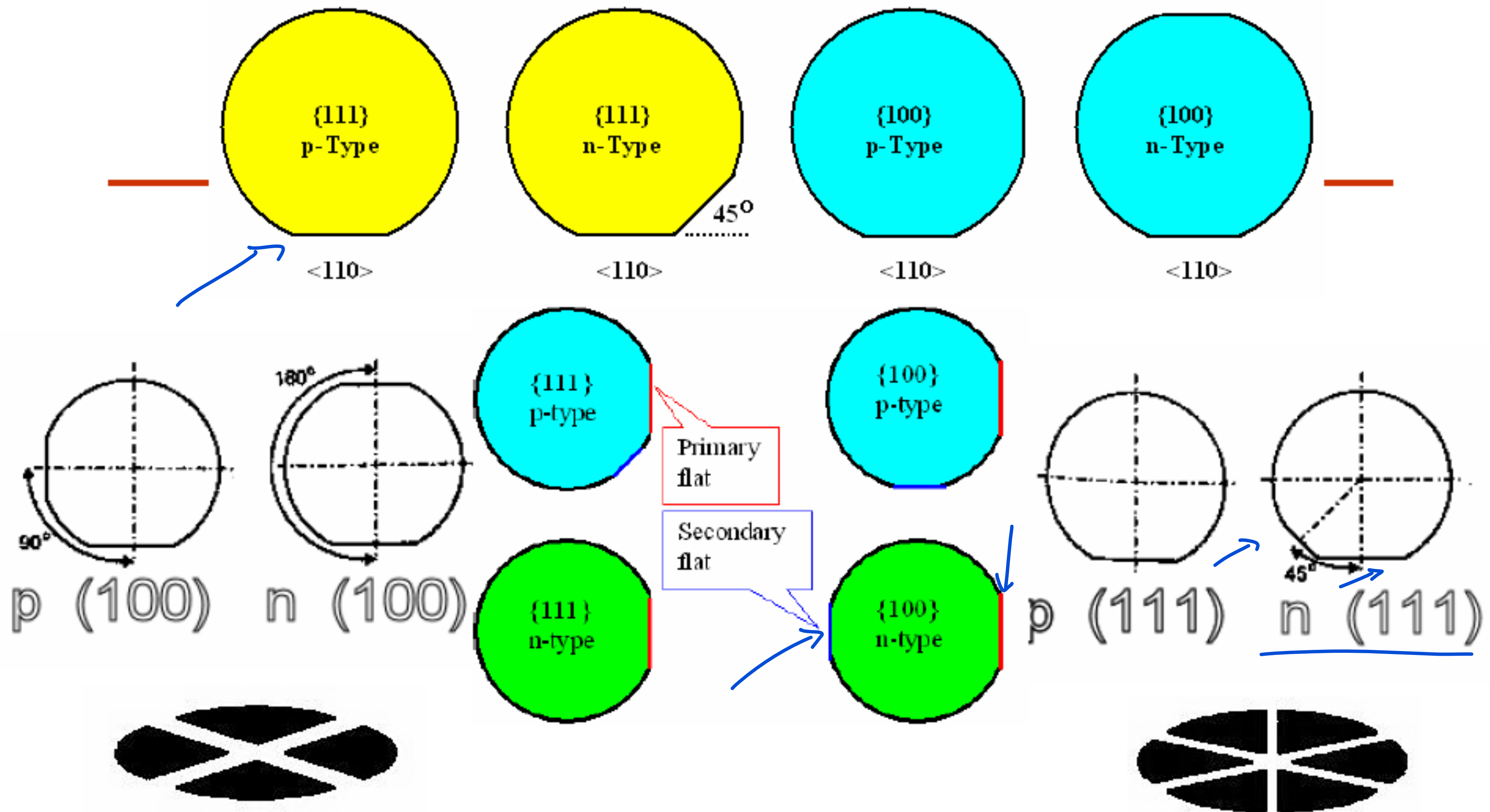
- A seed crystal is suspended in a molten bath of silicon
- It is slowly pulled up and grows into an ingot of silicon
- The ingot is removed and ground down to diameter
- The end is cut off, then thin silicon wafers are sawn off (sliced) and polished
- For example, in a 8” wafer about 500 devices/ chips can be accommodated by design. They are rectangular in shape
- Wafers are processed typically in batches of 25 (lot)

Wafer Terminology

1. Chip = Die = Microchip = Bar
2. Scribe Lines
3. Engineering Test Die
4. Edge Die
5. Crystal Planes
6. Wafer Flats



Source: Institute of Microelectronic Systems



Wafers have **flats**, and the flats told you two things:
The doping type of the wafer (**n-** or **p-**type)

The orientation of the wafer: **{100}** or **{111}**

Source: tf.uni-kiel.de

Wafer processing

- Wet cleans
- Photolithography
- Ion implantation (in which dopants are embedded in the wafer creating regions of increased (or decreased) conductivity)
- Dry etching
- Wet etching
- Plasma ashing
- Thermal treatments
  - Rapid thermal anneal
  - Furnace anneals
  - Thermal oxidation
- Chemical vapor deposition (CVD)
- Physical vapor deposition (PVD)
- Molecular beam epitaxy (MBE)
- Electrochemical Deposition (ECD). See Electroplating
- Chemical-mechanical planarization (CMP) (Polishing)
- Wafer testing (where the electrical performance is verified)
- Wafer backgrinding (to reduce the thickness of the wafer so the resulting chip can be put into a thin device like a smartcard or PCMCIA card.)

Source: Wikipedia

- Die preparation
  - Wafer mounting
  - Die cutting
- IC packaging
- Die attachment
  - IC Bonding
    - Wire bonding
    - Thermosonic Bonding
    - Flip chip
  - Tab bonding
- IC encapsulation
  - Baking
  - Plating
  - Laser marking
  - Trim and form
- IC testing

Plastic or **ceramic** packaging involves mounting the die, connecting the die pads to the pins on the package, and sealing the die.

Tiny wires are used to connect pads to the pins. In the old days, wires were attached by hand, but now purpose-built machines perform the task.

Traditionally, the wires to the chips were gold, leading to a "lead frame" (pronounced "leed frame") of copper, that had been plated with solder, a mixture of tin and lead. Lead is poisonous, so lead-free "lead frames" are now mandated by ROHS.

Source: Wikipedia

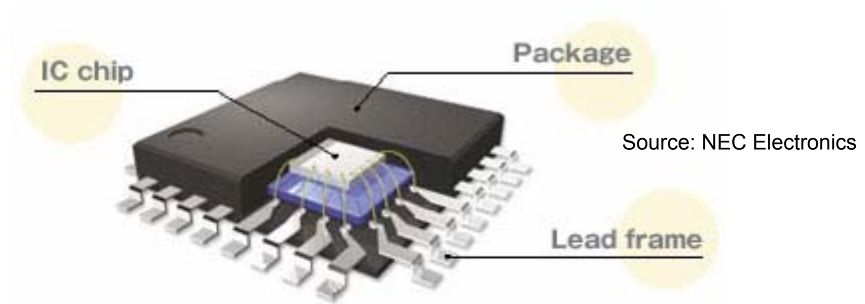
Semiconductor manufacturing processes

10 µm — 1971
3 µm — 1975
1.5 µm — 1982
1 µm — 1985
800 nm (0.80 µm) — 1989
600 nm (0.60 µm) — 1994
350 nm (0.35 µm) — 1995
250 nm (0.25 µm) — 1998
180 nm (0.18 µm) — 1999
130 nm (0.13 µm) — 2000
90 nm — 2002
65 nm — 2006
45 nm — 2008
32 nm — 2010
22 nm — approx. 2011
16 nm — approx. 2013
11 nm — approx. 2015

Wafer sizes are 300mm, 450mm

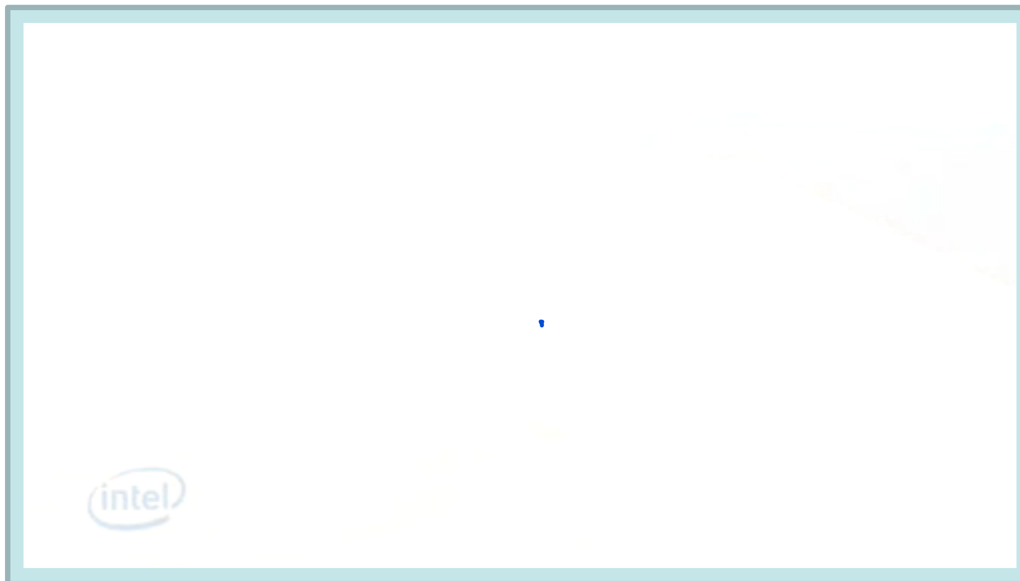
Source: Web

From Sand to Silicon to Wafer….
is an interesting process.



Source: NEC Electronics

Now, you will see a short video clip titled Sand-to-Silicon.
This video is reproduced with written permission from Intel



Source: INTEL