Review

Front-end processing

Wafer
Die

Sand to Silicon (purity)
Silicon to Wafer (Silicon)
sizes (dia) thickness

Clean Room
32 nm
22 nm
11 nm

Wafer Ingot
Slicing

Photoresist (PR)
— types

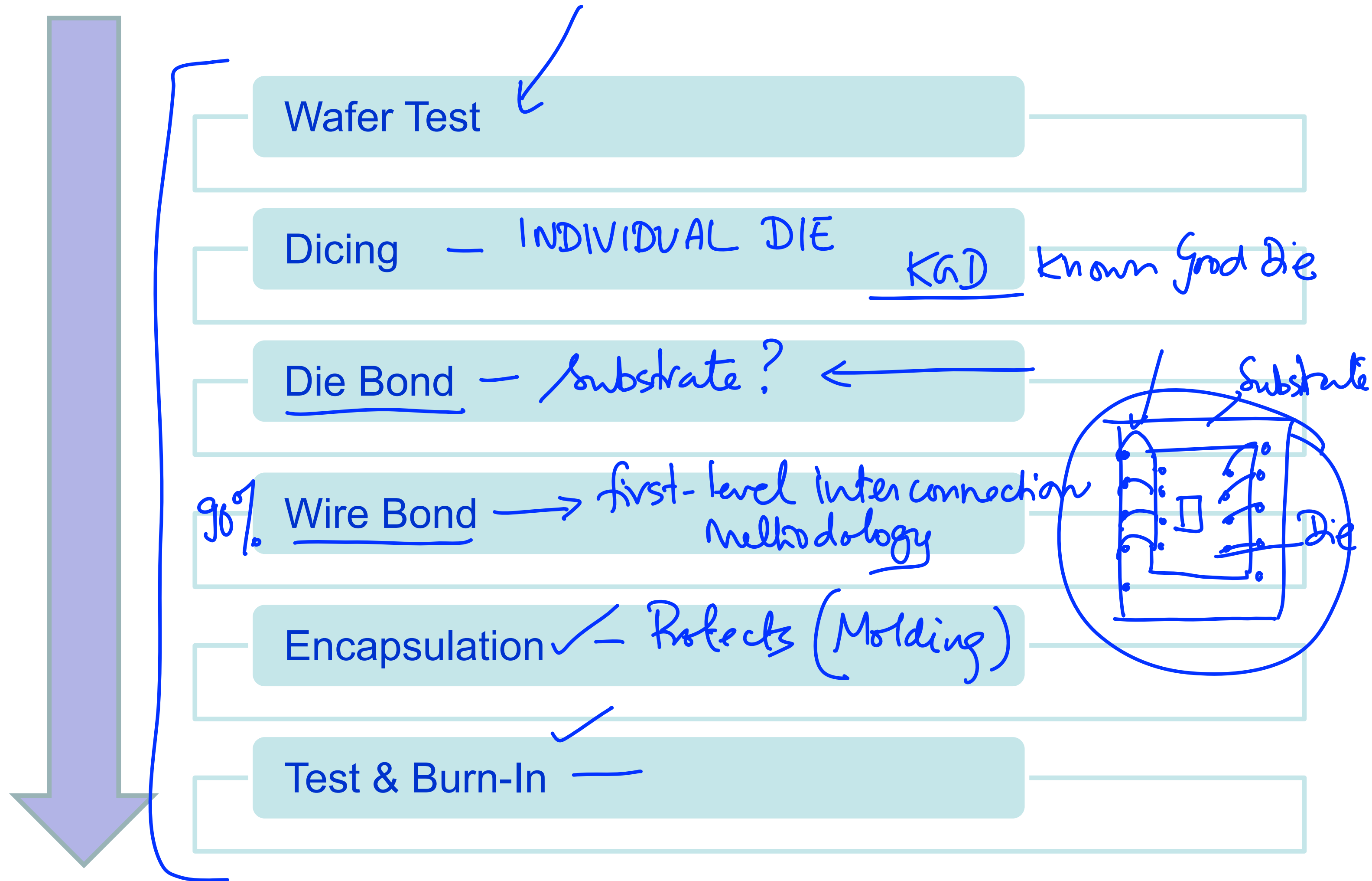
UV exposure
(photolithography)
(MASK)

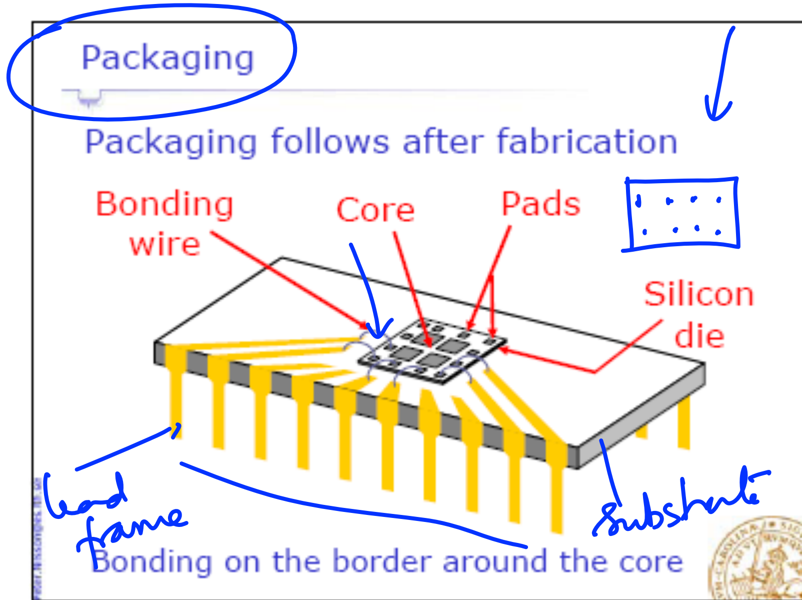
Developing
PR Strippers
Etching — types
wet resist
dry etching
Deposition
— Electroplating

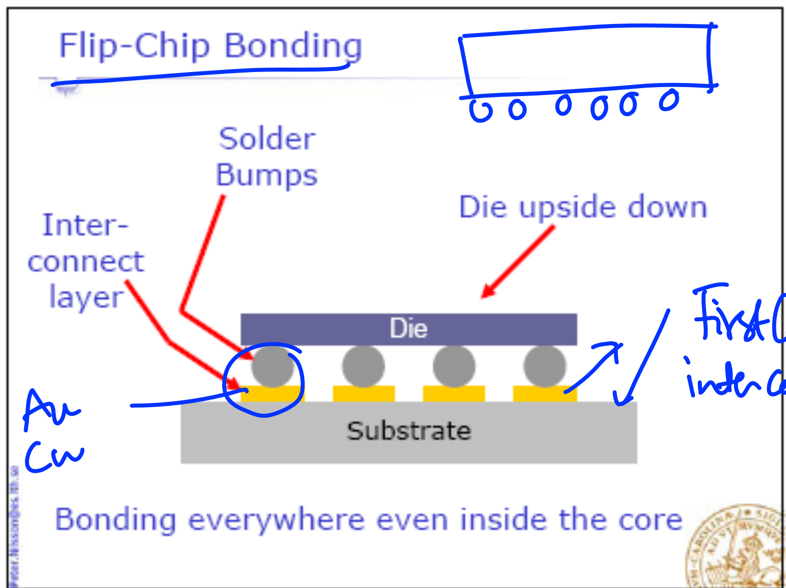
TESTING

Test, Assembly & Packaging :Back-end

Materials management, Chemical Distribution, Automation, CIM

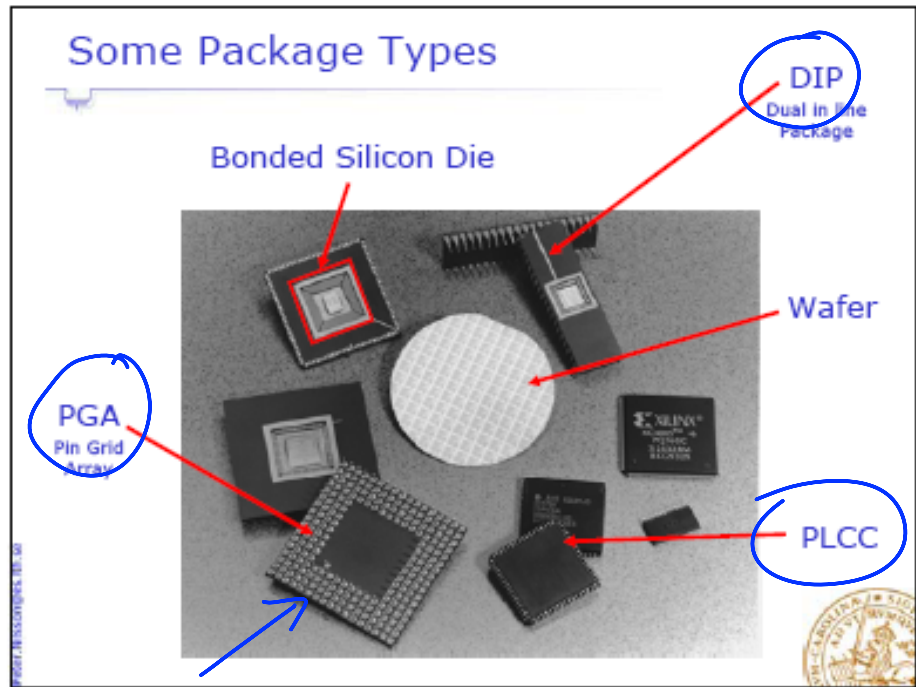






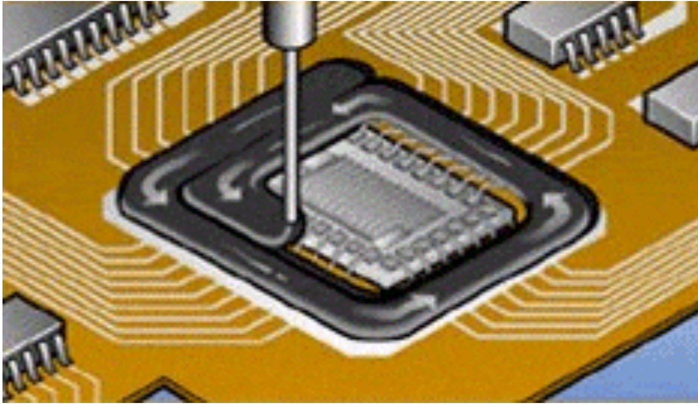
TAB
Tape Automated Bonding

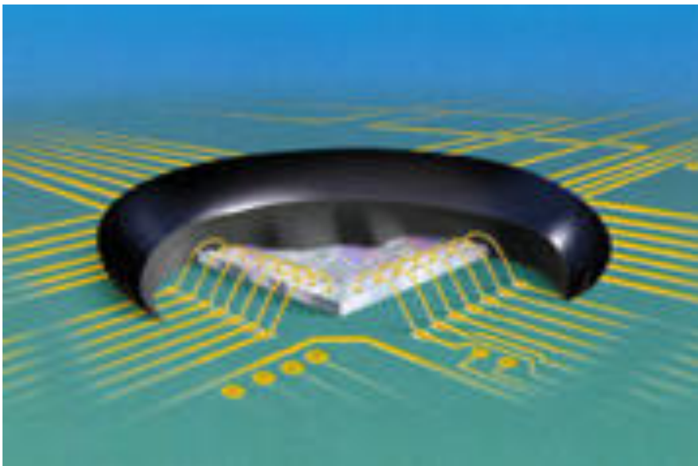
BGA
CSP

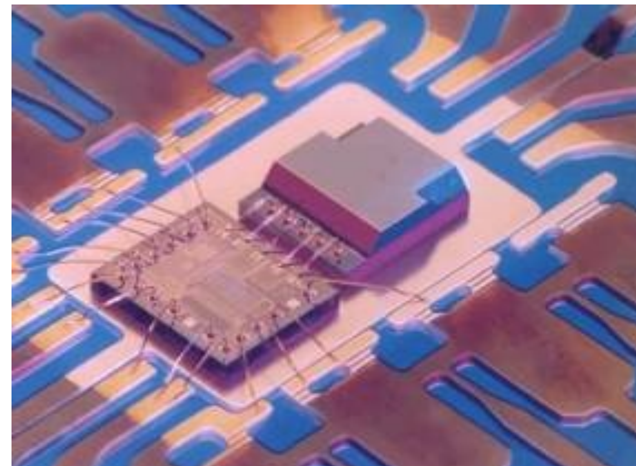


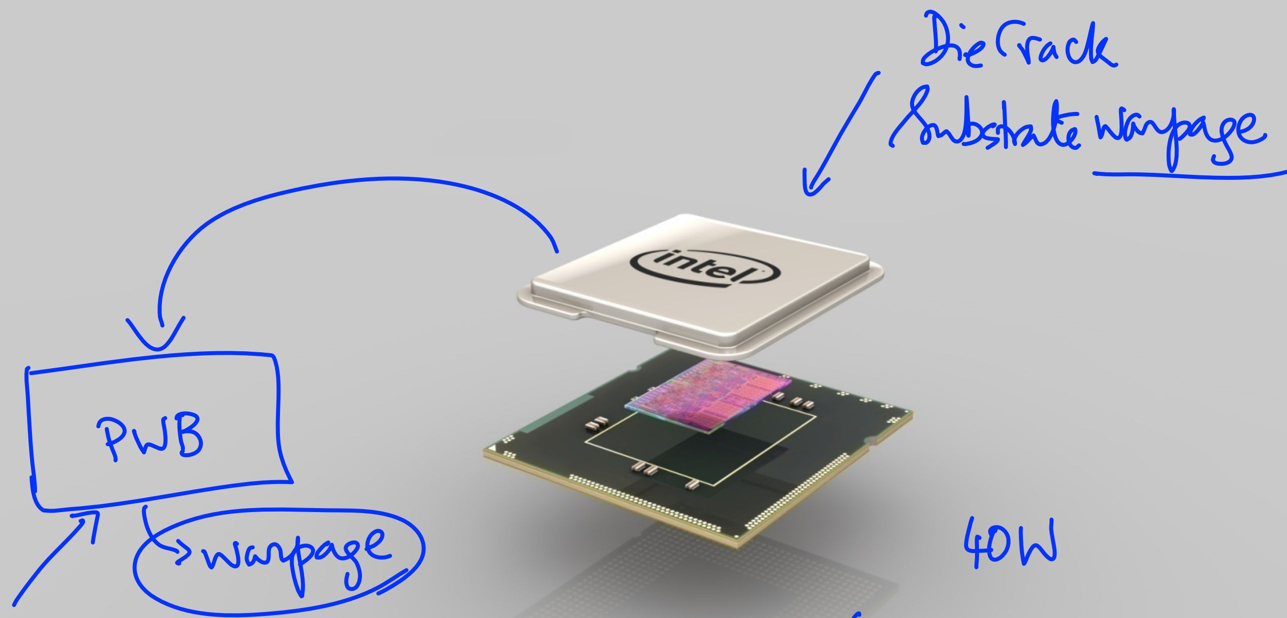
Source: Peter Nilsson, LTH, Sweden

Encapsulation and Decoupling





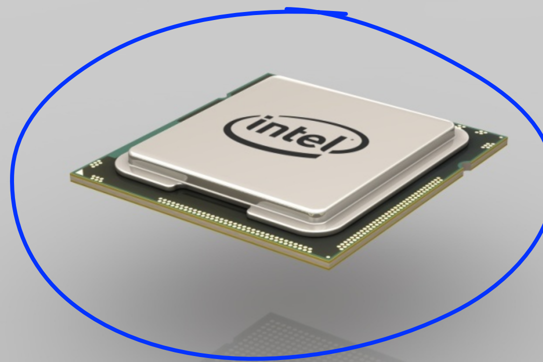




Packaging

The substrate, the die and the heat spreader are put together to form a completed processor. The green substrate builds the electrical and mechanical interface for the processor to interact with the rest of the PC system. The silver heat spreader is a thermal interface where a cooling solution will be put on to. This will keep the processor cool during operation.

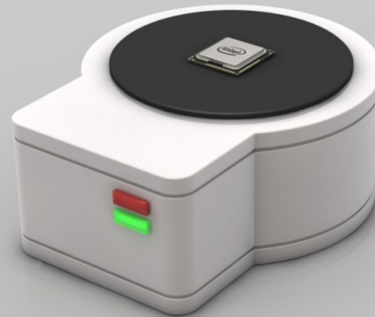
Source: INTEL



Processor

Completed processor (Intel® Core™ i7 Processor in this case). A microprocessor is the most complex manufactured product on earth. In fact, it takes hundreds of steps –only the most important ones have been visualized in this picture story -in the world's cleanest environment (a microprocessor fab) to make microprocessors.

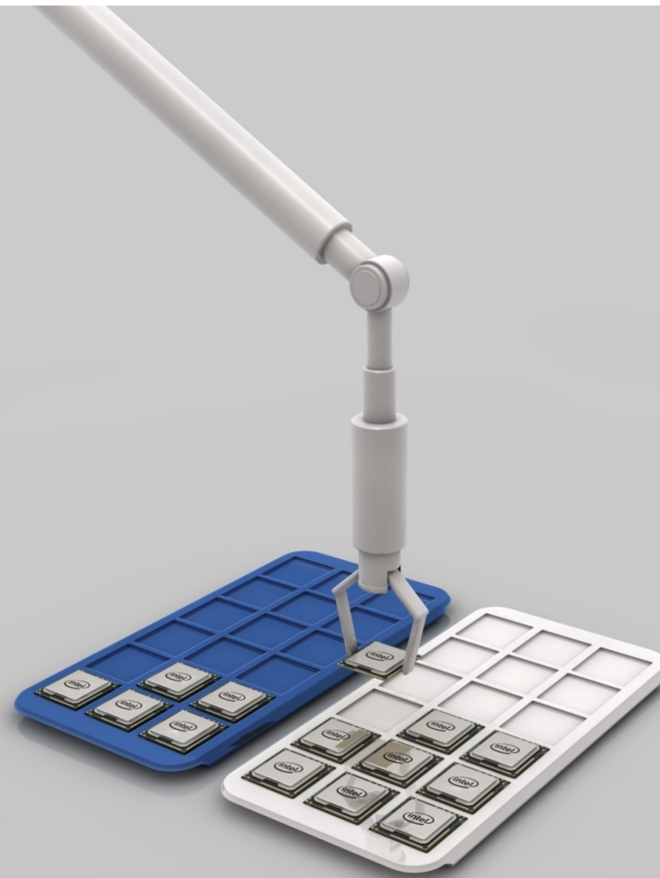
Source: INTEL



Class Testing

During this final test the processors will be tested for their key characteristics (among the tested characteristics are power dissipation and maximum frequency).

Source: INTEL



Binning
Based on the test result of class testing processors with the same capabilities are put into the same transporting trays.

Source: INTEL

Retail Package

The readily manufactured and tested processors (again Intel® Core™ i7 Processor is shown here) either go to system manufacturers in trays or into retail stores in a box such as that shown here.

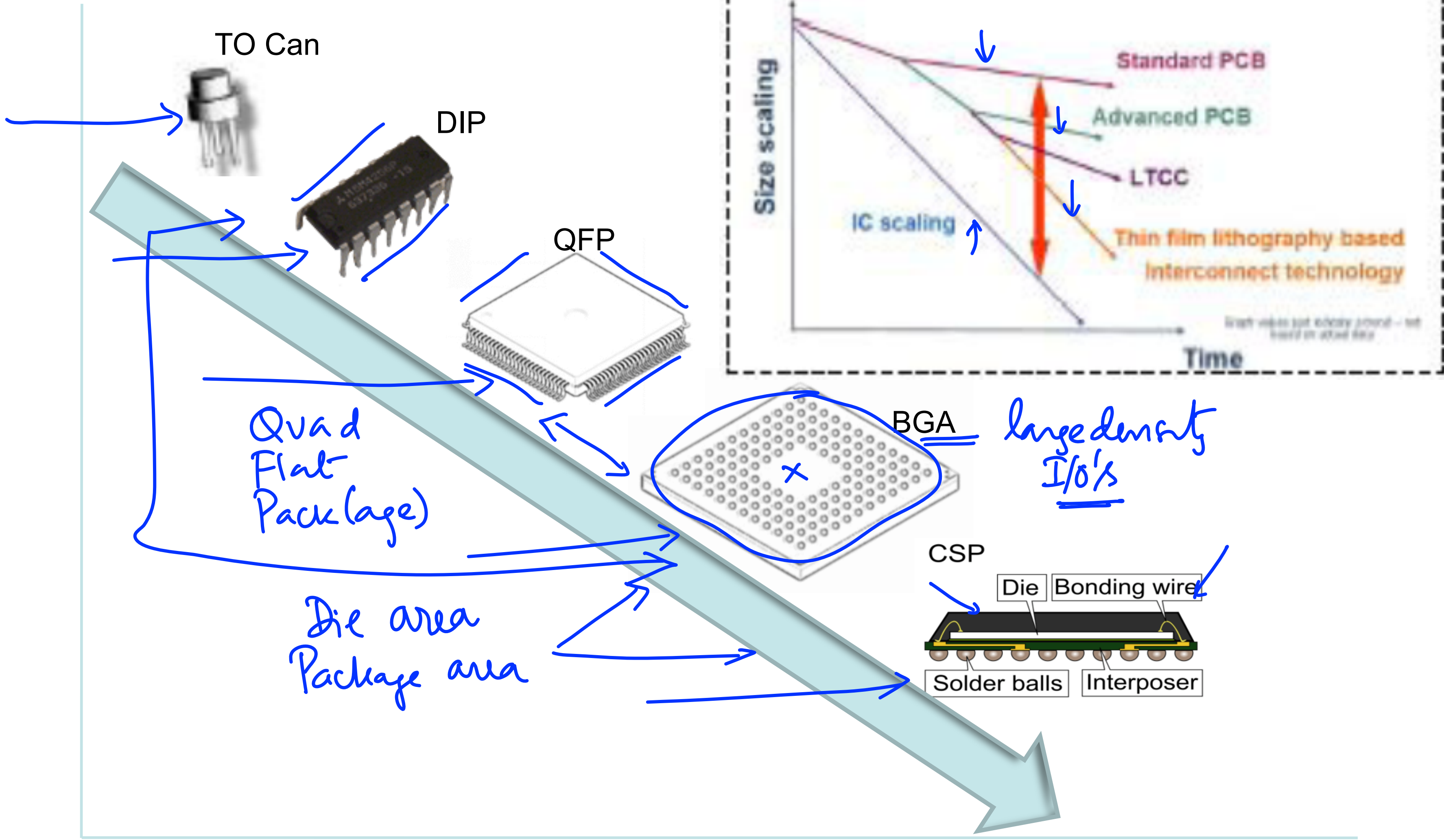
Source: INTEL

You can also visit the following websites for very informative videos on semiconductor manufacturing:

www.siliconrun.com

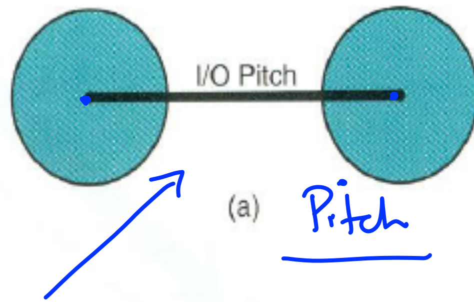
www.nec.com

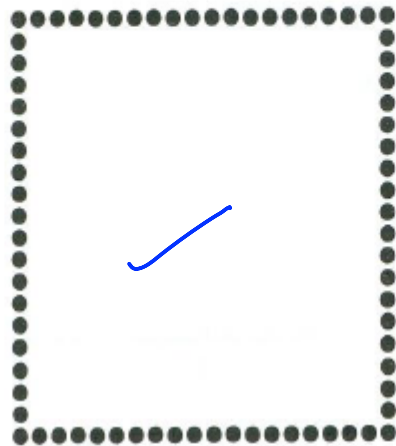
PACKAGING EVOLUTION HAS BEEN SLOWER COMPARED TO SEMICONDUCTOR EVOLUTION

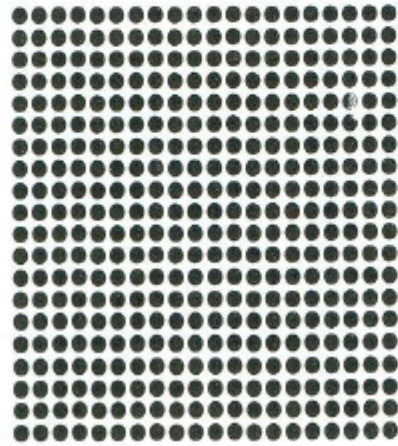


Time and Packaging Efficiency

Source: Wikimedia Commons







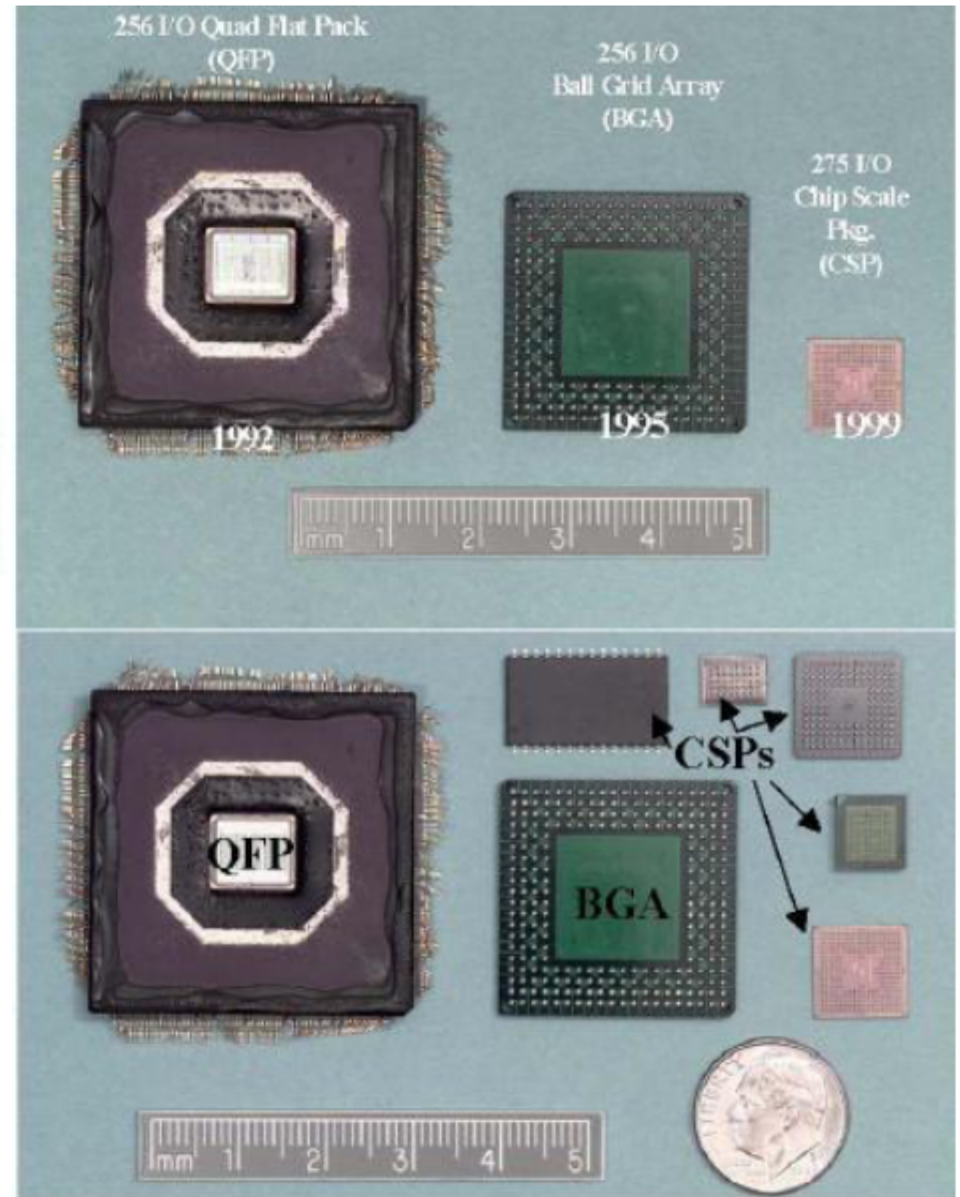
Peripheral

20mm Size, 0.5mm Pitch
total I/O = 160

Area

20mm Size, 0.5mm Pitch
Total I/O = 1600

(b)



Peripheral to Area Array: Another Packaging Example to increase density

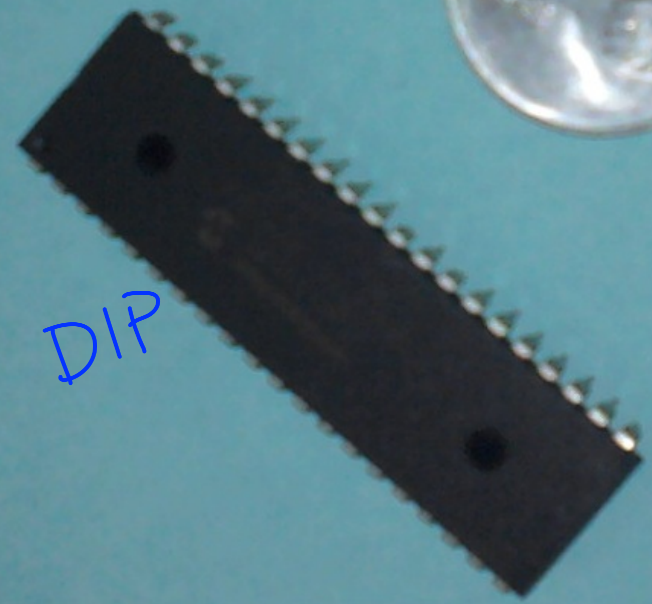
Picture Source: NASA

TopLine™
QFP128T30-3.2
QFP

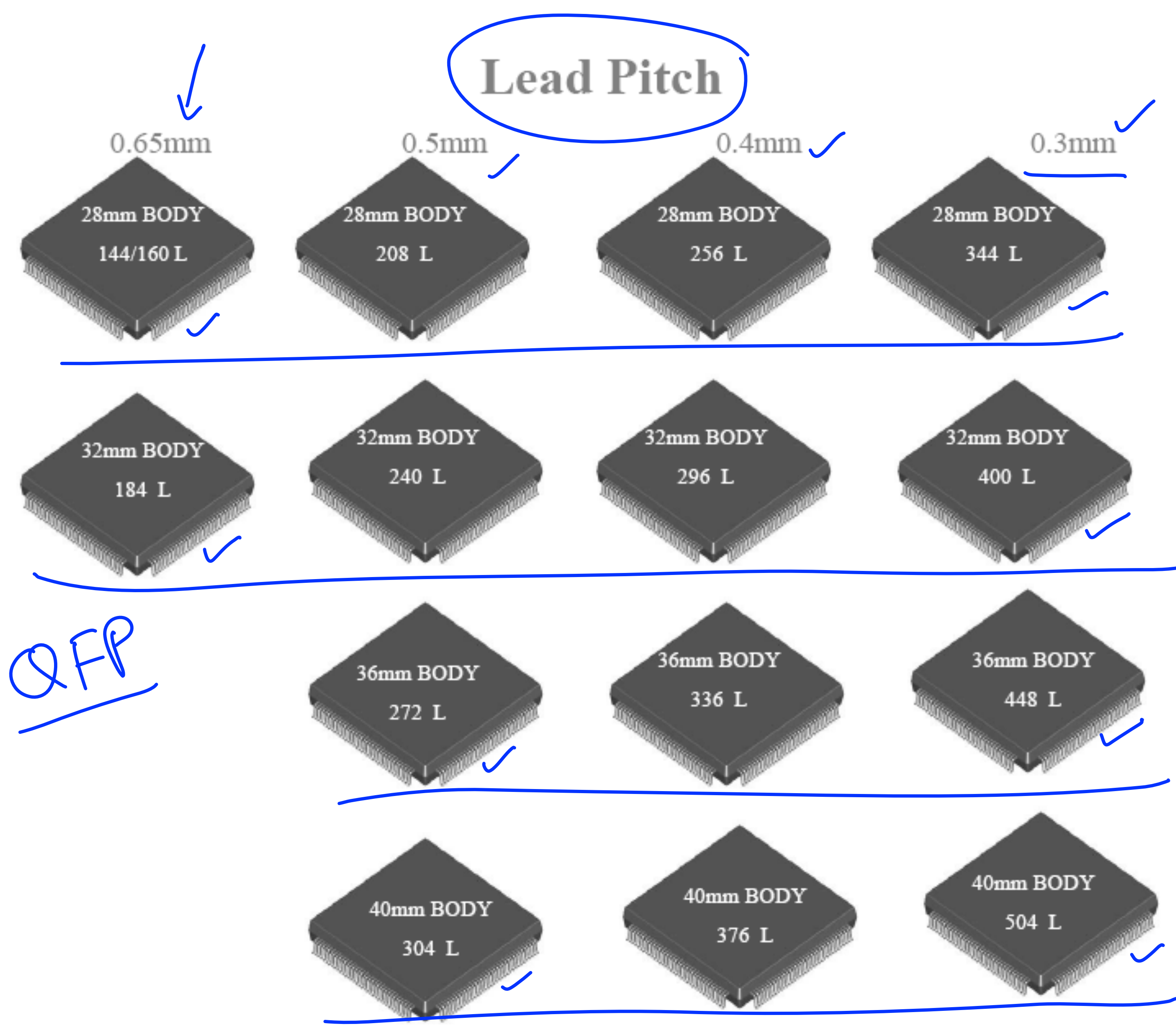
Bare Die

CSP

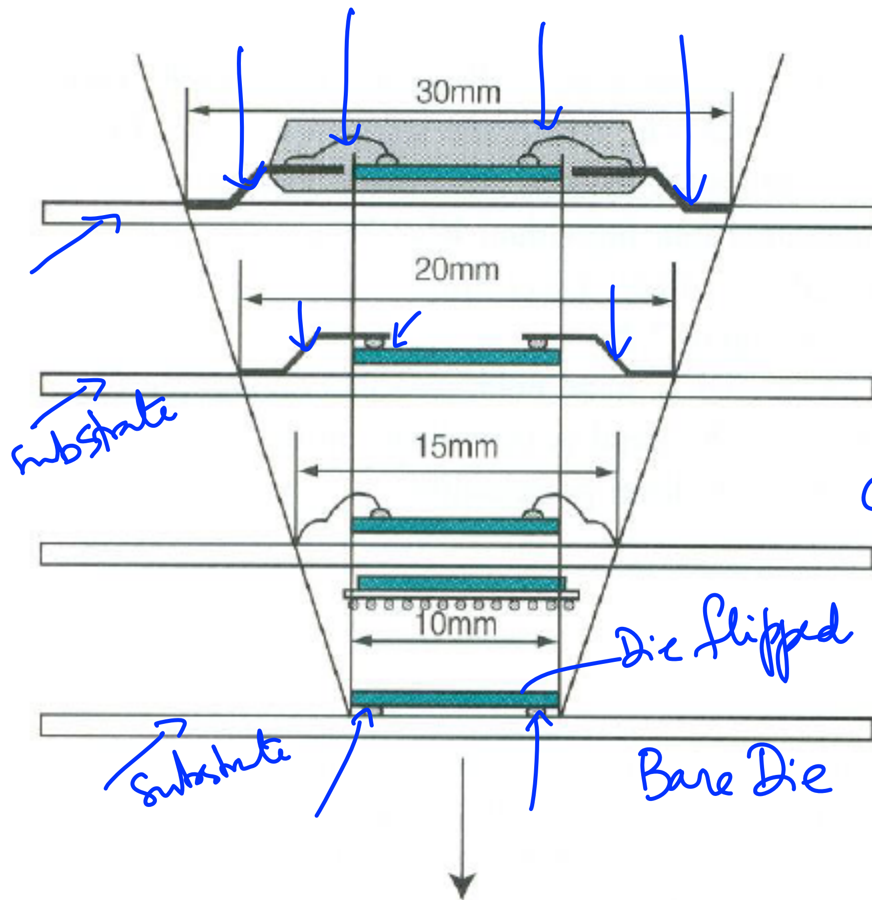
CSP


DIP

BGA



Small Form Factor: A Packaging Example with QFPs



Wafer-level packaging as the future trend.

Example

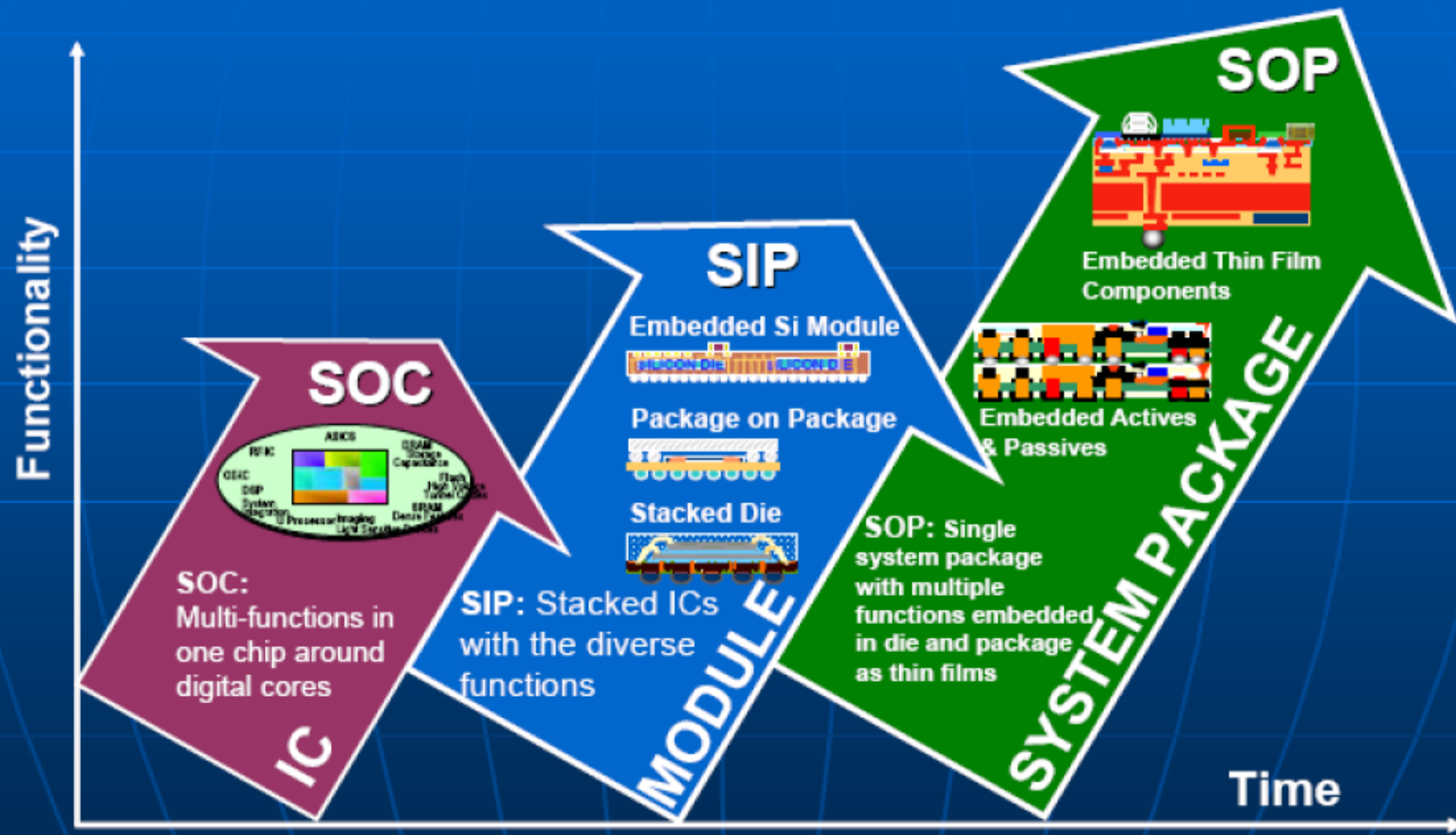
Type	Area	
QFP	900 mm²	100%
TAB	400 mm²	44%
COB	225 mm²	25%
CSP	115 mm²	13%
Flip Chip	100 mm²	11%

Wafer Level Flip Chip or CSP

From QFP to flip chip:

Savings in real estate and increase in density, performance

SOC, SIP & SOP: Complementary



Source: TI and
Prof Rao Tummala, GTech

Chip level interconnections

- 1 st level interconnection

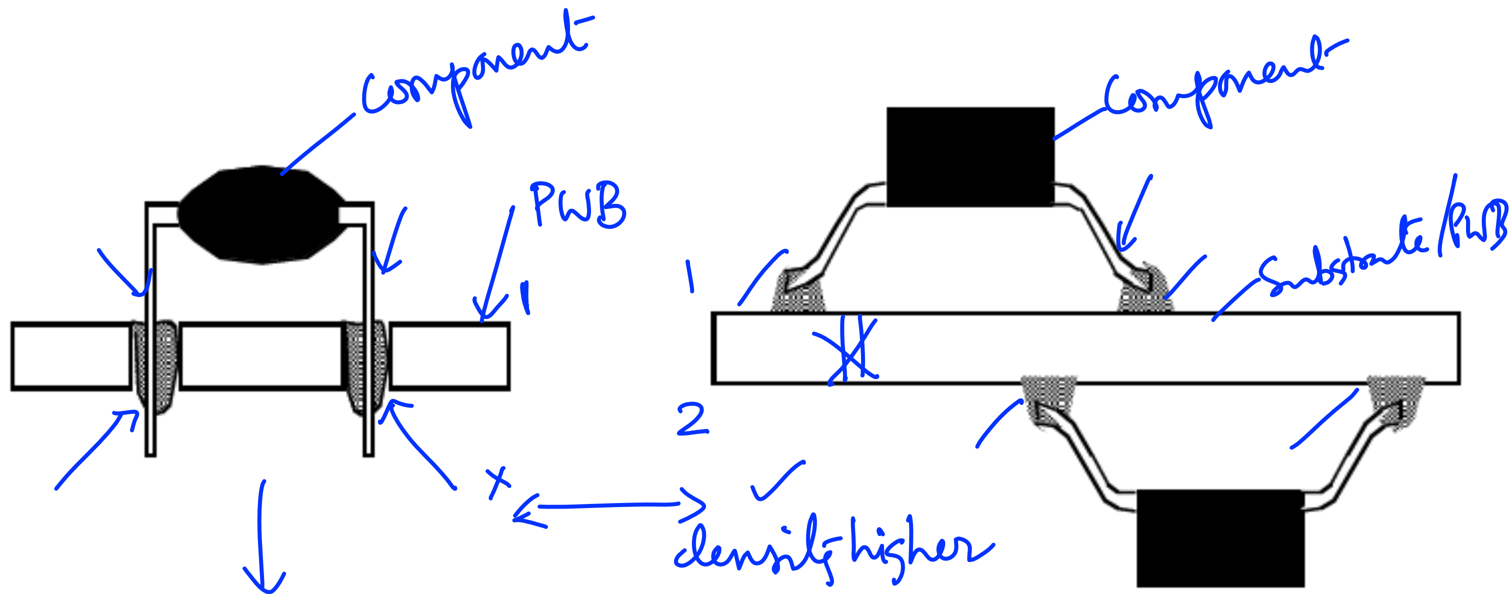
  -Connection of die to the package

  (single or multichip; SCM or MCM)

- 2 nd level interconnection

  -Connection of the package to the PWB

Package-to-Board Interconnect



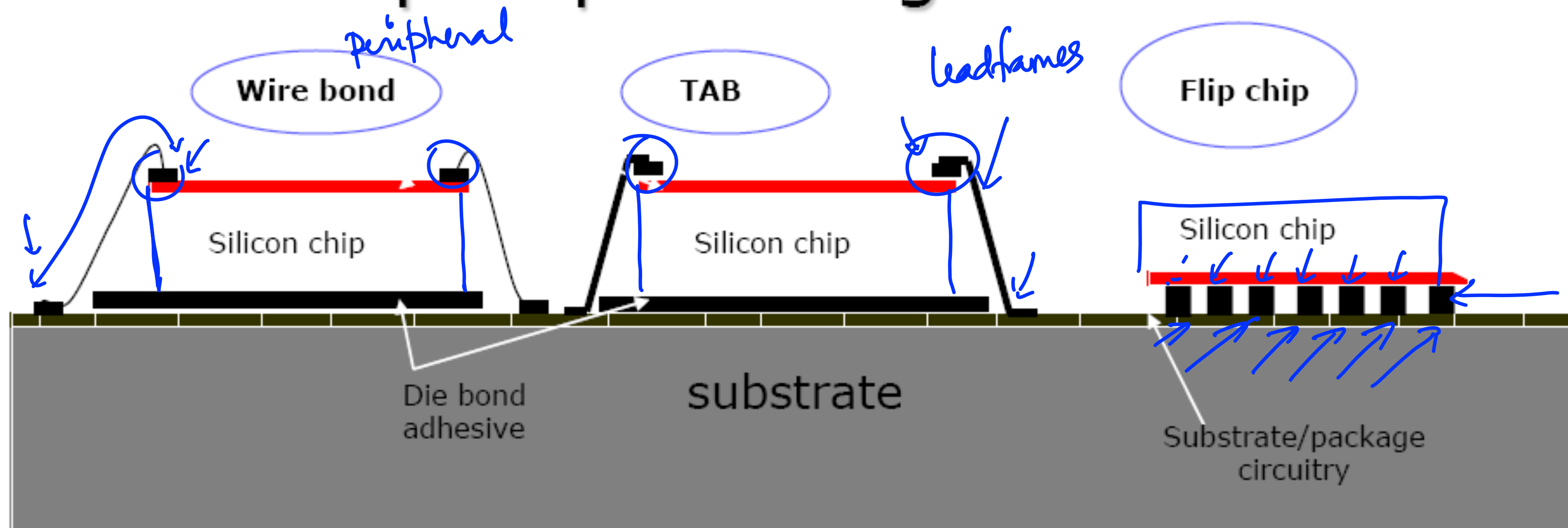
(a) Through-Hole Mounting

(b) Surface Mount

- Plated through hole Technology (PTH or THT)
  -Leaded components require through hole
- Surface Mount Technology (SMT)
  -Leaded components mounted on surface
  -Direct chip attach like flip chip (DCA)
  -Chip on Board (COB) using wirebonding
  -Solder ball based connection like BGA, CSP

Common 1st level interconnections

1. Wire bonding
2. Tape automated bonding
3. Flip chip bonding



Wirebond | TAB | Flip Chip

Wire
Pad
Epoxy
Active face
Adhesive
CHIP
Inner Lead Bond Encapsulation
TAB Beam Lead
CHIP
Active Face
Bumps
Underfill
CHIP
CHIP CARRIER

Two options:

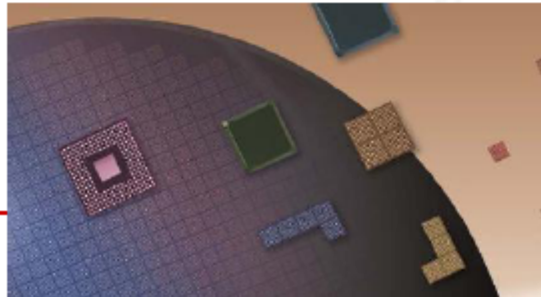
- Ball bonding
- Wedge bonding

Two options:

- Face up chip
- Face down chip

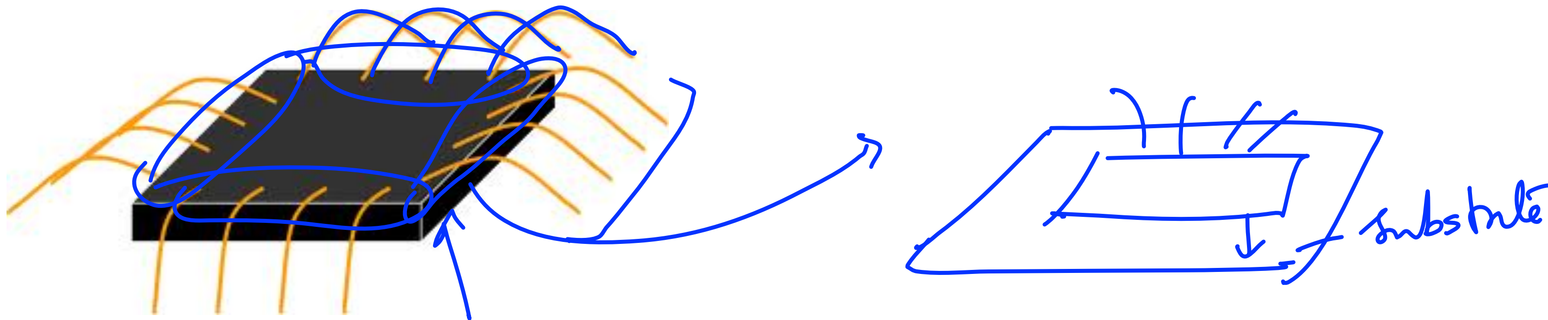
Three options:

- Metallurgical bond
- Metallurgical and adhesive bond
- Adhesive bond



Chip to package connection

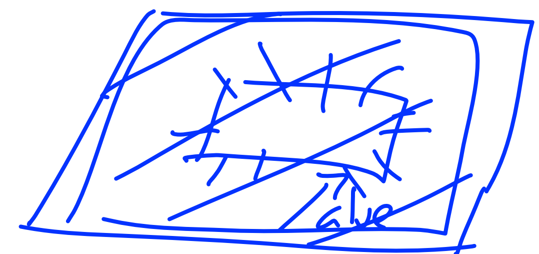
- Wire bonding
  - Only periphery of chip available for IO connections
  - Mechanical bonding of one pin at a time (sequential)
  - Cooling from back of chip
  - High inductance (~1nH)

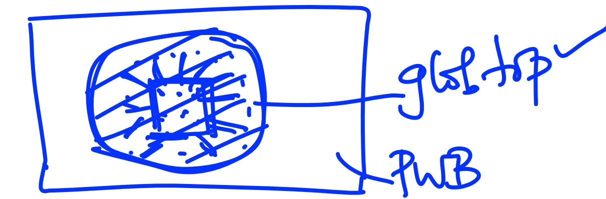


Picture Source: Palomar Technologies

Wirebond Attachment

- Used in Lead Frame, PGA and BGA packaging
- Over 80% of Packages are Wire bonded
- Epoxy Glue to Attach Chip
- Typically Gold Wire
  - Also Copper, Aluminum
  - Wire length- typ. 1-5 mm
  - Wire diam.- typ. 25-35 μm
  - Inexpensive, Reliable





- Molding or Encapsulation done with epoxy resin
- Chip-on-Board involves glob top to bare die with epoxy resin