REVIEW

1st level interconnections
- wire bond
- TAB
- Flip chip

Pitch

TO can → CSP, WLP, new formats, lower sizes of packages, more I/O's

Package density

TO can
↓
DIP
↓
QFP
↓
PGA
↓
BGA
↓
CSP

EPOXY Resin

organic

- molding
- protech
- encapsulation

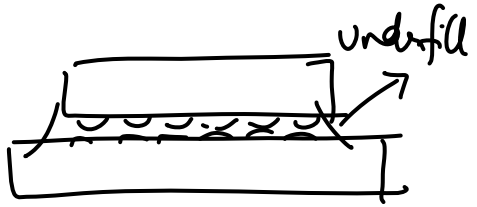
epoxide

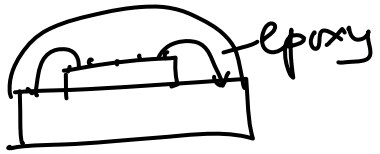
EPOXY

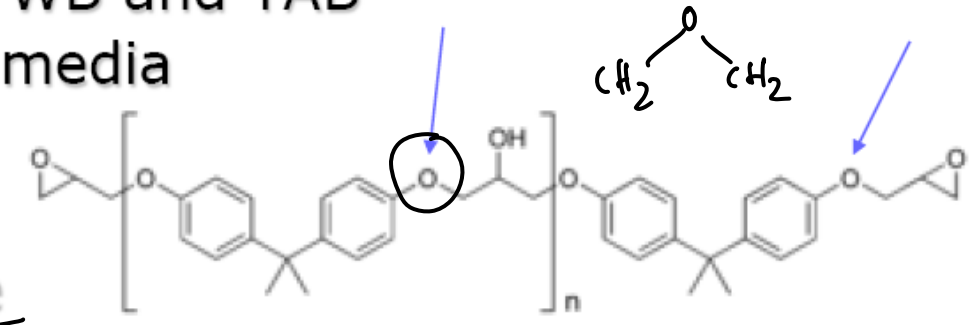
EPOXIES

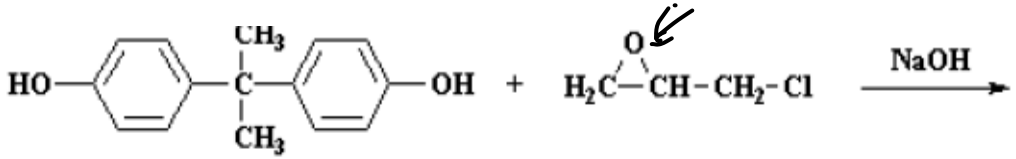
Epoxy resin

- Molding Compound; Potting samples
- Package encapsulation
- Underfill media
- Photoimageable solder mask media
- PWB substrate (resin)
- Conformal coating
- COB glob top media- WB and TAB
- Conductive adhesive media
- Solder paste media
  - And so on…
- Epoxy or Polyepoxide
- Thermosetting polymer (curing with hardener)
- Typical epoxy resin is from Bisphenol A and Epichlorohydrin
- Ciba, DuPont, Shell etc..



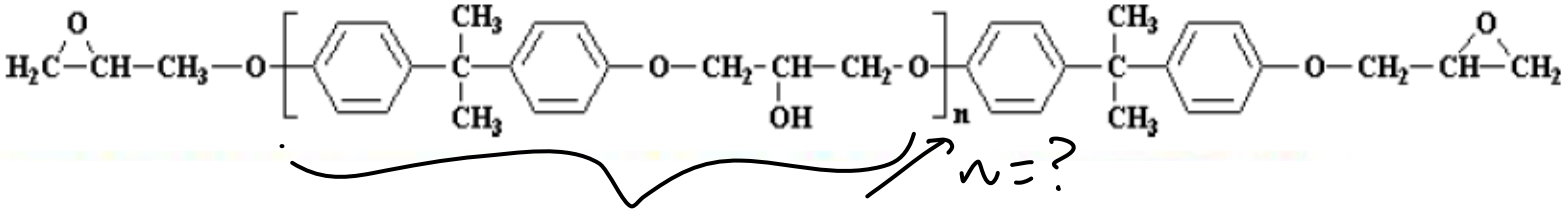




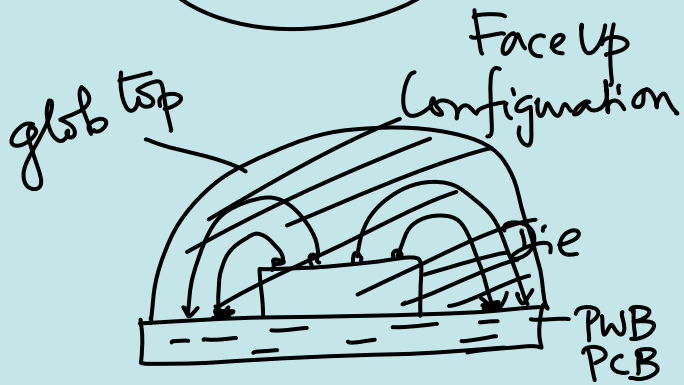


bisphenol A

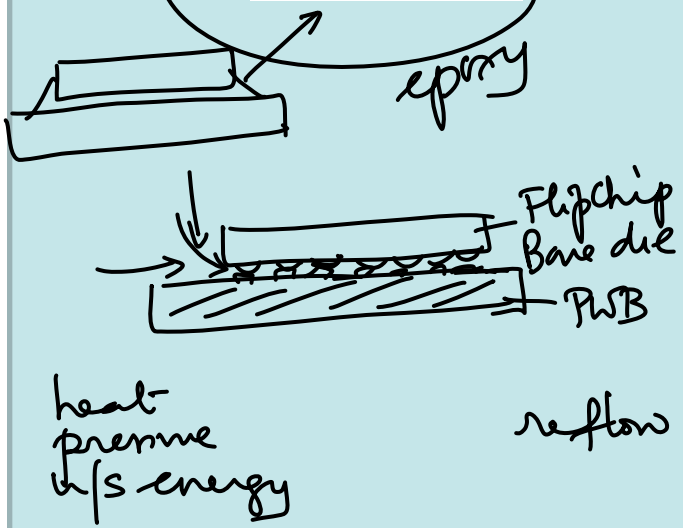
epichlorhydrin



GLOB TOP

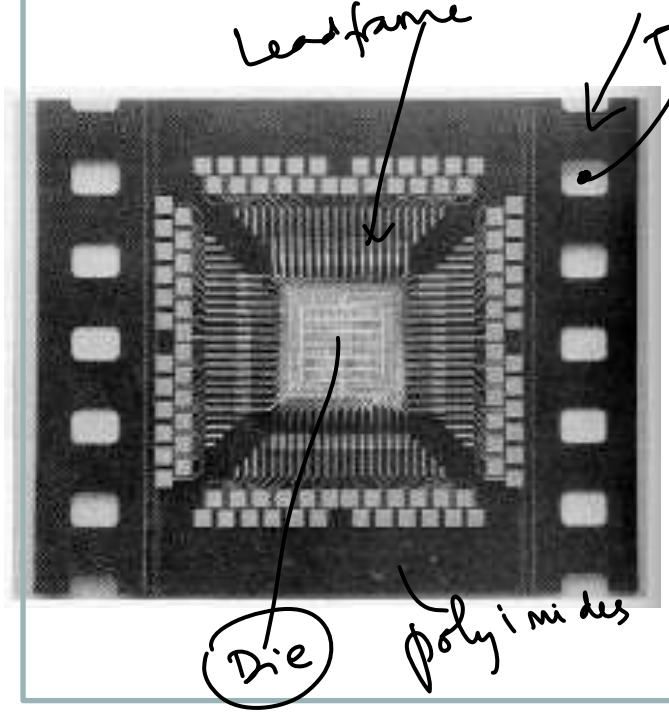


UNDERFILL

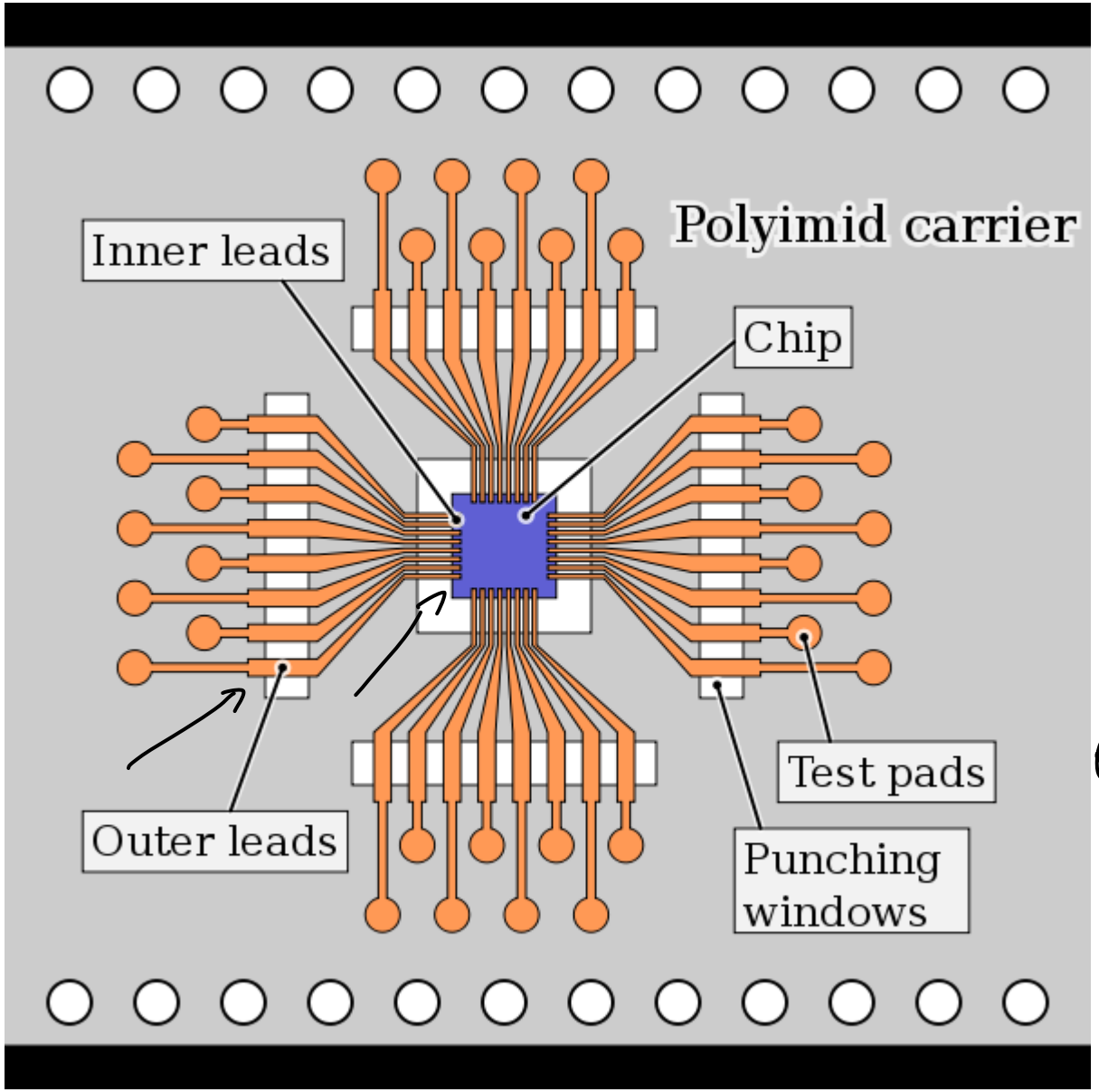


TAB (Tape Automated Bonding)

- Interconnect Patterned On Tape
- Stronger Lead Bonding Strength
- Supports Smaller On-chip Pin Size and Pitch
- Supports upto 850 pins
- Better Electrical Performance than Wire bonds



TAB is an approach to fine the pitch interconnection of a chip to a lead frame. The interconnections are patterned on a multi layer polymer tape. The tape is positioned above the 'bare die' so that the metal tracks (on the polymer tape) correspond to the bonding sites on the die. Welding is done by thermo-compression bonding.



Source: Wikimedia Commons

Where is TAB used?

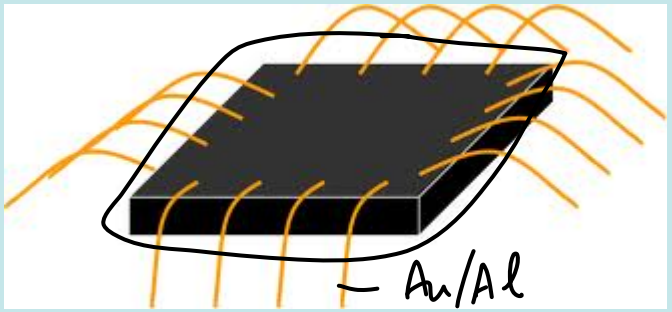
- Smart cards
- phone cards
- ID/RF cards
- pocket calculators
- digital radios

Inner lead Bonding
Outer lead Bonding

Flip-Chip (C4) Attachment

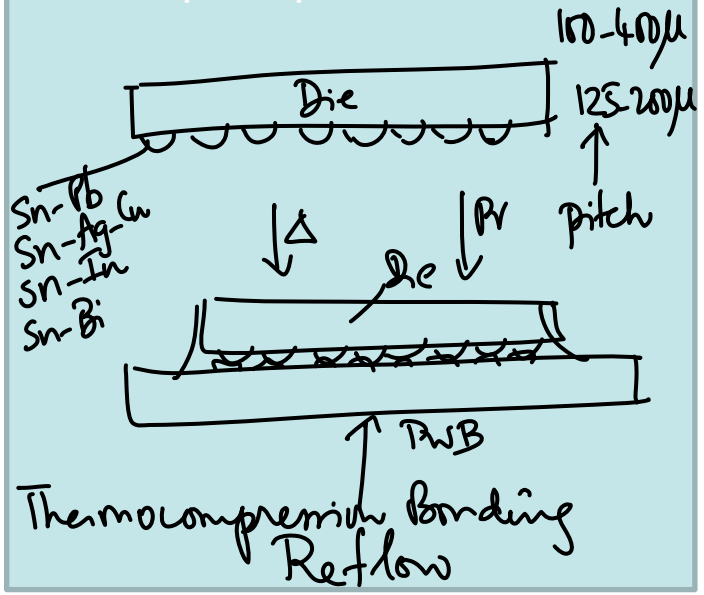
- What is Flip-Chip?
  - A method to electrically connect the die to the package carrier
  - The bond wire is replaced with a conductive "bump" placed directly on the die surface
    - Under-fill epoxy is used to secure the attachment and absorb stress
  - The chip is then "flipped" face down onto the package carrier using a re-flow process
  - Bump sizes range from 90-125 microns in diameter
  - Also known as C4 (Controlled Collapsible Chip Connection)
    - Invented by IBM in 1963

Wire bonding



Picture Source: Palomar Technologies

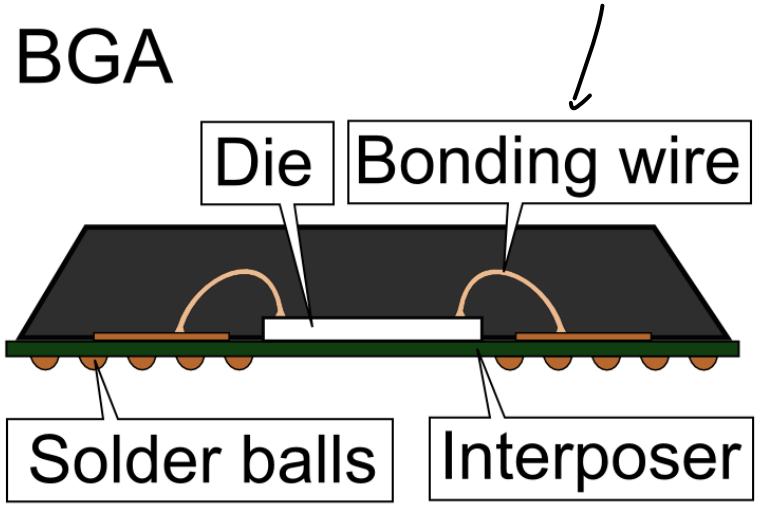
Flip Chip attachment

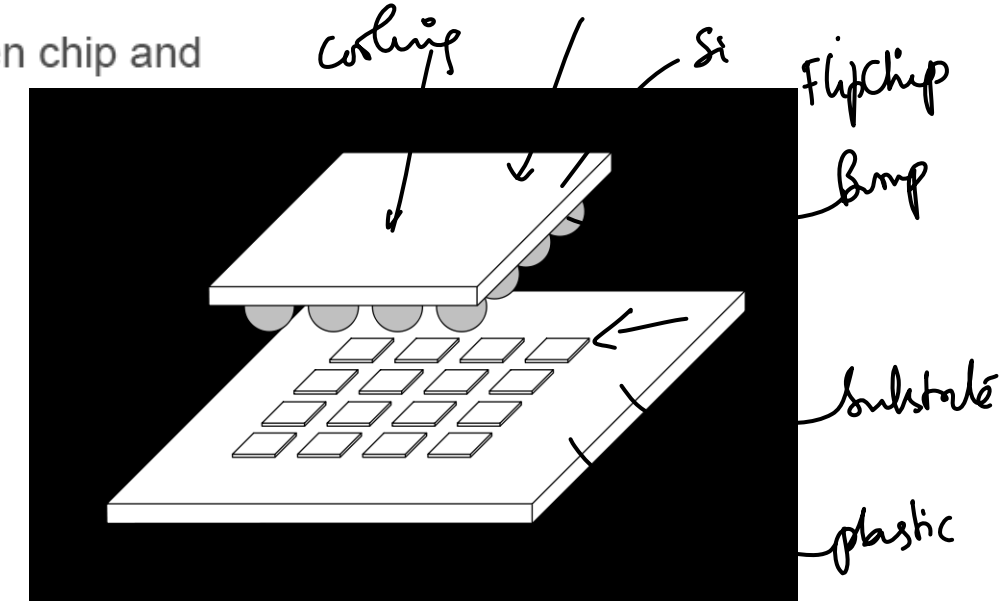


- Flip-chip
  - Whole chip area available for IO connections
  - Automatic alignment
  - One step process (parallel)
  - Cooling via balls (front) and back if required
  - Thermal matching between chip and substrate required
  - Low inductance (~0.1nH)

Flip chip Use:
- COB
- BGA packages
- CSP packages

Yields are high





Source: Wikimedia Commons

Flip Chip

- **Flip-Chip is :**
  - **NOT a Specific Substrate material**
  - **NOT a Specific Package like SOIC**
  - **NOT a Specific Package Type like QFP, BGA or PGA**
  - **Can be mounted on organic and ceramic substrates; in other words- at board level too**

→ COB

Where is FC used?

→ digital cameras
→ Camcorders
→ laptop
→ Comm/handheld products

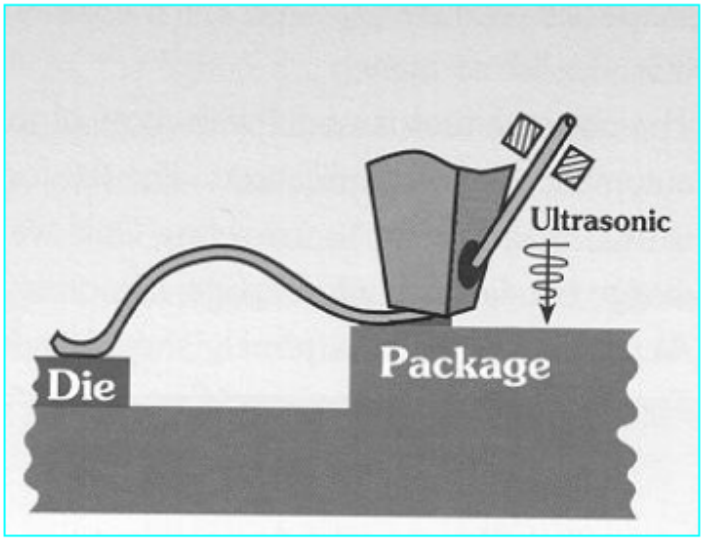
Summary of first level connection choices
Next up: Description of Wirebonding, TAB and C4 processes

WB
TAB
C4

Wire Bonding

Used in interconnecting the Die to various substrates

...the most popular interconnection method



Wire bonding is a **SOLID phase welding process** where the two metallic materials, **a thin wire** and the metallization on **pad surface** are brought into intimate contact under a **combination of heat, pressure, and/or ultrasonic energy...**

Wire bonding - Types

Wire bonding is made using two types of tools:

Tool

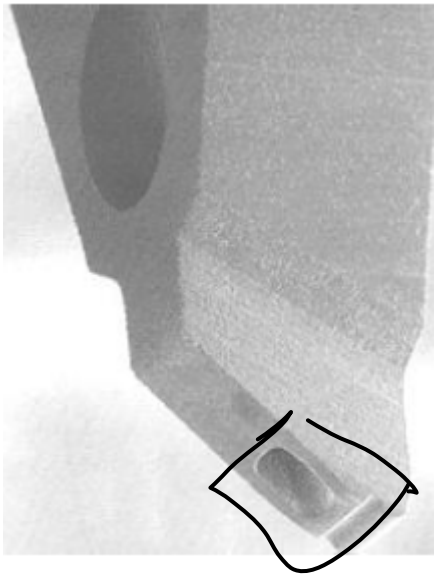
a. Wedge – Called **wedge bonding**
b. Capillary – Called **ball bonding**

Very inexpensive- A penny per pin!

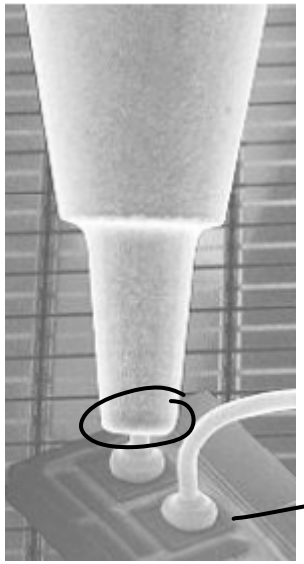
Progress in IC packaging is essentially due to technology improvements in WIRE BONDING

Bonding Tools

- Wedge



- Capillary



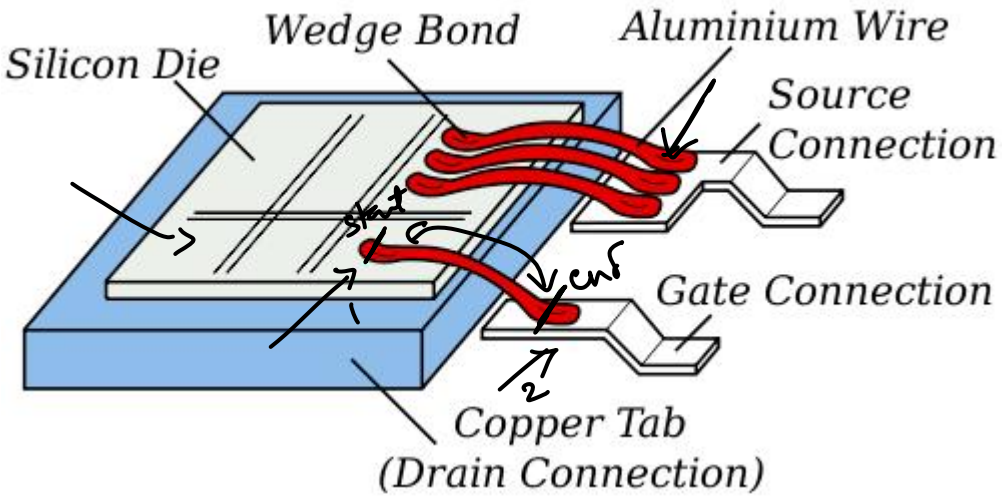
- Thermocompression
- Ultrasonic
- Thermosonic Δ/U/S

Al is more suited for wedge bonding

Process Steps

Al

- Wedge tool loaded with wire
- Apply pressure and ultrasonic energy to form wedge (chip)
- Bonding on substrate pad
- Loop formation
- Package bond pad formation
- Wire break-off to finish process



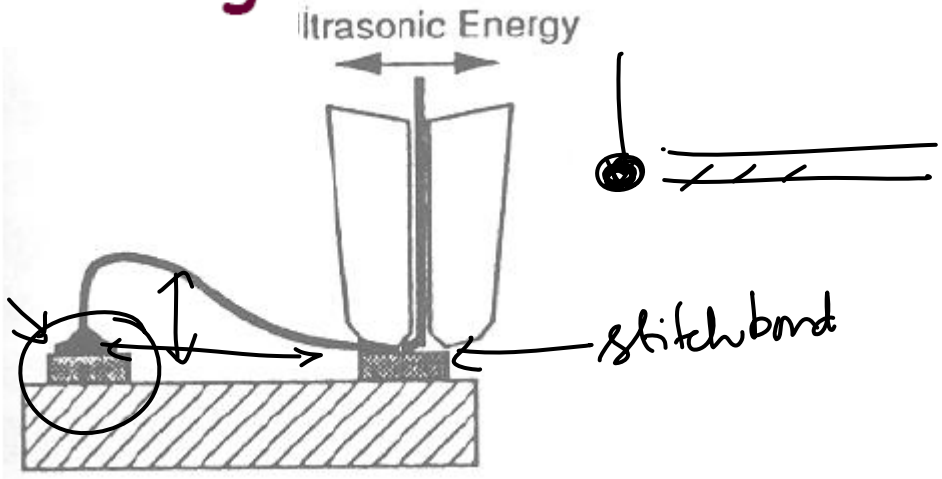
Source: Wikimedia Commons

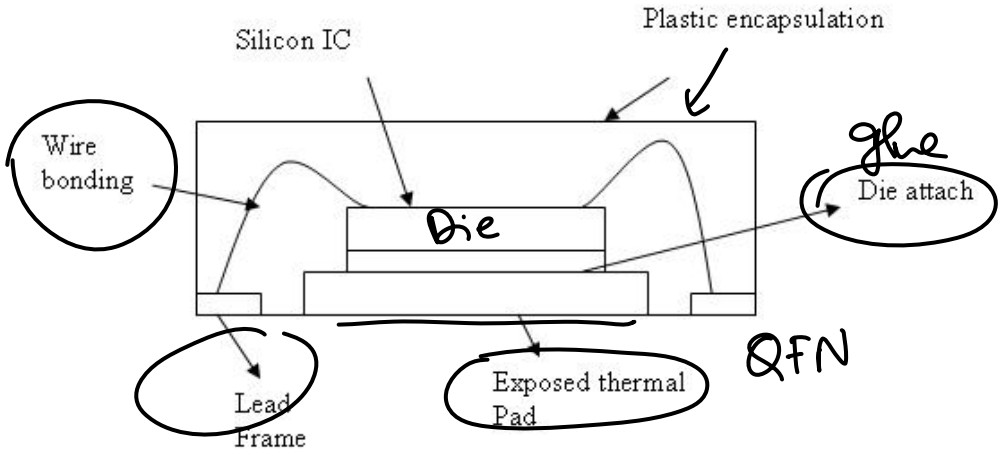
Ball bonding

Process Steps

Gold

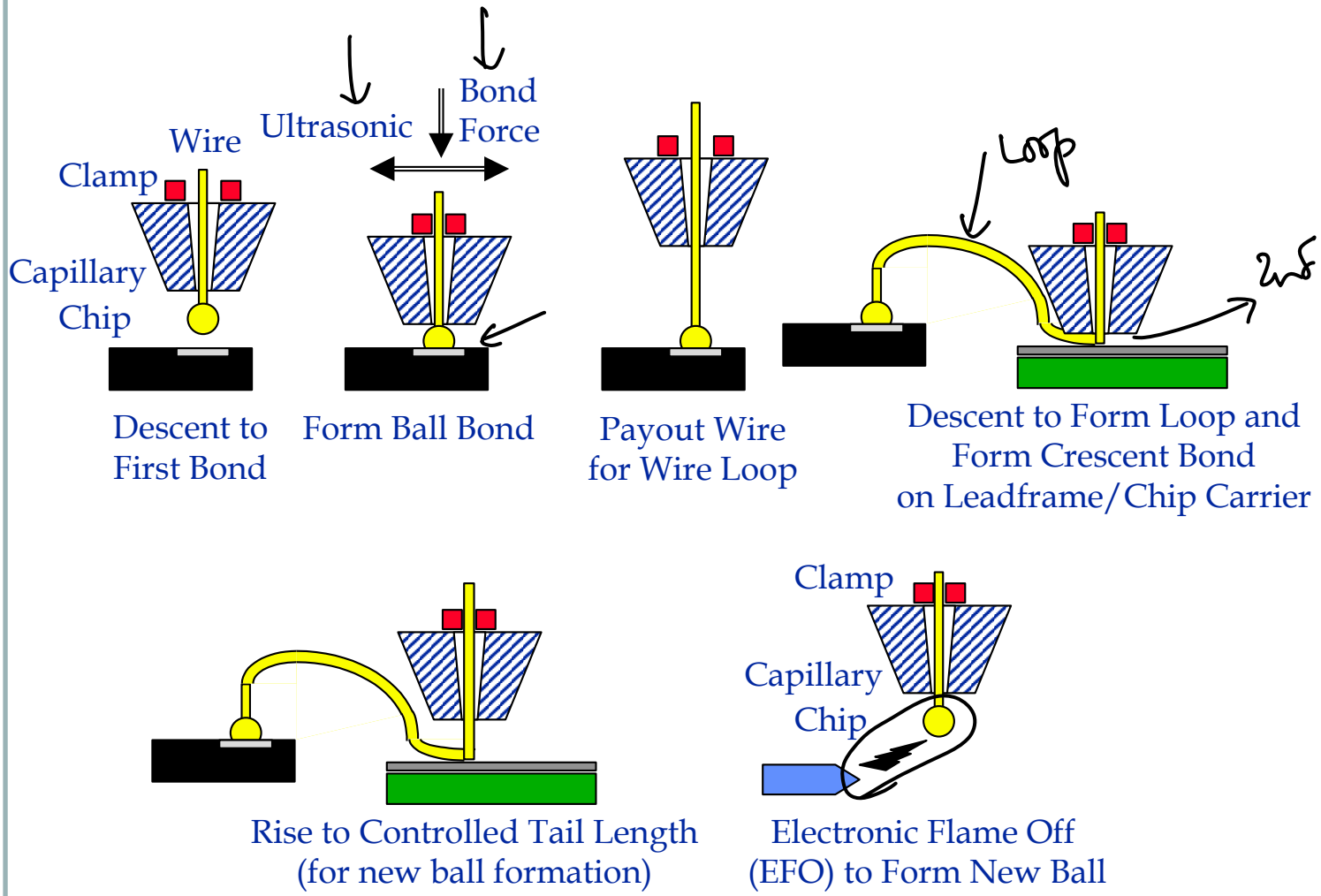
- Capillary loaded with Au wire
- ~~EFO wand~~ generates a spark to melt the Au wire at the tip
- Apply pressure and ultrasonic energy, heat to form ball bond at bond pad on chip side
- Bonding on substrate pad
- Loop formation
- Package bond pad formation by stitch bonding
- Wire break-off to finish process





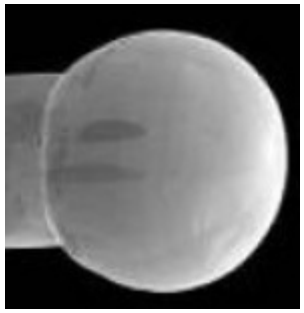
Cross-section view of a QFN package

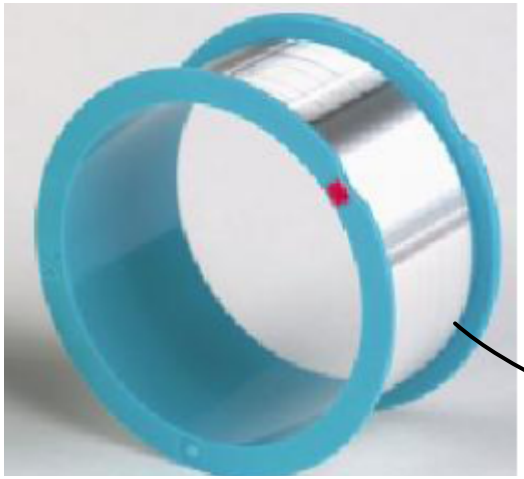
Source: Wikimedia Commons

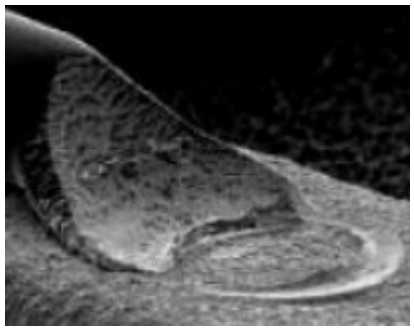


Typical Wirebonding process steps

Source: “Fundamentals of MSP” –Rao Tummala



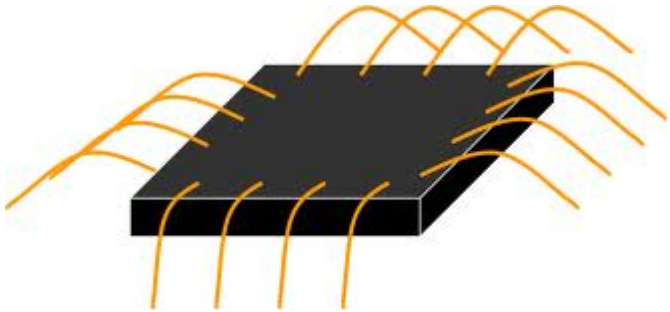




1mil=25.4μm

	20um	25um
Shear Force (g)	12.0	23.2
Shear Strength (g/mil²)	6.5	6.9

1. Wires:
   - Gold Bond Wire
   - Aluminum Wire
   - Copper Wire
2. Pad:
   - Aluminum, gold, silver, Nickel & copper
3. Die bond adhesive
   - Epoxy- organic polymer



Die Bonding

Thanks and Courtesy: © ESEC

Wire Bonding

Thanks and Courtesy: © ESEC

Ball-Wedge-Ribbon Bonding

Thanks and Courtesy: © TWI UK

Features of Wire bonding methods

- High speed (bonding time 40ms:2-4 wires/sec)
- Economical
- Strong bond
- Larger Bonding Pad

(2 mil gold wire: 5*5mil pad)

- Ultrasonic can be used for Al wires
- Thermosonic works at 150 C- faster bond time

Comparison of three methods

Wirebonding	Pressure	Temperature	Ultrasonic energy	Wire	Pad
Thermo-compression	High	300-500 ^{o}C	No	Au	Al, Au
Ultrasonic	Low	<80 ^{o}C	Yes	Al	Al, Au
Thermosonic	Low	100-150 ^{o}C	Yes	Au	Al, Au

1. Bond Failure
   - Wirebond fatigue (temp cycling)
   - Interdiffusion (impurities)
2. Wire failure
   - Wire flexure
   - Vibration fatigue
   - Axial fatigue
3. Corrosion
4. Intermetallic growth properties
   - Au-Be; Al-Si/Mg; Cu-Al..

Testing

1. Bond failure
   - Ball bond shear test
   - Destructive pull test
2. Wire failure
   - Random vibration
   - Accelerated tests as per standards
     - HAST
   - Mechanical shock
3. Testing for Corrosion