REVIEW

Epoxy resin material
different uses

Wire bonding
Tape Automated bonding
Flip chip

1st level interconnection choices
1st level chip connection choices

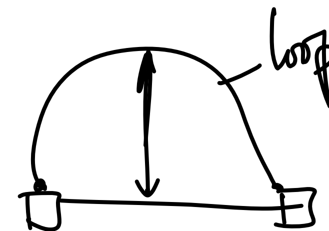
Detailed process steps for WB

Capillary ✓ Ball/Stitch
Wedge ✓

Thermocompression
Thermosonic — Al

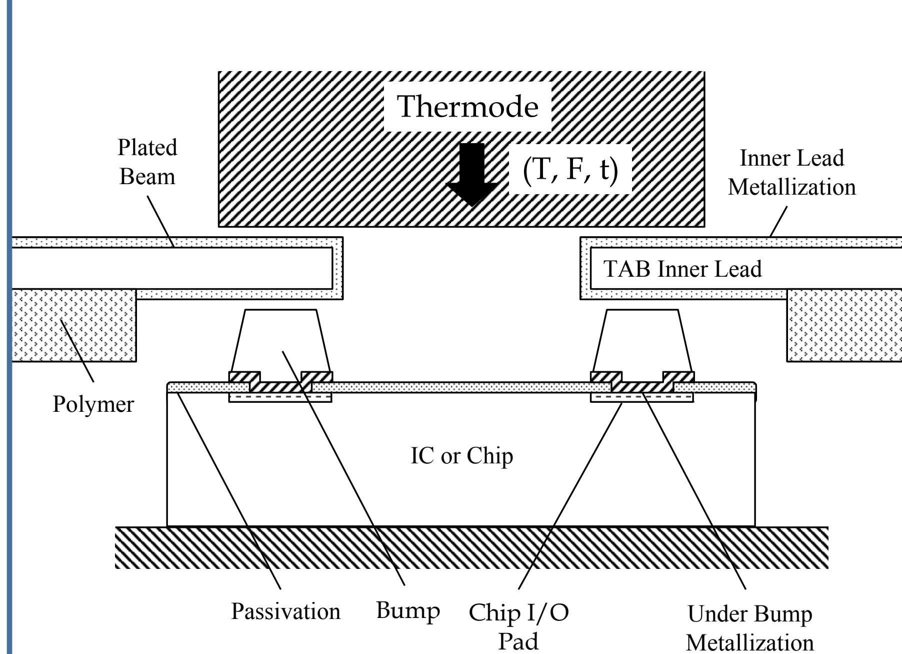
Reliability testing
Failure modes in WB

COB

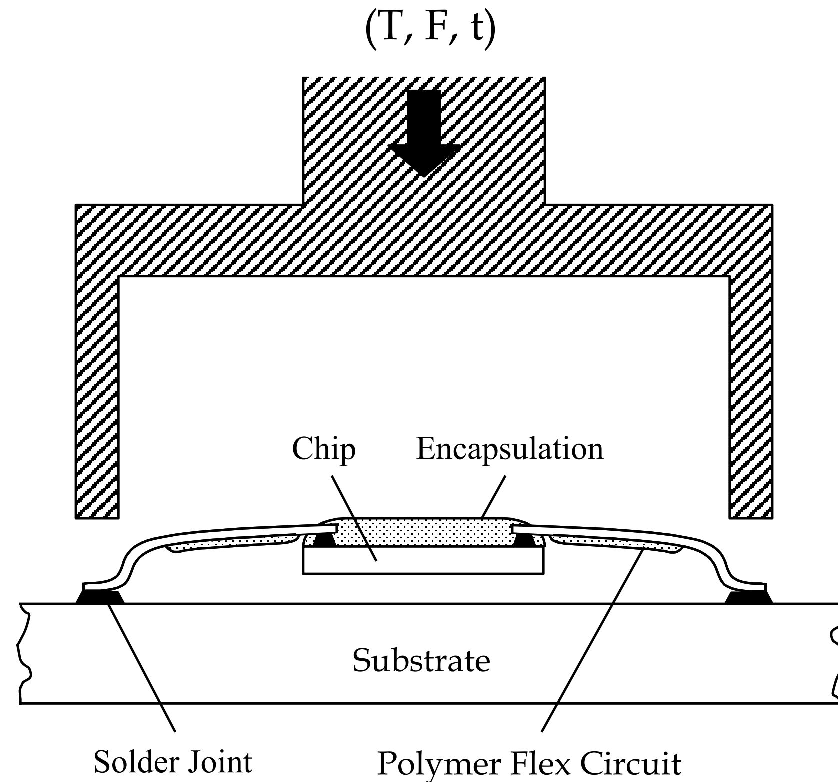


Tape Automated Bonding [TAB] ....an alternative for WB.

As the "pitch" decrease, lead frames become very flimsy....



TAB Inner lead bonding



TAB Outer lead bonding

Source: "Fundamentals of MSP" –Rao Tummala

Tape Automated Bonding

Advantages over wire bonding

1. A smaller bonding pad
2. Smaller on–chip bond pitch ~100 um-125um
3. Decrease in quantity of Gold used
4. Reduction in variations in bond geometry
5. Increase in production rate due to "gang' bonding
   Single point bonding; gang bonding (bar)
   by thermocompression; eutectic reflow (melt) (Sn-Au)?,
   thermosonic; laser
6. Stronger and uniform inner bonding
7. Chip face-up bonding possible

*Disadvantages of TAB technology include the time and cost of designing and fabricating the tape.

*In addition, each die must have its own tape patterned for its bonding configuration.

*For these reasons, TAB has typically been limited to high-volume production applications.

Major limitation- Only peripheral bonding possible

TAB tape materials

- conductors
  - rolled & annealed copper
  - electrodeposited copper
- dielectric
  - polyimides (DEC 3.5; MA% 2-4) (tradenames: Upilex and Kapton)
- Adhesive
- Plating finish (edges)
  - -tin
  - -gold
  - -nickel & gold

Encapsulation

- Epoxies and silicones are popular materials for encapsulation.

Failure

- TAB lead and solder joint failure
- TAB tape
  - Failure due to thermal cycles
  - Metal to dielectric delamination
  - Dielectric expansion
  - Moisture absorption
    - High in polyimides than epoxies
  - Accelerated tests as per standards

thermal behaviour

T_g

thermal cycles, 125°C/100-200……
-25°C to +125°C

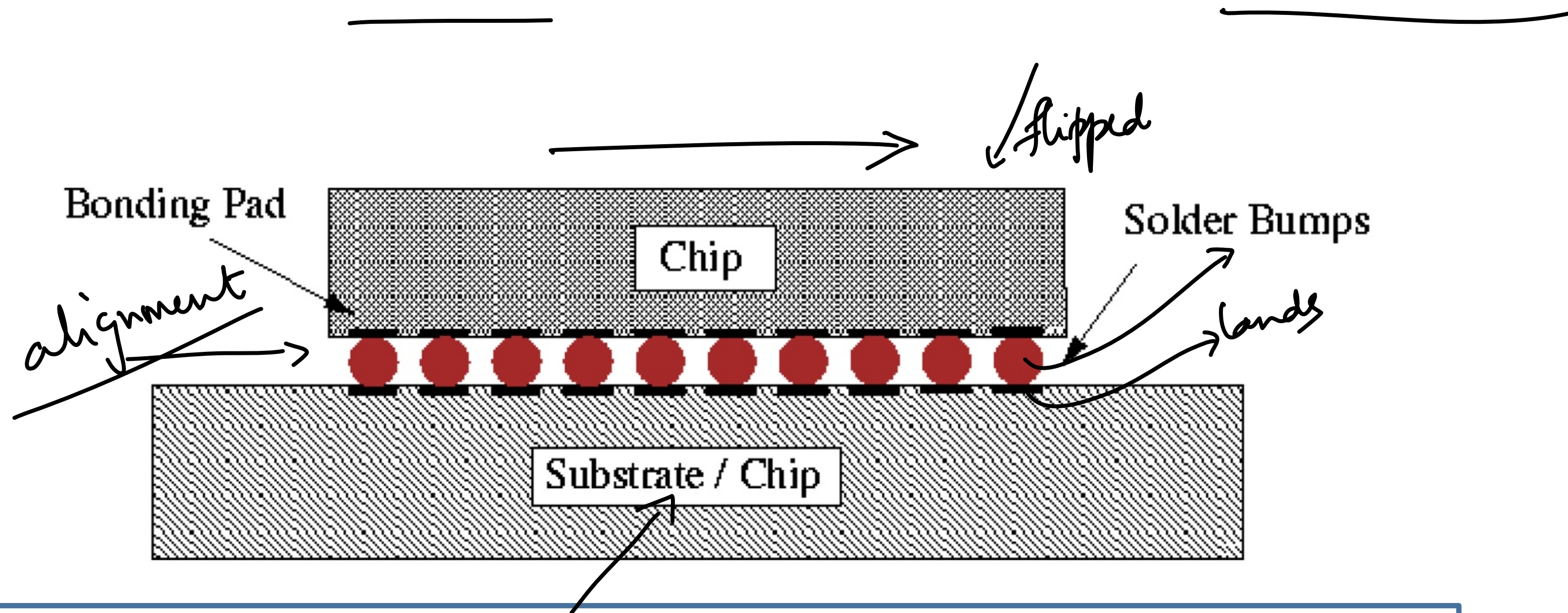
Tape Automated Bonding (TAB)

Thanks and Courtesy: TWI UK

This video clip belongs to TWI UK; used for educational purpose only

Flip-chip bonding

The length of the electrical connection between the chip and substrate can be minimized by placing solder bumps on the die, flipping the die over, aligning the solder bumps with the contact pads [wafer bumping] on the substrate, and reflowing the solder balls in a reflow oven.



FCA with underfill

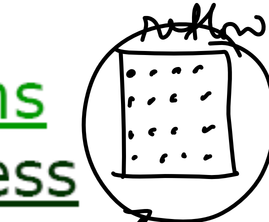
FCA without underfill

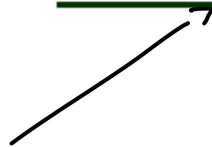
Flip chip method- Advantages

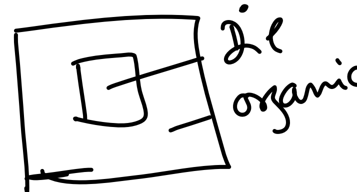
a. Minimum length of electrical connection
b. Ability to use the entire "area" under the die
c. More efficient use of Silicon area
d. SELF-ALIGNING PROPERTY (C4)-
   Controlled Collapsible Chip Connection

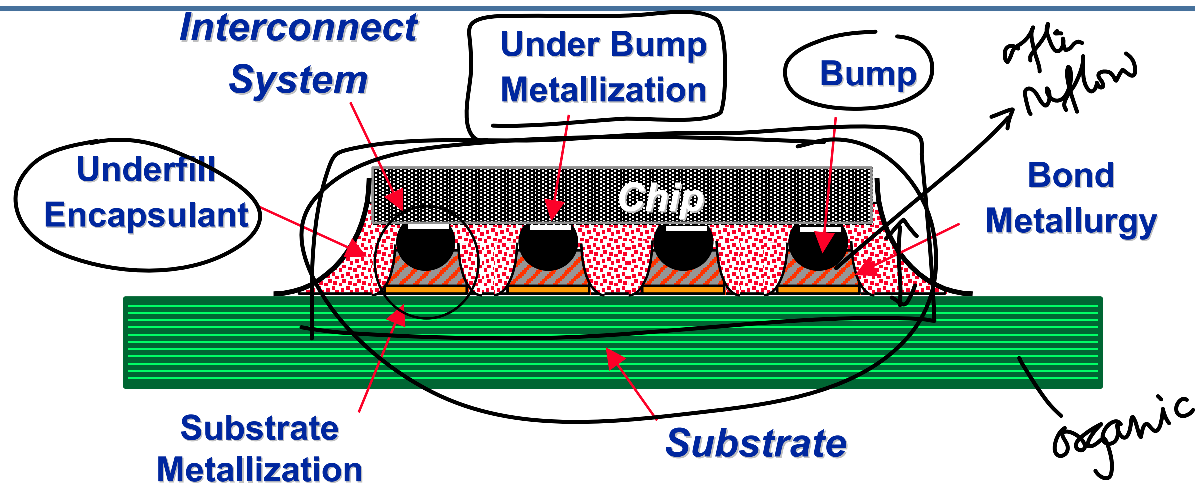
Flip chip method- Disadvantages ??

- Need to dissipate heat to environment faster
- Difficult to inspect the solder joints
- Increased thermal mismatch problems
- Wafer bumping is an expensive process







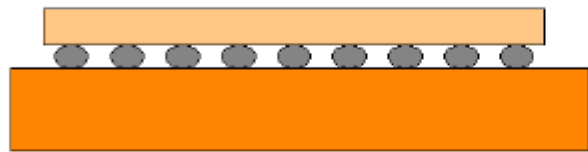


Why Underfill for Flip chip

- Non-Conductive adhesive joining surface of chip to substrate.
- Protects bumps from moisture or other environmental hazards.
- Provides mechanical strength to assembly.
- CTE of silicon is 3 ppm/ °C and typical FR4 (epoxy glass) material is 17 ppm/ °C - large strain observed in solder bumps due to this thermal expansion mismatch
- Compensates for this mismatch
- Thermally conductive; electrically insulating

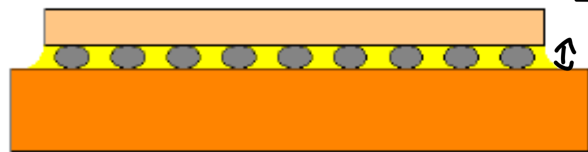
glob top COB

Source: "Fundamentals of MSP" –Rao Tummala



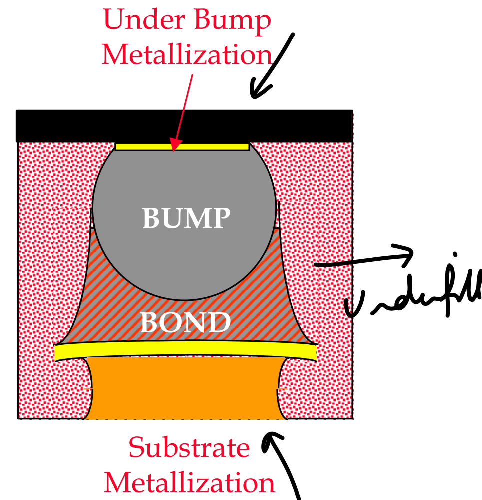
flip-chip
without underfill-material

C4 on organic



flip-chip
with underfill

100-125μ



How to dispense underfill?

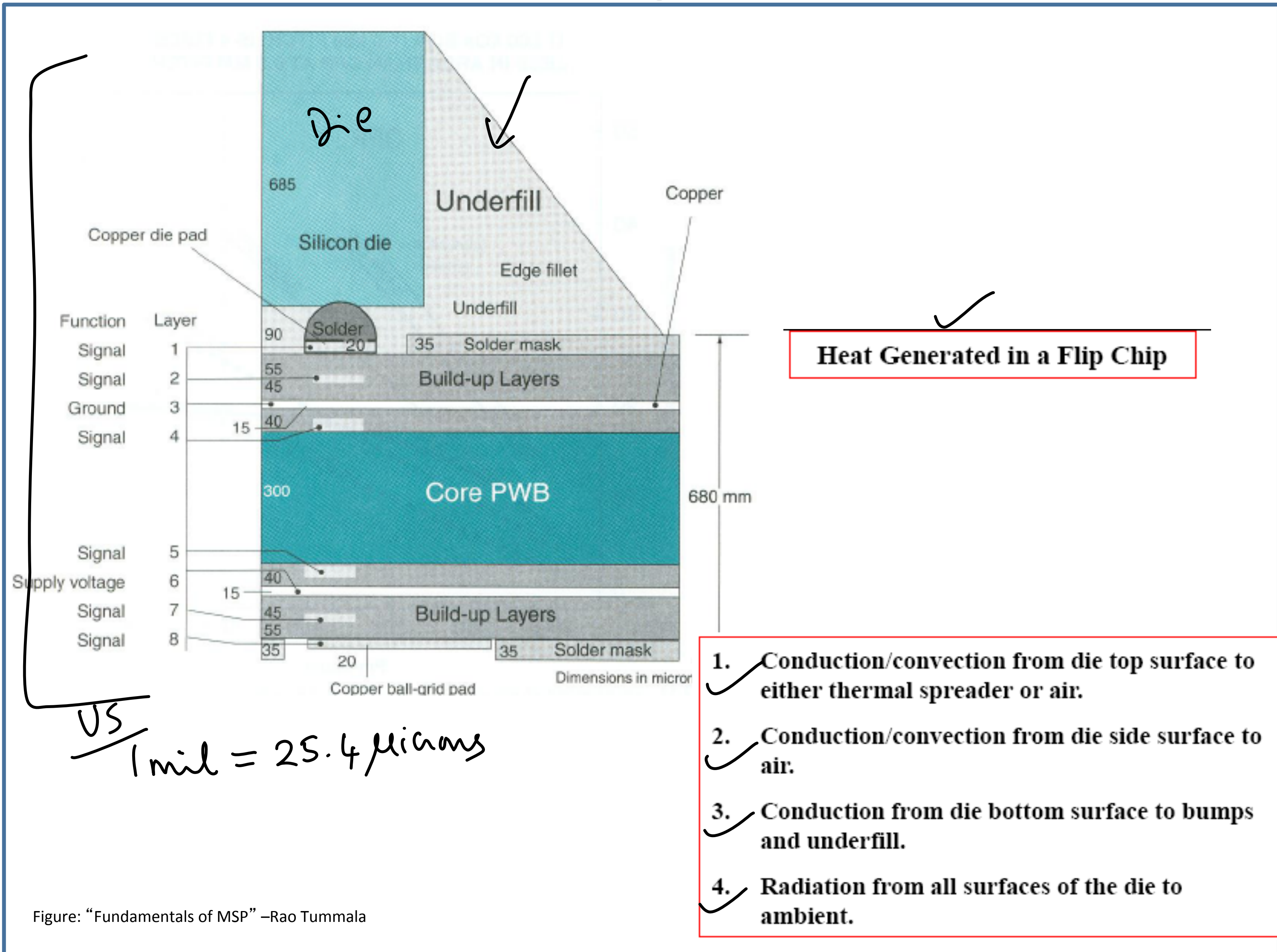
Capillary method:

Underfill

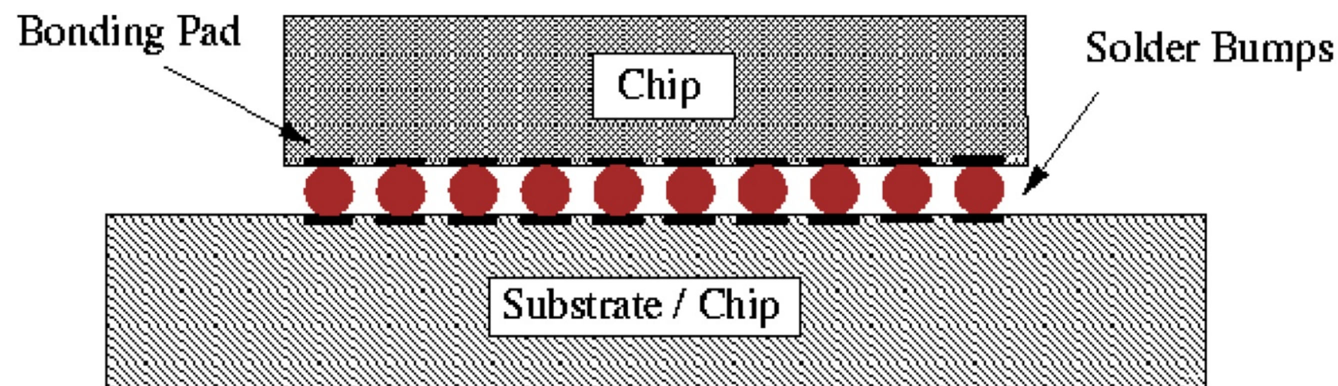
Chip

Substrate

Source: “Fundamentals of MSP” –Rao Tummala

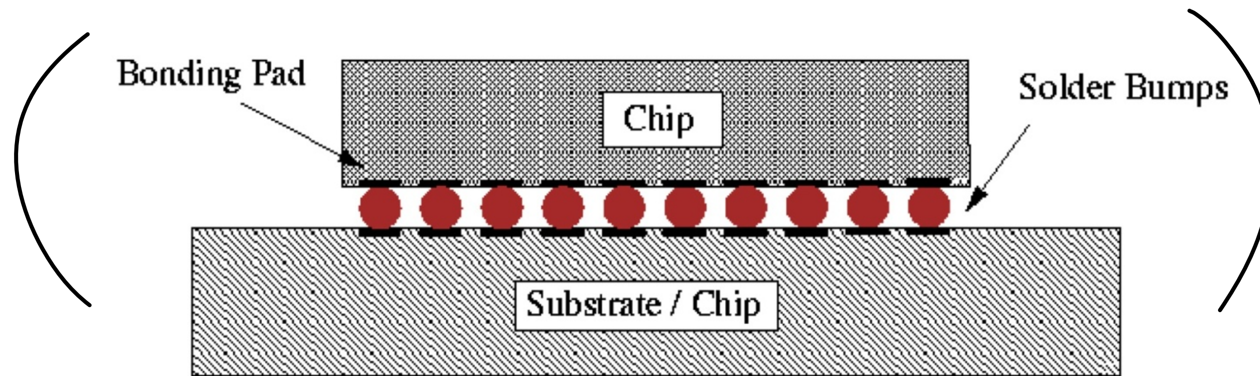

Heat Generated in a Flip Chip
1. Conduction/convection from die top surface to either thermal spreader or air.
2. Conduction/convection from die side surface to air.
3. Conduction from die bottom surface to bumps and underfill.
4. Radiation from all surfaces of the die to ambient.
Die
685
Silicon die
Underfill
Copper
Copper die pad
Edge fillet
Underfill
Function
Layer
Solder
90
20
35
Solder mask
Signal 1
Signal 2
Ground 3
Signal 4
55
45
Build-up Layers
15
40
300
Core PWB
680 mm
Signal 5
Supply voltage 6
Signal 7
Signal 8
40
15
45
55
Build-up Layers
35
35
Solder mask
20
Copper ball-grid pad
Dimensions in micron
US
1mil = 25.4 microns
Figure: "Fundamentals of MSP" –Rao Tummala

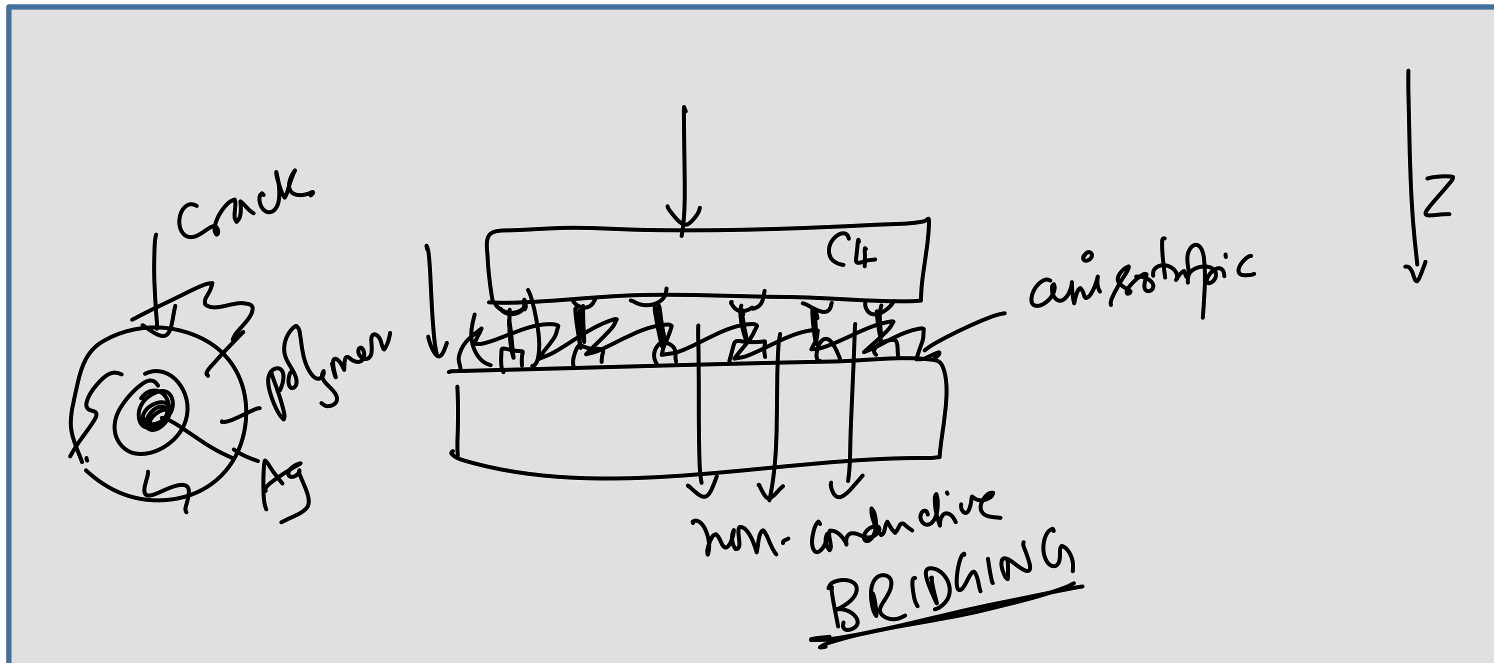
Only reflow process ensures self-alignment
Thermo-compression and Thermo-sonic bonding by using conductive adhesives; heat, pressure and ultrasonic energy; Use of flip-chip bonder equipment
Solder bump can be high-melting solder and bond pad on substrate can be low-melting solder
Use of isotropic and anisotropic conductive adhesives
Anisotropic conductive adhesives are getting popular



FCA with underfill FCA without underfill

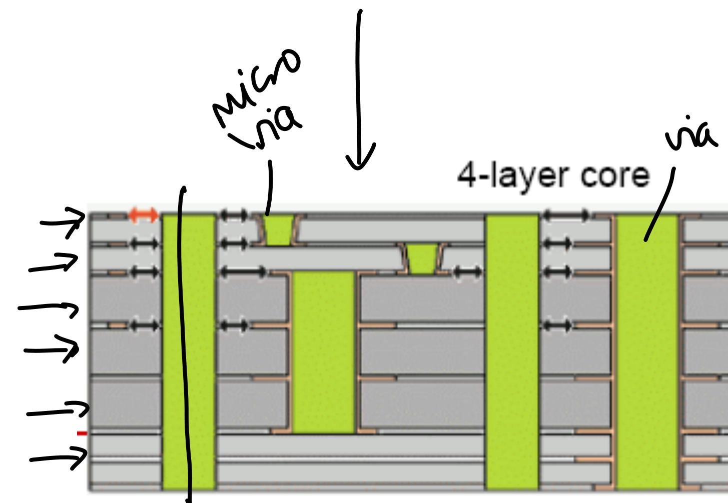
HOW ANISOTROPIC CONDUCTIVE ADHESIVE METHODOLOGY WORKS?





Flip-Chip…The Build-Up Process

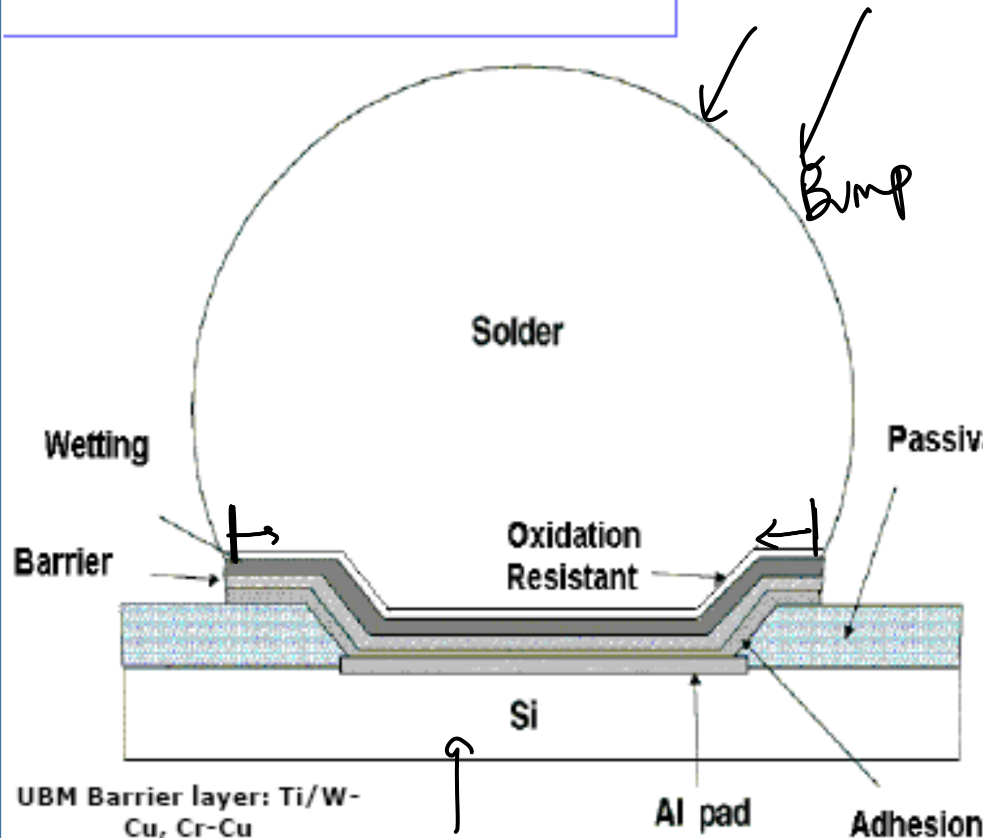
- Based on High Density, Micro Via Organic Substrate
  - Also Referred To As Sequential Build-up (SBU)
  - Requires Flip-Chip Escape Route Patterns
  - Typical Package Assembly Based on a 2-layer Core and Build-Up From Each Side of Core
    - i.e. 3/2/3 process equals 3 build-up layers from each core side
- Die Cost (size) Drives Use of Flip-Chip, Build-Up Process
- Layer to Layer Connections Typically Use:
  - Micro-Vias of 100um or Less
  - Special Patterns (Stagger, Staircase, etc.)
  - Core Vias Larger Than Micro Vias
  - Lines and Spaces < 35um



Performance considerations for the 3 Chip Connection Choices

- Electrical (Performance)
  - Speed, design and testability
  - Low parasitics
- Mechanical/Thermal
  - thermal dissipation , reliability , rework, robustness
- Density
  - chip size vs. I./O interconnects
  - chip to chip spacing (MCM)
- Economics of manufacturing

Flip Chip bond structure



Typical Process Sequence

1. Remove oxide and expose fresh aluminum surface.
2. Deposit 100nm Ti/Cr as the adhesion layer
3. Deposit 80nm of Cr/Cu as the diffusion barrier layer
4. Deposit 300nm of Cu/Ni-V as the solder wettable layer
5. Deposit 50nm of Au as the oxidation barrier layer (optional)

UBM
Under Bump Metallization

Assembly consists of thin metal layers called
-Ball-limiting metallurgy on the die bond pads
-Top-surface metallurgy on the substrate bond pads

Why UBM at all ?

- To reduce mechanical stress caused by reflow process.
- To limit inter-diffusion of metals during soldering and after.
- To strengthen (robustness) of the joint.
- The methodology comes more with experience and defects seen with different materials.

UBM components

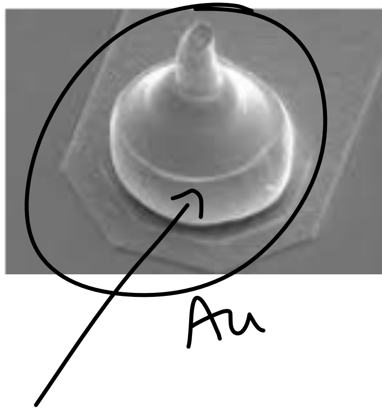
- UBM is to a flip chip bump like foundation to a house
- UBM enhances self-aligning property
- The final metal layers of most IC bond pads is Al
- Al is not readily solderable, neither wettable nor bondable by most solders and get oxidized in air which is insulating
- Adhesion Layer: Adhere to Al pad
- Barrier layer: Diffusion barrier during soldering process
- Wetting layer: Good wetting of solder material
- Oxide resistant barrier: prevents oxide formation of outermost layer

Types of Solder Bump Formation Techniques:

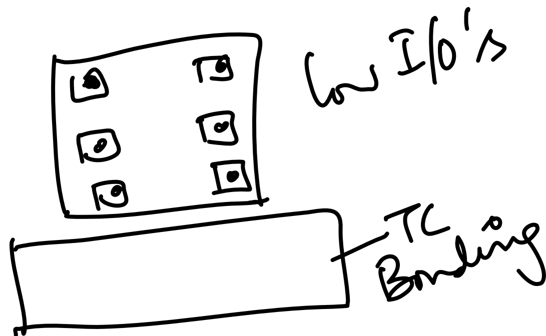
- Evaporation
- Electroplating
- Printing
- Stud Bumping

The result of these methods may differ in bump size and spacing ("pitch"), solder components and composition, cost, manufacturing time, equipment required, assembly temperature, and UBM.

Stud Bumping



- Create conductive gold stud bumps on die bond pads
- Connect to substrate with adhesive or ultrasonic assembly
- No UBM required
- Similar to “ball bonding” process used in wire bonding



COMPARISION

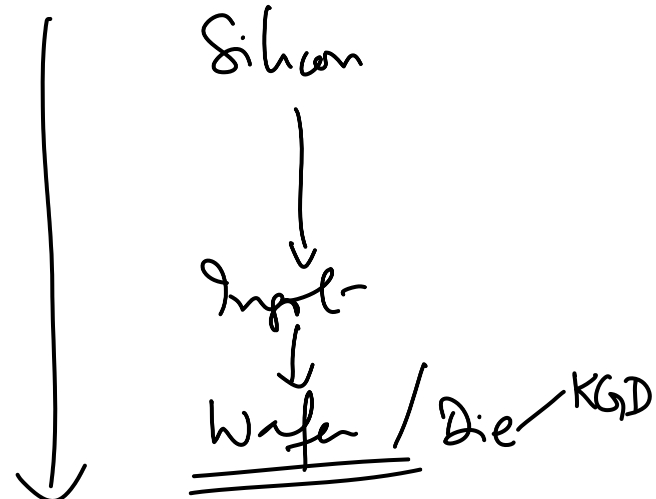
	WIRE BONDING	TAB	FLIPCHIP
COST	Less	Moderate	Less
I/O DENSITY	Low	Moderate	High (area array)
HEAT REMOVAL	Good	Good	Good?
INDUCTANCE	High	Moderate	Low
REWORK POTENTIAL	Low	Low	Moderate

Failure mechanism

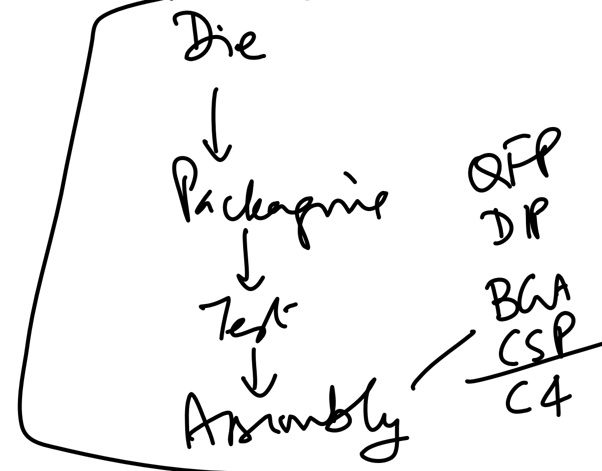
- Solder Joint Fatigue
- Inter-diffusion
- Creep
- Corrosion

Tutorials

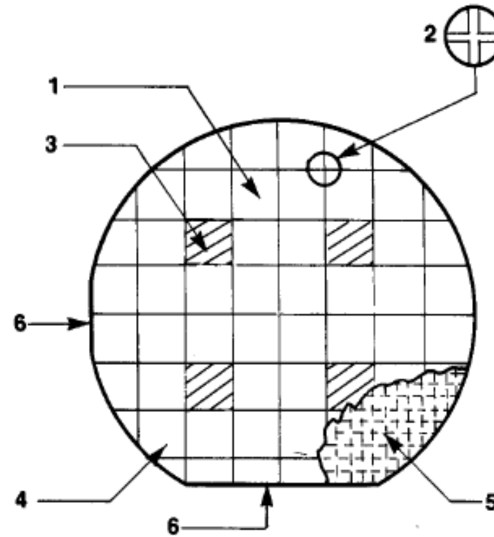
1.What is the chief end-product from front-end processing in semiconductor fab?



2.What are the activities under the head 'back-end process'?



3. Identify the arrowed sections:



4. Why is clean room important in semiconductor wafer fabrication? Define clean room classes.

Class 1
10
100
1000
10000

22nm 32nm
11nm

5. What is CMP? When is it used?

Chem. Mech planarization

6. What is the mask usually made of?

glass mask

7. What is the light source for photolithography?

UV / lithography methods

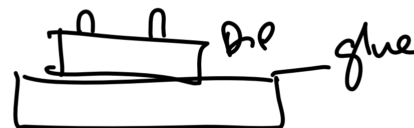
8. What are the metallization methods adopted usually?

plating | CVD, PVD, evaporation

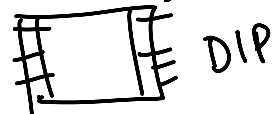
9. When does a die become a KGD?

Die | Test | → KGD

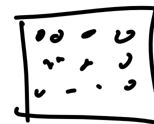
10. What is die bonding?



11. Peripheral and Array bonding? Do you see any significance?



BGA



12. From QFPs to CSPs, there is increase in I/O density. How is this achieved?

pitch → reducing

13. What is SOC, SIP and SOP?

SOC – Sys on chip
SIP – Sys in package
SOP – Sys on package

14. What are first and second level interconnections?

WB
TAB
FC

PCB

15. Name the three first-level interconnection choices.

TAB
WB
FC

16. What packages result from wire bonding process? Give some examples.

DIP SIP
QFP

17. Name two metals used for wire bonding.

Au
Al

18. What are the two bonding methods in TAB?

ILB & OLB

19. What is C4 process?

Self-aligning property

20. Draw the cross-section of a flip chip attachment.

21. Is flip chip a package? Why not?

no! first level

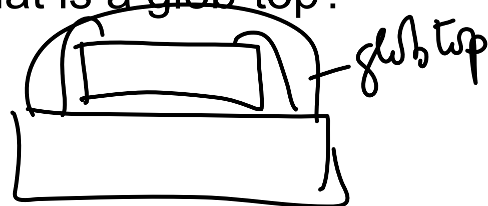
22. Name the two wire bonding tools.

Capillary
Wedge

23. How is TAB encapsulated?

epoxy

24. What is COB? What is a glob-top?



25. What is UBM? Why is it essential for a flip-chip?

Further queries on this chapter? Write to: mahesh@cedt.iisc.ernet.in