# NPTEL VIDEO COURSE ON ELECTRONICS SYSTEMS PACKAGING

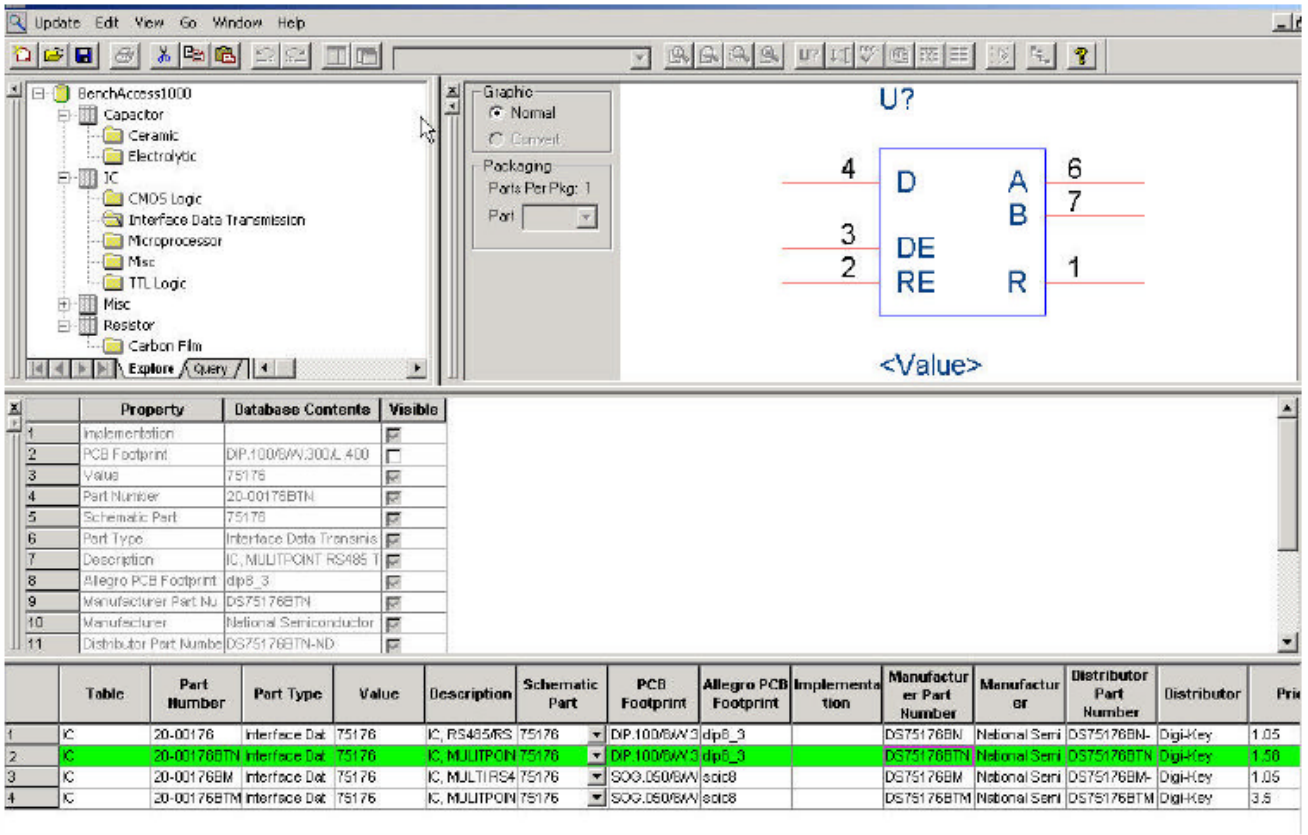
- Introduction to systems packaging
- Semiconductor packaging overview and fundamentals
- Packages
- Electrical design issues in packaging
- CAD for printed wiring boards and Design for manufacturability

- Technology of system-level Printed Wiring Boards

# A QUICK REVIEW OF THE CAD PROCESS STEPS BY ILLUSTRATIONS

# Electrical Component Selection

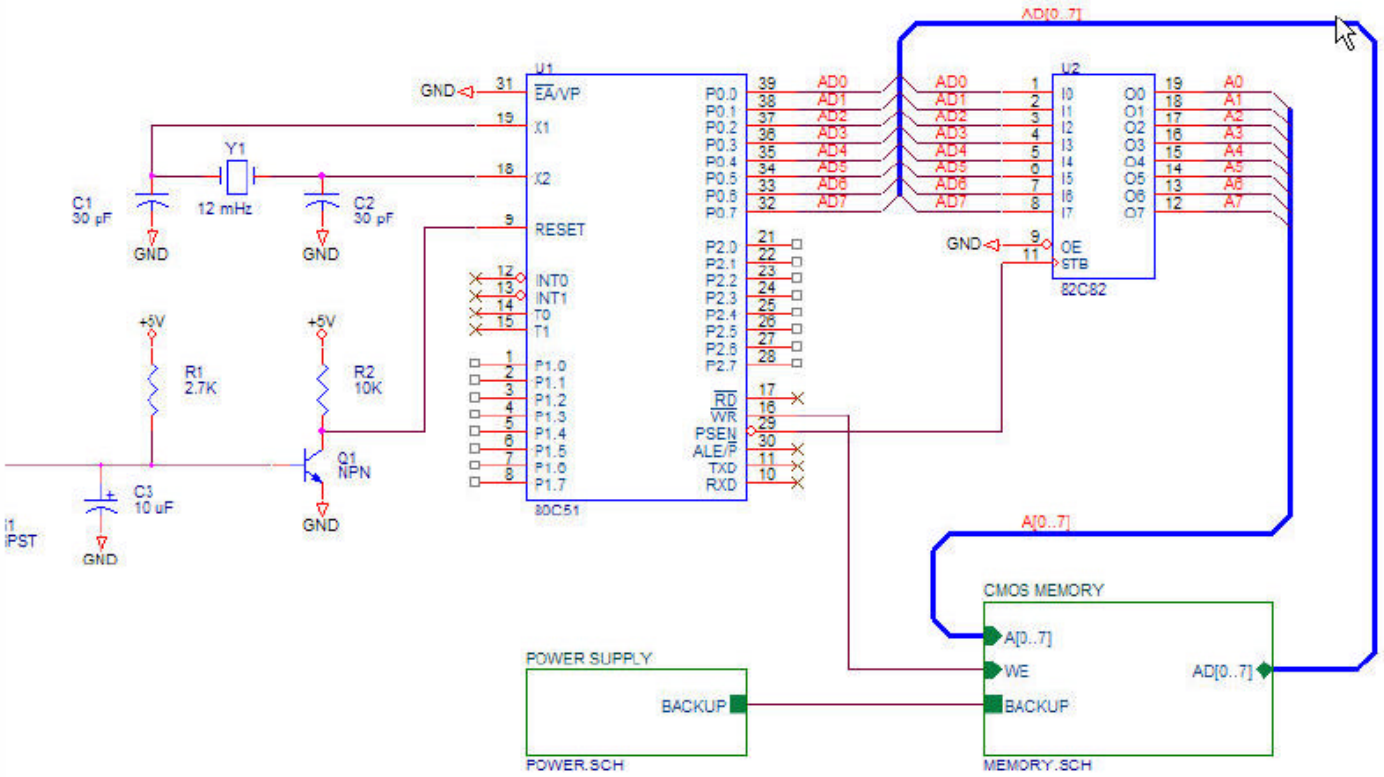
Components that will be used in the electrical schematic are selected and designed.




*Courtesy: PCB3D.COM*

# Schematic

The electrical components are placed in the schematic and net connections established.




*Courtesy: PCB3D.COM*

# Bill of Materials

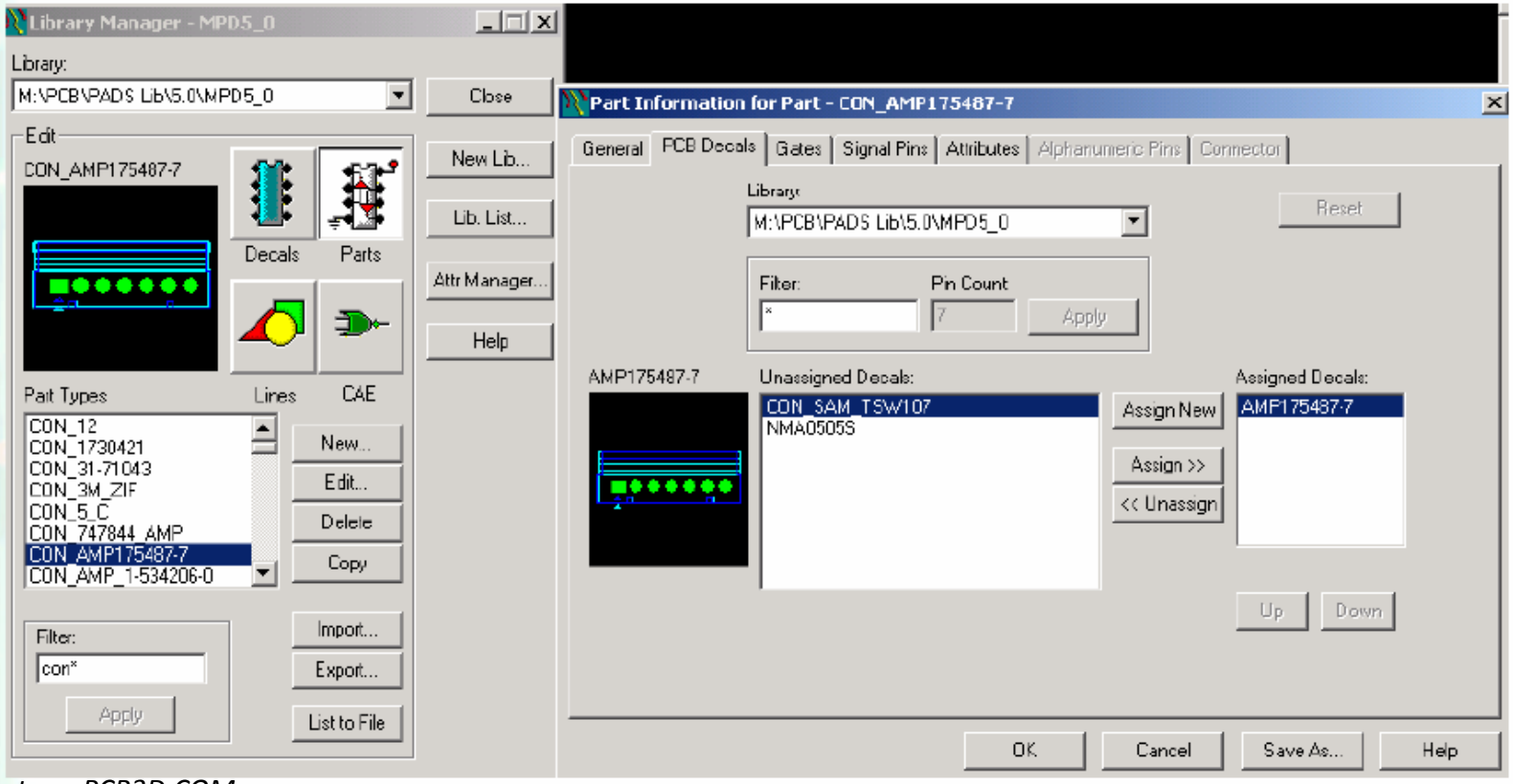
The Bill of Materials is derived from the components that exist in the schematic.

| Item | Quantity | eferenc | Part | Value | Decal | MFG Part Number | Datasheet |
|---|---|---|---|---|---|---|---|
| 1 | 1 | C1 | 1000PF | +/-1% 50V | 1206 | GRM3195C1H102FA01B | ..\..\MurataCerCap.pdf |
| 2 | 2 | C2 | .01UFD | +/-5% 50V | 1206 | GRM3195C1H103JA01J | ..\..\MurataCerCap.pdf |
| | | C14 | .01UFD | +/-5% 50V | 1206 | GRM3195C1H103JA01J | ..\..\MurataCerCap.pdf |
| 3 | 1 | C3 | 4.7UFD | +/-10% 50V | 1812 | GRM43ER71E475KA01L | ..\..\GRM43ER71E475KA01L.pdf |
| 4 | 5 | C4 | 33ufd 25V | +/-10% 25V | C-CASE | B45196E5336K30 | ..\..\B45196E5336K30.pdf |
| | | C5 | 33ufd 25V | +/-10% 25V | C-CASE | B45196E5336K30 | ..\..\B45196E5336K30.pdf |
| | | C6 | 33ufd 25V | +/-10% 25V | C-CASE | B45196E5336K30 | ..\..\B45196E5336K30.pdf |
| | | C8 | 33ufd 25V | +/-10% 25V | C-CASE | B45196E5336K30 | ..\..\B45196E5336K30.pdf |
| | | C16 | 33ufd 25V | +/-10% 25V | C-CASE | B45196E5336K30 | ..\..\B45196E5336K30.pdf |
| 5 | 5 | C7 | .1UFD | +/-10% 50V | 0603 | GRM188R71H104KA93J | ..\..\MurataCerCap.pdf |
| | | C11 | .1UFD | +/-5% 50V | 1206 | GRM319R71H104JA01L | ..\..\MurataCerCap.pdf |
| | | C12 | .1UFD | +/-5% 50V | 1206 | GRM319R71H104JA01L | ..\..\MurataCerCap.pdf |
| | | C13 | .1UFD | +/-5% 50V | 1206 | GRM319R71H104JA01L | ..\..\MurataCerCap.pdf |
| | | C15 | .1UFD | +/-5% 50V | 1206 | GRM319R71H104JA01L | ..\..\MurataCerCap.pdf |
| 6 | 1 | C9 | 1UFD | +/-10% 50V | 1206 | GRM31MR71H105KA88L | ..\..\MurataCerCap.pdf |
| 7 | 1 | C10 | .001UFD | +/-1% 50V | 1206 | GRM3195C1H102FA01B | ..\..\MurataCerCap.pdf |
| 8 | 1 | D1 | MBRS120T3 | - | 403A | MBRS120T3 | ..\..\MBRS120T3-D.pdf |
| 9 | 2 | D2 | MRA4003T3 | - | 403D | MRA4003T3 | ..\MRA4003T3.pdf |
| | | D3 | MRA4003T3 | - | 403D | MRA4003T3 | ..\MRA4003T3.pdf |
| 10 | 6 | D4 | IN4148 | - | MELF3 | LS4148 | ..\..\ln4148.pdf |
| | | D5 | IN4148 | - | MELF3 | LS4148 | ..\..\ln4148.pdf |
| | | D6 | IN4148 | - | MELF3 | LS4148 | ..\..\ln4148.pdf |
| | | D7 | IN4148 | - | MELF3 | LS4148 | ..\..\ln4148.pdf |
| | | D8 | IN4148 | - | MELF3 | LS4148 | ..\..\ln4148.pdf |
| | | D9 | IN4148 | - | MELF3 | LS4148 | ..\..\ln4148.pdf |
| 11 | 1 | D10 | SMCJ16A | - | DO-214AB | SMCJ16A | ..\..\smcjxxx.pdf |
| 12 | 1 | F1 | FUSE | - | 2010 | LBCLRZ2010-R000 | \..\LRZ.pdf |

*Courtesy: PCB3D.COM*

# PCB Component Development

The components that reside on the pcb are designed from the Bill of Materials.
These pcb library parts are captured in the netlist, and consist of a decal and a part name.




*Courtesy: PCB3D.COM*

# Netlist

The netlist is typically an ASCII format generated from the schematic. It contains all components (*part*) and connections (*net*) required for the pcb design.

78727-0122r06.asc - Notepad

File Edit Format Help

```
!PADS-POWERPCB-V3.5-MILS!

*CLUSTER* ITEM


*PART*
Q5 2N7002W
Q9 2N7002W
Q12 2N7002W
Q13 2N7002W
U27 74AHCT1G32DCK
U36 74AHCT1G32DCK
U33 74VHC138MTC
U40 74VHC138MTC
U16 AD5231
U29 AD5231
U35 AD5231
U43 AD5231
U37 AD7888BRU
U38 AD7888BRU
U59 AD7888BRU
U60 AD7888BRU
U5 AD8602ARM
U7 AD8602ARM
U18 AD8602ARM
U47 AD8602ARM
U17 AD8604ARU
U19 AD8604ARU
U20 AD8604ARU
U23 AD8604ARU
U24 AD8604ARU
U25 AD8604ARU
U55 ADN8830ACP
U56 ADN8830ACP
Q10 BSS138@SOT23
Q11 BSS138@SOT23
C1 CAP0402
C2 CAP0402
C3 CAP0402
C4 CAP0402
C5 CAP0402
C6 CAP0402
C7 CAP0402
```

78727-0122r06.asc - Notepad

File Edit Format Help

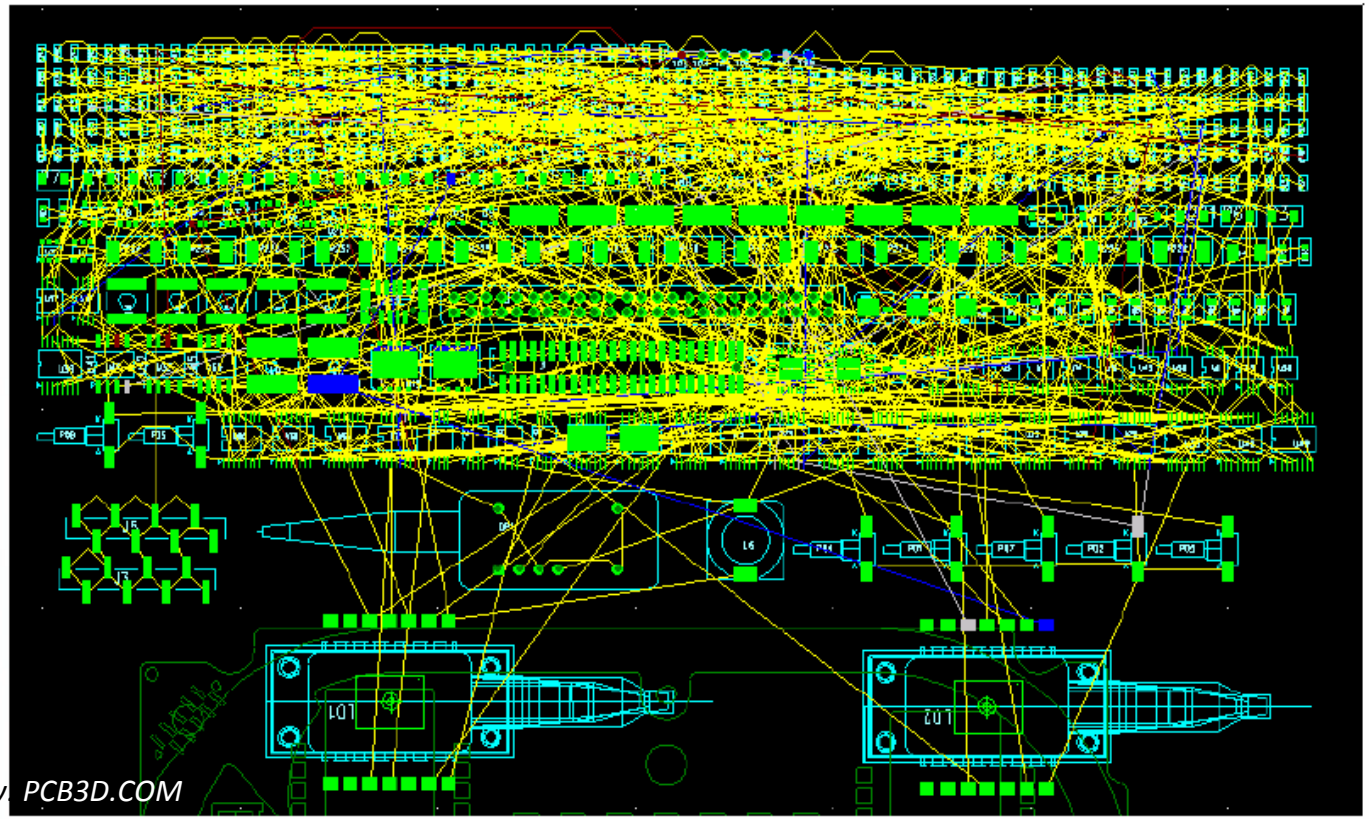
```
OP1 VOA_JDS_MEMS_TH@VOA_JDS_MEMS_TH

*NET*
Q5.1 R59.2 U27.4
*SIGNAL* $4N925
Q9.1 R294.2 U36.4
*SIGNAL* $4N940
Q6.1 Q6.2 Q6.5 Q6.6 R26.2 R194.2
*SIGNAL* $3N1197
C153.1 R195.1 U14.7
*SIGNAL* $3N1206
C153.2 R194.1 R239.2 U14.6
*SIGNAL* $3N1331
R2.1 R28.2 U14.5
*SIGNAL* $3N1349
C53.2 R27.1 R172.2 U11.3
*SIGNAL* $3N1358
D6.A L8.2 U11.1
*SIGNAL* $3N1381
Q6.3 R195.2
*SIGNAL* $3N1420
J4.39 R276.2 R278.2
*SIGNAL* $3N1422
J4.40 R277.1 R279.1
*SIGNAL* $3N1445
Q8.3 Q8.6 R280.1
*SIGNAL* $3N1450
Q8.2 Q8.5 R281.2 R311.1
*SIGNAL* $3N1456
TP9.1 TP10.1 U7.1 U7.2
*SIGNAL* $3N1463
R281.1 U22.5
*SIGNAL* $3N1472
C36.1 R199.2 U22.1
*SIGNAL* $3N1474
C142.1 R282.2 U22.3
*SIGNAL* $3N1477
C151.2 R30.1 R282.1 R283.2
*SIGNAL* $3N1520
Q7.A1 R280.2
*SIGNAL* $4N299
C58.1 R31.2 U3.3
*SIGNAL* $4N314
```

*Courtesy: PCB3D.COM*

# PCB Netlist Verification

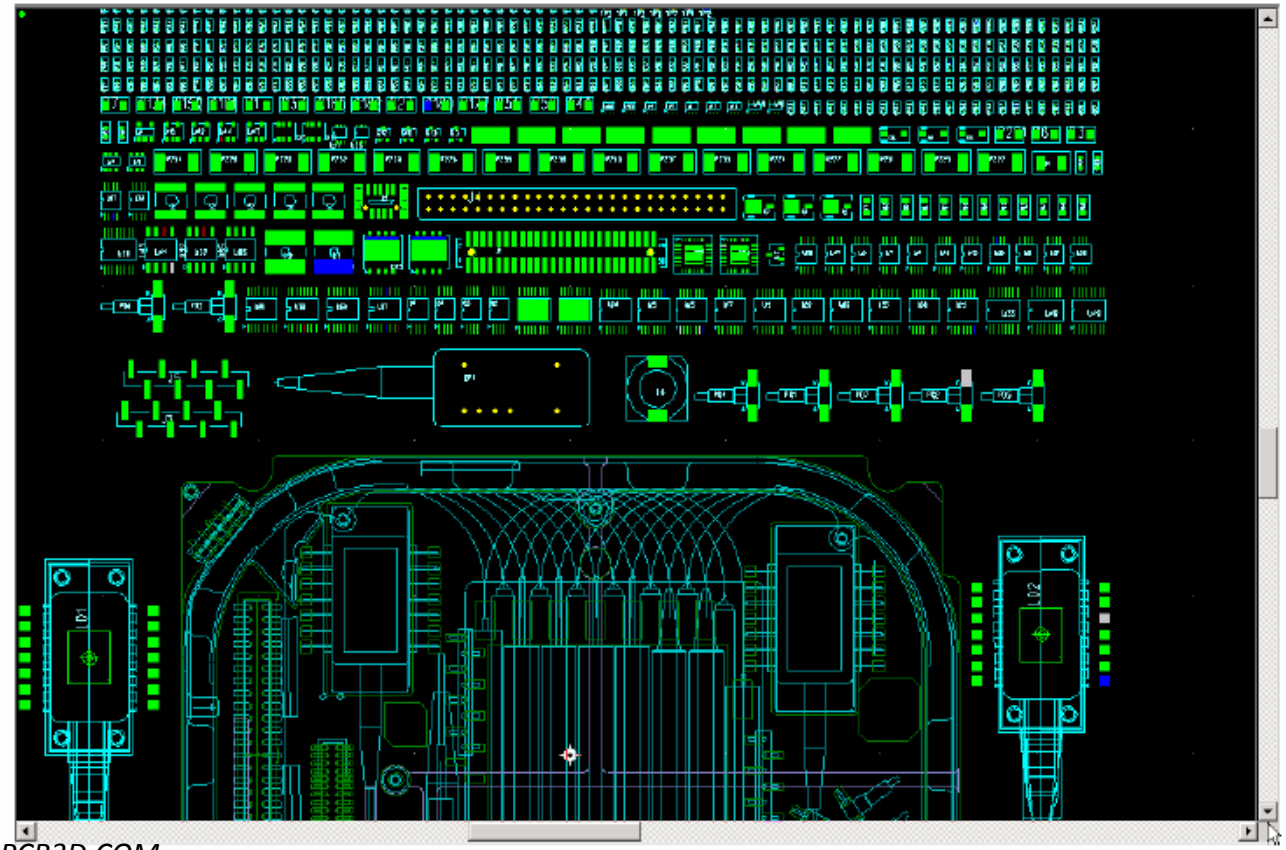
The netlist is imported into the pcb database. If all components and connections from the netlist match the pcb database of library components, they will appear as pictured below. Green indicates all components (*part*), yellow indicates connections (*net*) to the components.



*Courtesy PCB3D.COM*

# PCB Design: Components

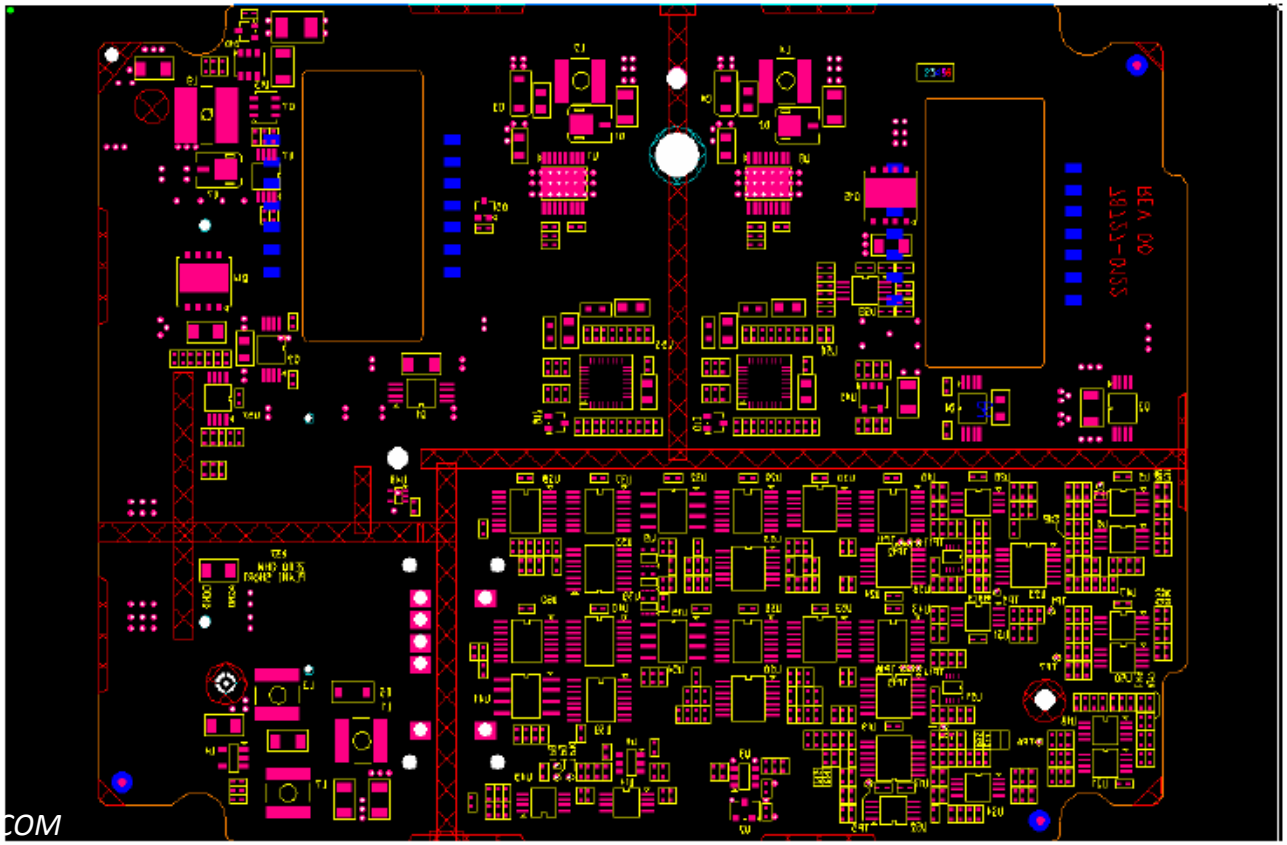
Components from the netlist are dispersed and grouped according to function.
The components are then manually placed inside the pcb outline.



*Courtesy: PCB3D.COM*

# PCB Design: Placement

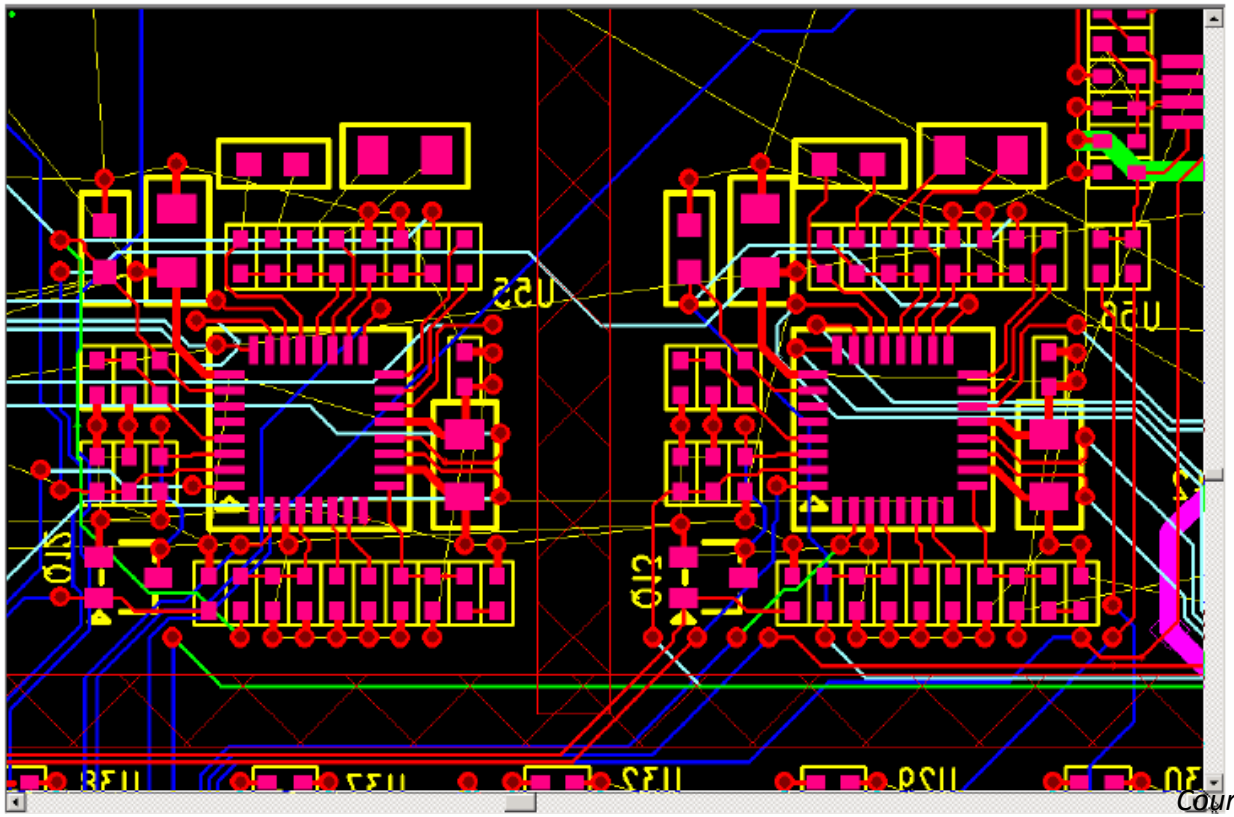
Components are placed within the pcb board outline.
Keepouts, cutouts and holes must be avoided.



*Courtesy: PCB3D.COM*

# PCB Design: Routing

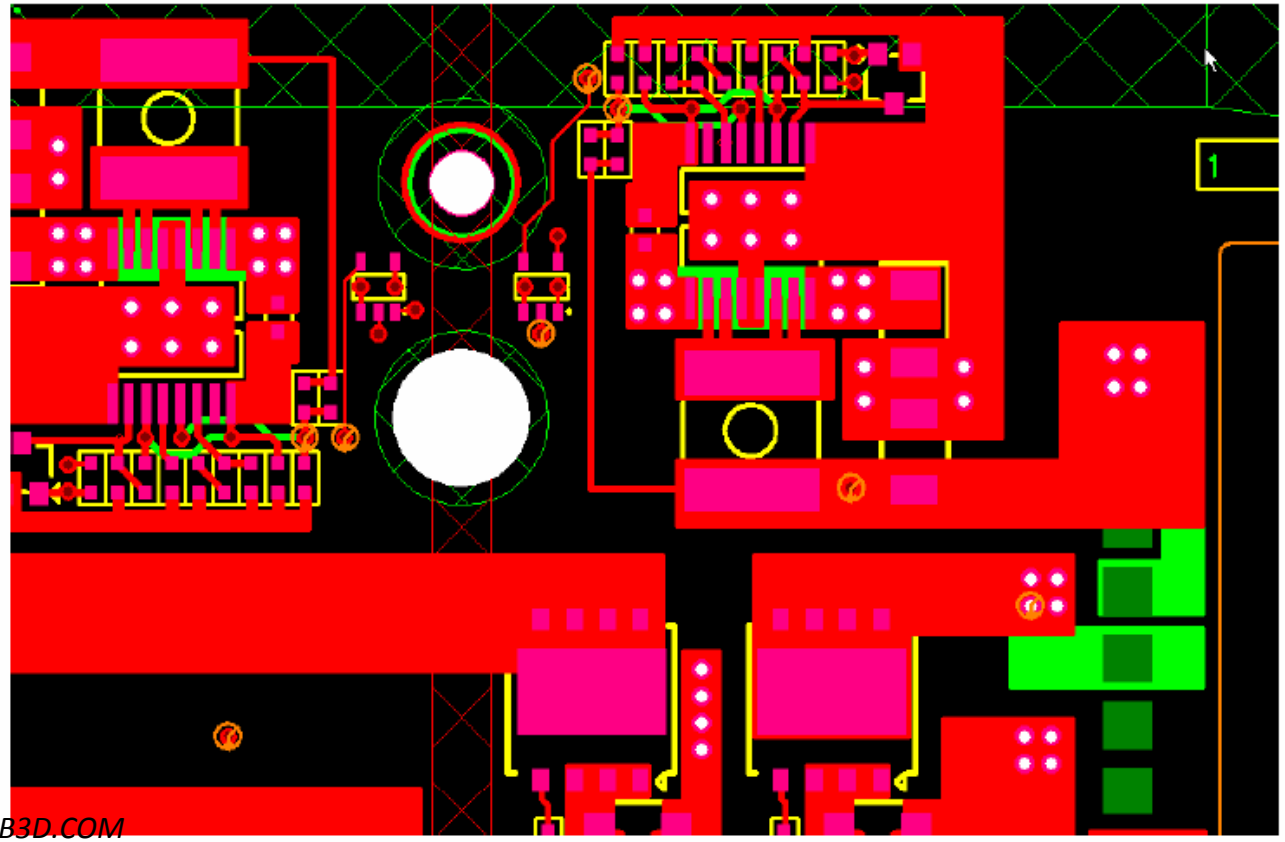
All connections (nets) require trace routing.
The red lines are completed trace connections.
The yellow lines represent unrouted traces or nets.
Plane connections are created with a via or direct connection to a copper area.
Trace routing may consist of component to component or component to plane connections.



*Courtesy: PCB3D.COM*

# PCB Design: Copper

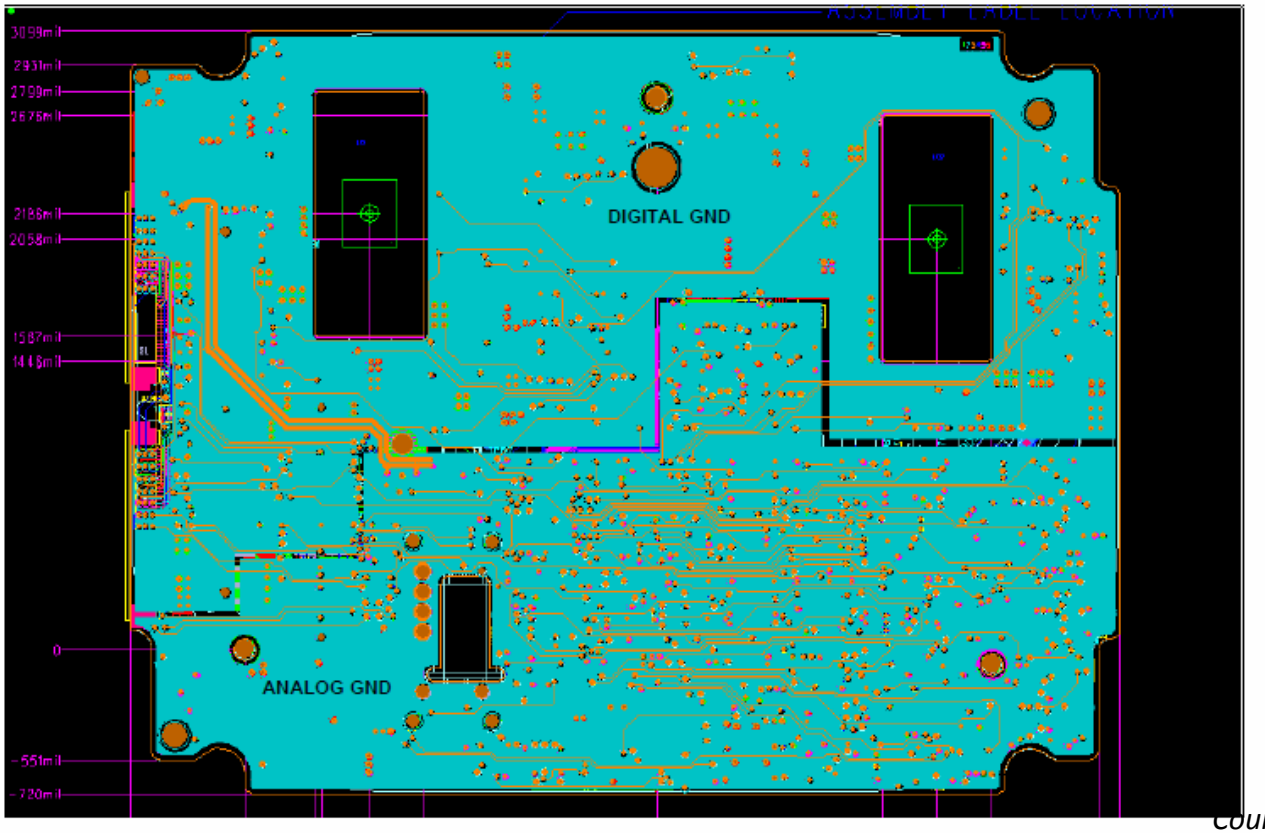
Copper areas are created (red) and poured over vias (white circles) and solder pads (violet). Copper areas are then assigned a net name that matches with the appropriate net connection.




*Courtesy: PCB3D.COM*

# PCB Design: Plane

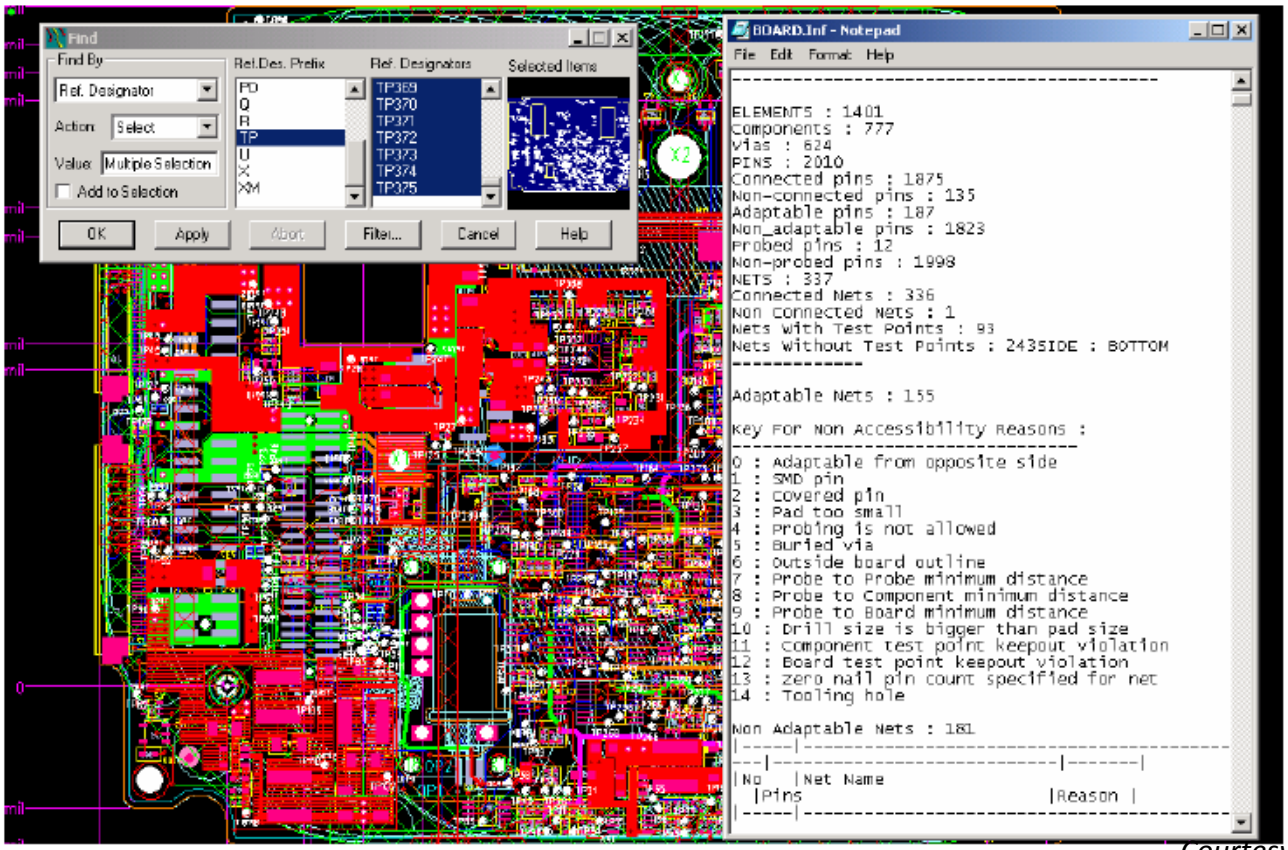
The copper planes are created, split and defined according to the design rules and net requirements for each layer. Thermal and non-thermal connections are placed accordingly.




*Courtesy: PCB3D.COM*

# PCB Design: DFT

Design for Test involves placement of test points into the completed pcb.
Two types of test points are used. Flying Probe (FPT) and In Circuit (ICT).
DFT analysis is executed and test points are audited for compliance and testability.

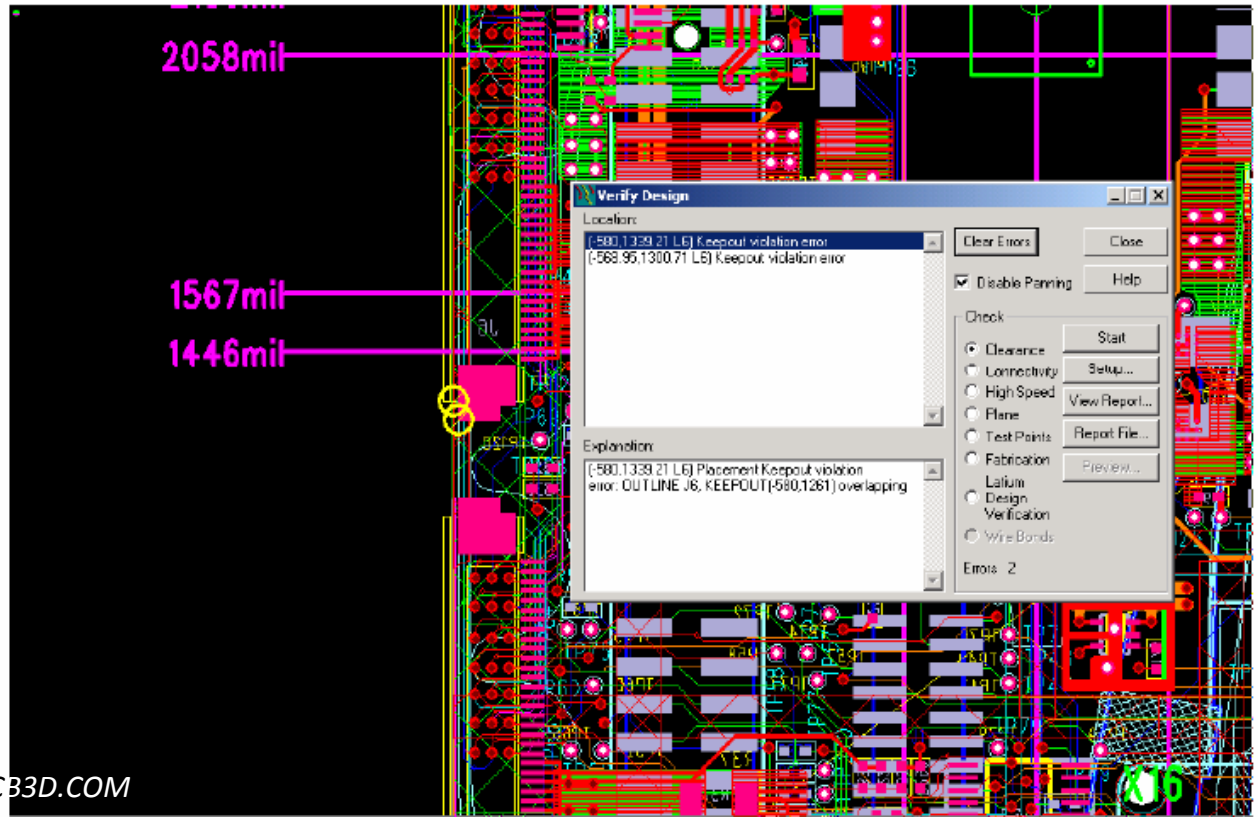



*Courtesy: PCB3D.COM*

# PCB Design: Verification

The pcb is complete and must be verified for design rules compliance. Verification includes clearance checks, net and copper connectivity, net and copper plane connectivity, duplicate nets, layer to layer connectivity, design rule violations, DFM and test points.

In this example, the yellow circles indicate a clearance violation (copper to board edge).




*Courtesy: PC3D.COM*

# Gerber Files

Gerber files are created to enable plotting of the individual design file elements. Depending on their function, each Gerber file is compiled as an individual electrical layer, process or design reference.

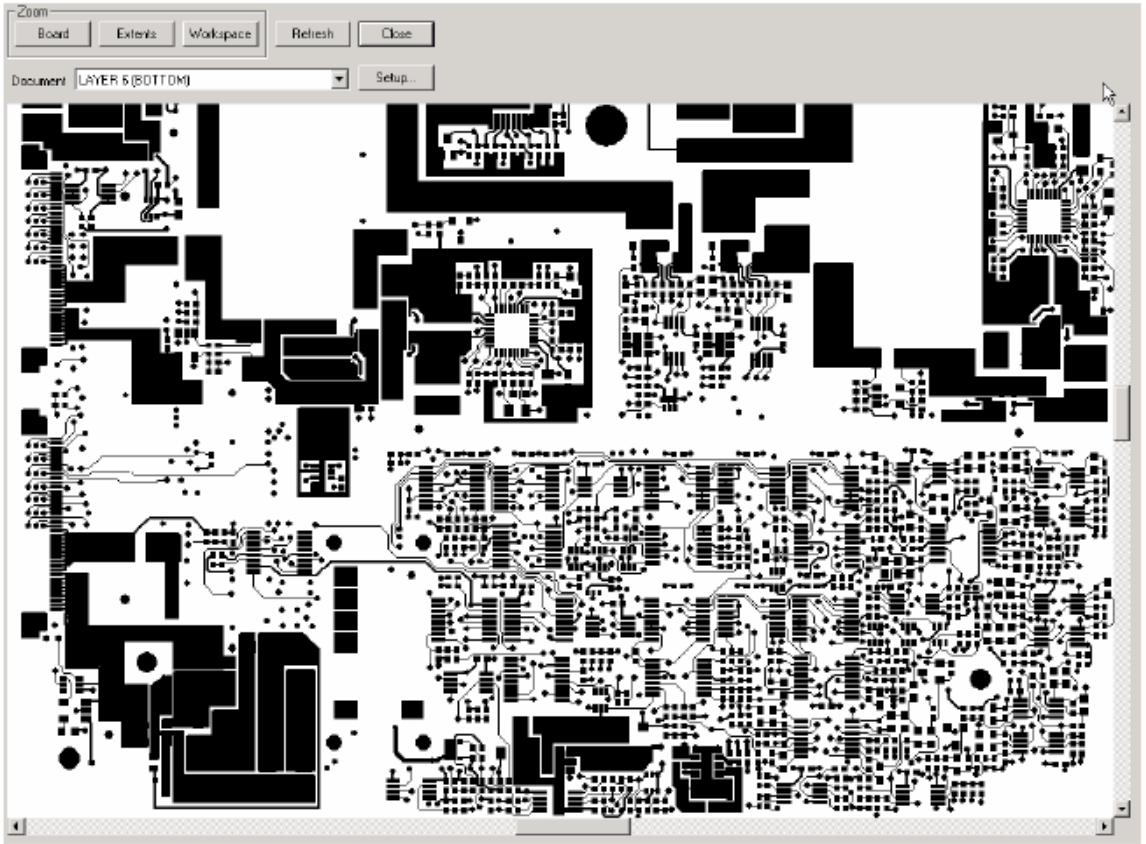
Typical Gerber File Structure

- Electrical Design Layers
- Silkscreen
- Solder Mask
- Solder Paste
- Fabrication Drawings
- Assembly Drawings
- Aperture Files
- Drill Files
- Netlist
- X-Y Placement Data

*Courtesy: PCB3D.COM*

# Gerber Files: Electrical Layers

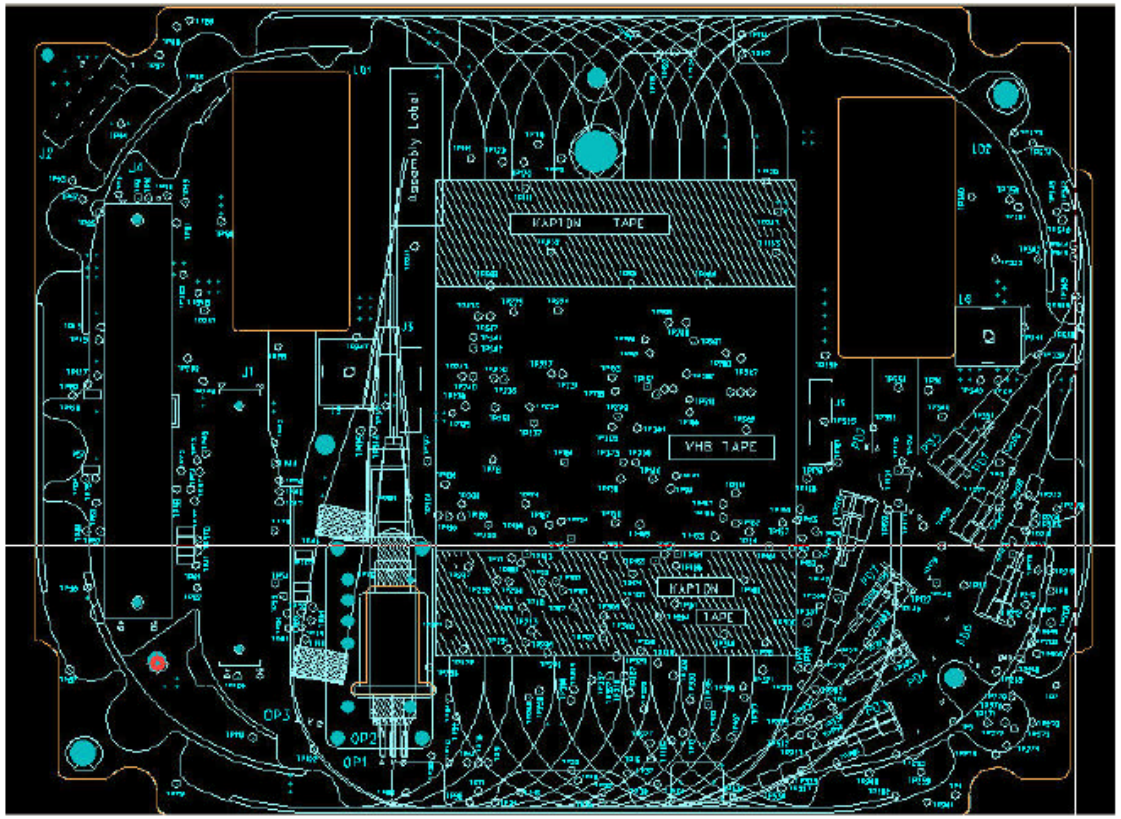
These Gerber files are processed to create each electrical layer (internal and external) that will ultimately be finished in copper on the pcb.




*Courtesy: PCB3D.COM*

# Gerber Files: Silkscreen

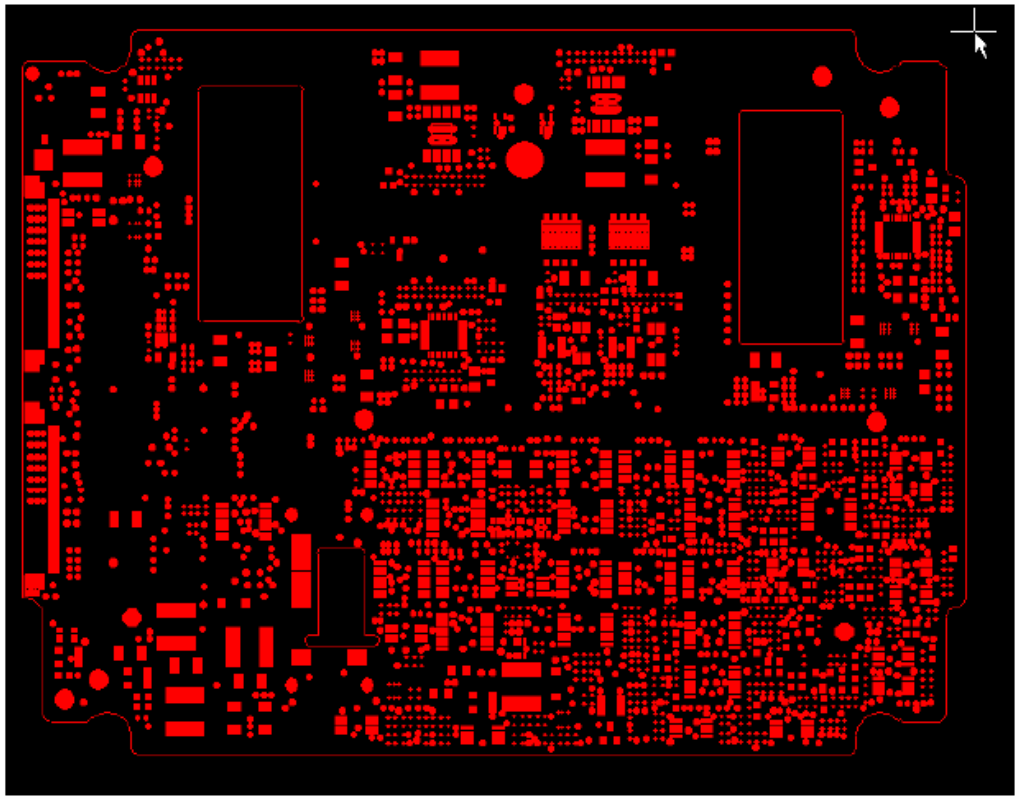
This file will create the stencil that will be used to apply the silkscreen (ink) to the pcb.
The Silkscreen is for component reference, identification and labeling.
The Silkscreen exists on the outer layers.




*Courtesy: PCB3D.COM*

# Gerber Files: Solder Mask

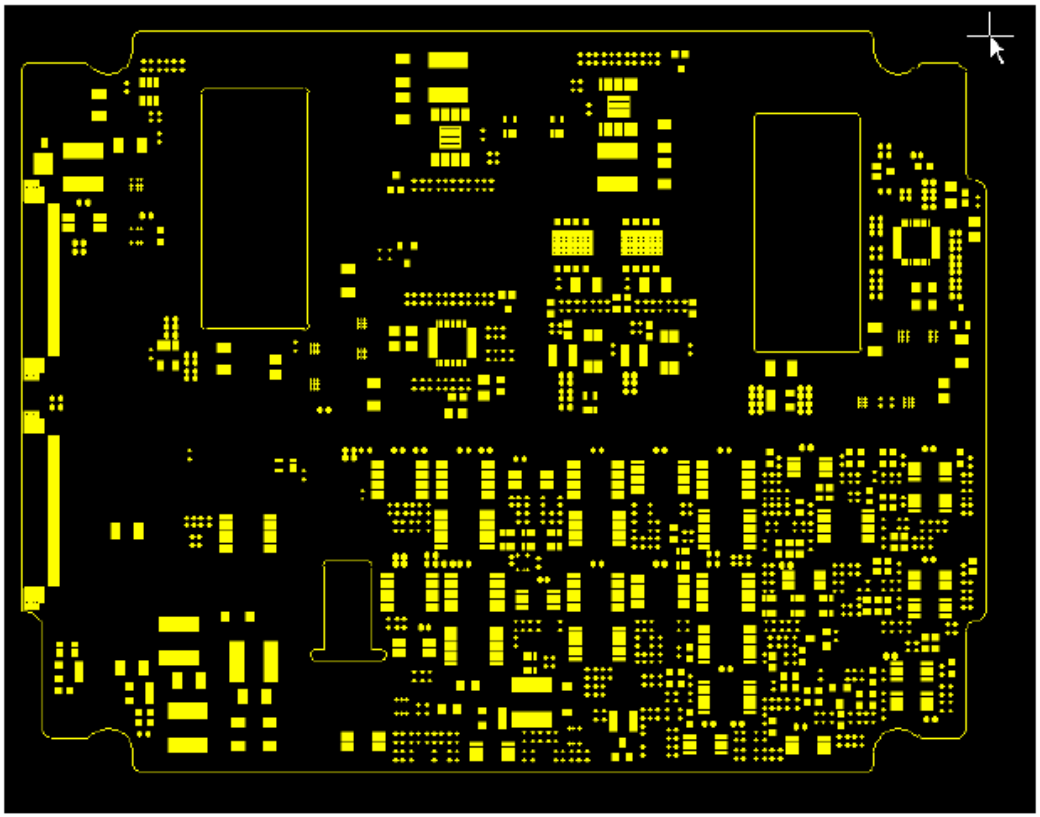
The solder mask will expose solderable areas and protect the pcb by covering all copper elements. The Solder Mask minimizes solder bridges.
In this example, the Gerber file was created as a negative. Areas in red will not be covered with mask. The solder mask exists on the outer layers.



*Courtesy: PCB3D.COM*

# Gerber Files: Solder Paste

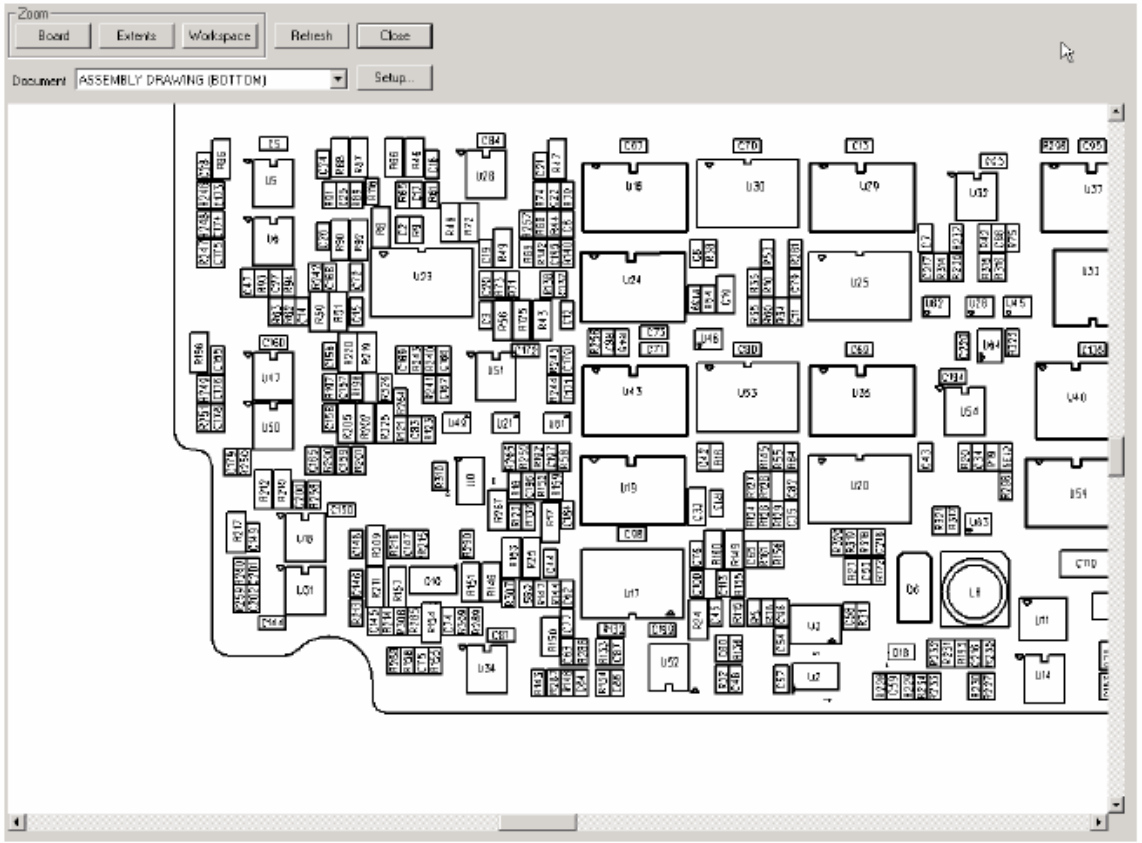
This file will be used to create a solder paste stencil. Prior to the board assembly, the stencil will be used to apply solder paste directly to the pads on the pcb (areas in yellow). Once the solder paste is applied, surface mount components can be placed and soldered.



*Courtesy: PCB3D.COM*

# Gerber Files: Assembly Drawing

Identifies location and orientation of the electronic components to be placed.




*Courtesy: PCB3D.COM*

# Gerber Files: Aperture Listing

This listing defines the shape of individual elements on the pcb.

Photo-Plotter Apertures Report

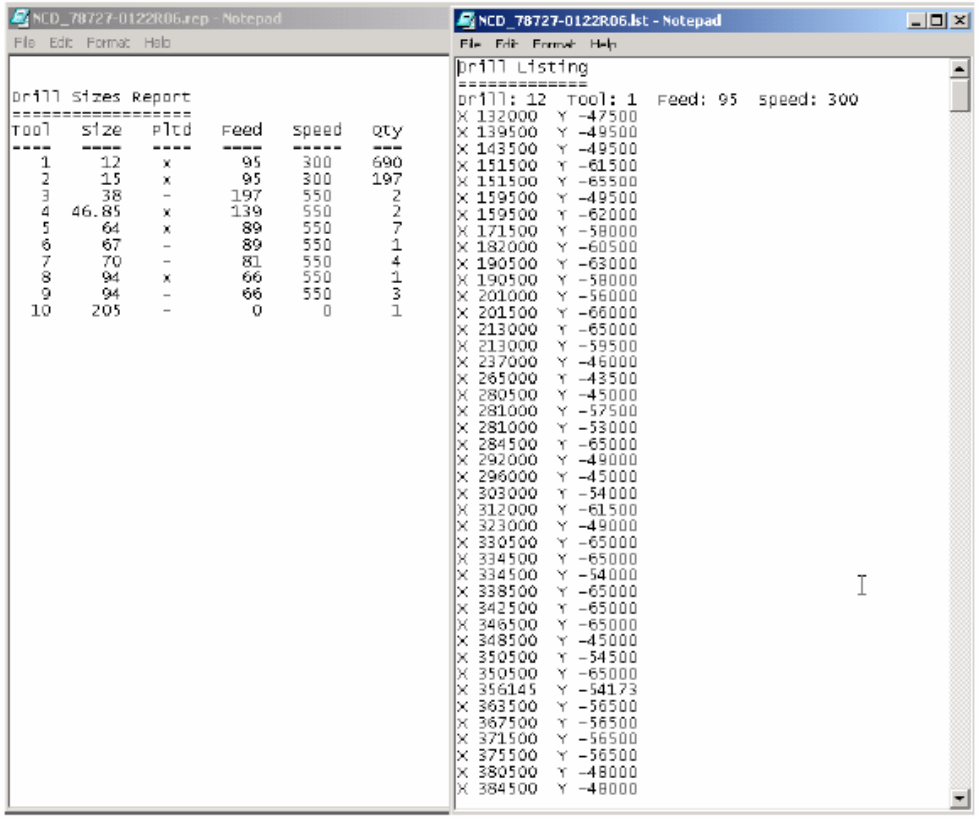
| Position | Width | Hgt/ID | Shape | Qty |
|---|---|---|---|---|
| 10 | 25 | 0 | RND | 292 |
| 11 | 20 | 0 | RND | 65 |
| 12 | 10 | 0 | RND | 3606 |
| 13 | 7 | 0 | RND | 61 |
| 14 | 5 | 0 | RND | 34500 |
| 15 | 1 | 0 | RND | 2 |
| 16 | 8 | 0 | RND | 4011 |
| 18 | 94 | 0 | RND | 8 |
| 21 | 70 | 0 | RND | 16 |
| 25 | 45 | 70 | RECT | 28 |
| 27 | 30 | 0 | RND | 916 |
| 28 | 50 | 0 | SQR | 38 |
| 35 | 40 | 0 | SQR | 32 |
| 48 | 12 | 0 | RND | 197 |
| 49 | 15 | 0 | RND | 40 |
| 51 | 35 | 0 | RND | 197 |
| 54 | 18 | 0 | RND | 37 |
| 59 | 3 | 0 | RND | 1202 |
| 60 | 100 | 0 | RND | 4 |
| 68 | 75 | 0 | RND | 8 |
| 74 | 55 | 0 | SQR | 28 |
| 75 | 105 | 0 | SQR | 1 |
| 78 | 34 | 0 | SQR | 50 |
| 79 | 25 | 0 | SQR | 46 |
| 80 | 35 | 0 | SQR | 1 |
| 89 | 0.5 | 0 | RND | 58 |
| 90 | 4 | 0 | RND | 641 |
| 92 | 6 | 0 | RND | 48 |
| 106 | 30 | 0 | SQR | 26 |
| 111 | 31 | 0 | SQR | 10 |
| 112 | 40.16 | 0 | SQR | 100 |
| 114 | 27.56 | 0 | SQR | 24 |
| 115 | 15.75 | 0 | SQR | 386 |
| 116 | 18 | 0 | SQR | 272 |
| 120 | 27 | 0 | SQR | 36 |
| 121 | 100 | 0 | SQR | 2 |
| 122 | 85 | 0 | SQR | 14 |
| 125 | 45 | 0 | SQR | 64 |
| 133 | 33 | 0 | SQR | 10 |

D codes

*Courtesy: PCB3D.COM*

# Gerber Files: Drill Files

CNC drill parameters used on the pcb fabricators system to drill and route the pcb.



NCD_78727-0122R06.rep - Notepad

File Edit Format Help

```
Drill Sizes Report
==================
Tool    Size    Pltd    Feed    speed    Qty
----    ----    ----    ----    -----    ---
   1      12       x      95      300    690
   2      15       x      95      300    197
   3      38       -     197      550      2
   4   46.85       x     139      550      2
   5      64       x      89      550      7
   6      67       -      89      550      1
   7      70       -      81      550      4
   8      94       x      66      550      1
   9      94       -      66      550      3
  10     205       -       0        0      1
```

NCD_78727-0122R06.lst - Notepad

File Edit Format Help

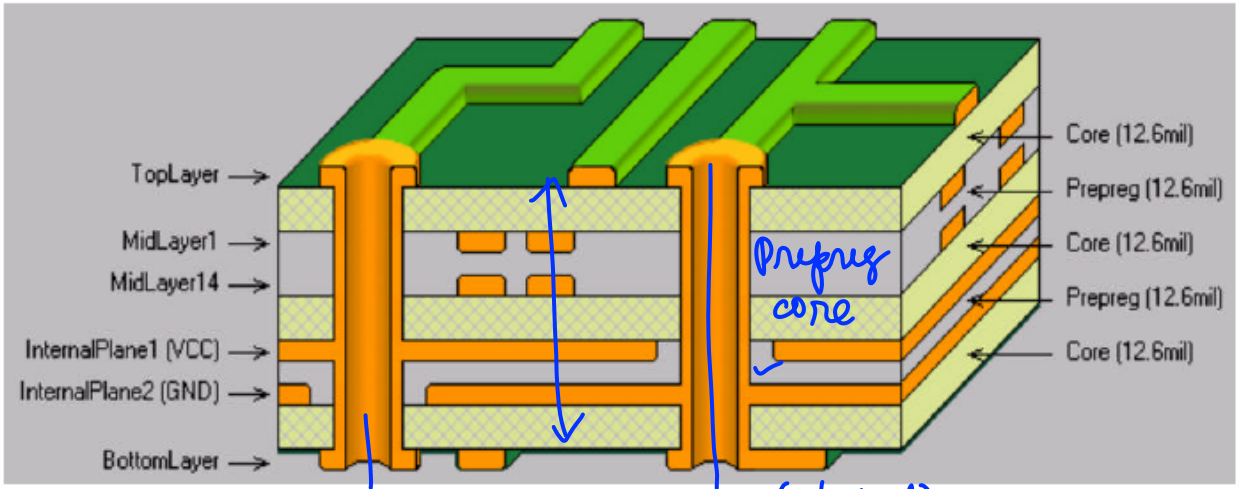
```
Drill Listing
=============
Drill: 12  Tool: 1  Feed: 95  speed: 300
X 132000  Y -47500
X 139500  Y -49500
X 143500  Y -49500
X 151500  Y -61500
X 151500  Y -65500
X 159500  Y -49500
X 159500  Y -62000
X 171500  Y -58000
X 182000  Y -60500
X 190500  Y -63000
X 190500  Y -58000
X 201000  Y -56000
X 201500  Y -66000
X 213000  Y -65000
X 213000  Y -59500
X 237000  Y -46000
X 265000  Y -43500
X 280500  Y -45000
X 281000  Y -57500
X 281000  Y -53000
X 284500  Y -65000
X 292000  Y -49000
X 296000  Y -45000
X 303000  Y -54000
X 312000  Y -61500
X 323000  Y -49000
X 330500  Y -65000
X 334500  Y -65000
X 334500  Y -54000
X 338500  Y -65000
X 342500  Y -65000
X 346500  Y -65000
X 348500  Y -45000
X 350500  Y -54500
X 350500  Y -65000
X 356145  Y -54173
X 363500  Y -56500
X 367500  Y -56500
X 371500  Y -56500
X 375500  Y -56500
X 380500  Y -48000
X 384500  Y -48000
```

*Courtesy: PCB3D.COM*

# PCB Fabrication

## PCB Basics

- Basic PCBs comprise a rigid sheet of epoxy-impregnated fiberglass material within copper sheets affixed to one or both sides. This is known as copper clad. In multilayer boards (those with more than two copper layers), a piece of material called prepreg is placed between core layers.




*Courtesy: PCB3D.COM*

NEXT CHAPTER:

**PRINTED WIRING BOARD TECHNOLOGIES**

# Photo tool (mask) generation

- Artwork, photomaster, phototool, mask
- CAD output in Gerber format (universal)
- X,Y table with light source
- Scanning, editing Gerber files
- Raster, Vector plotting equipment
- 4mil and 7mil Ag-halide film
- Photographic process
- Film stabilization

# **Photo plotted film** – The photo tool

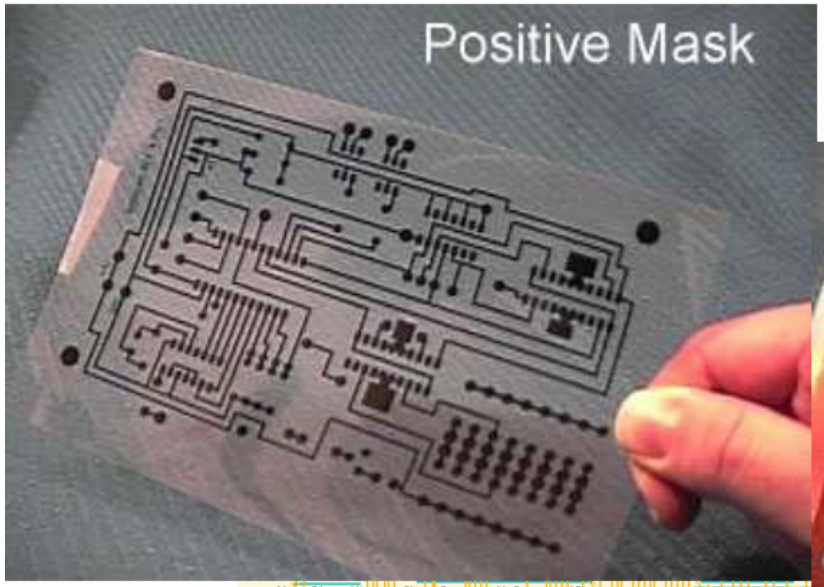
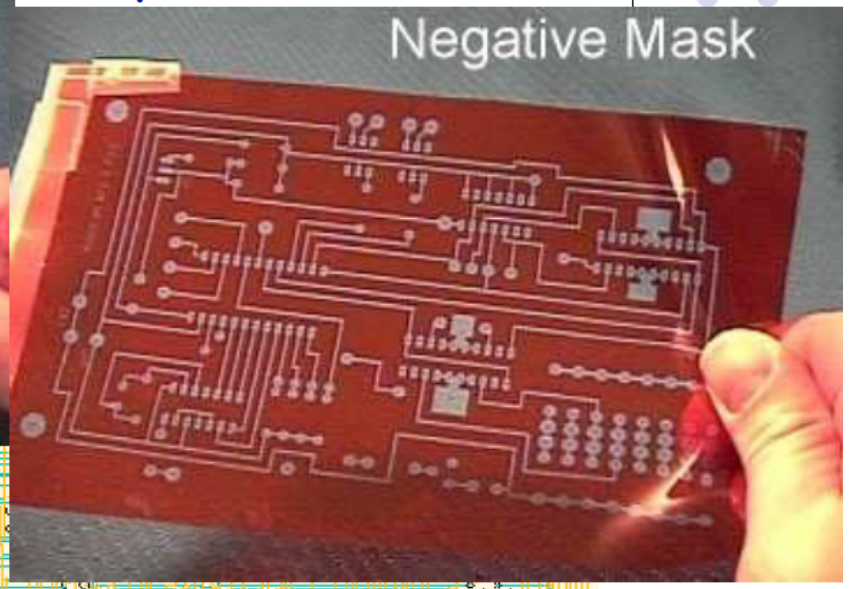



**Photo-tool is a delicate body**



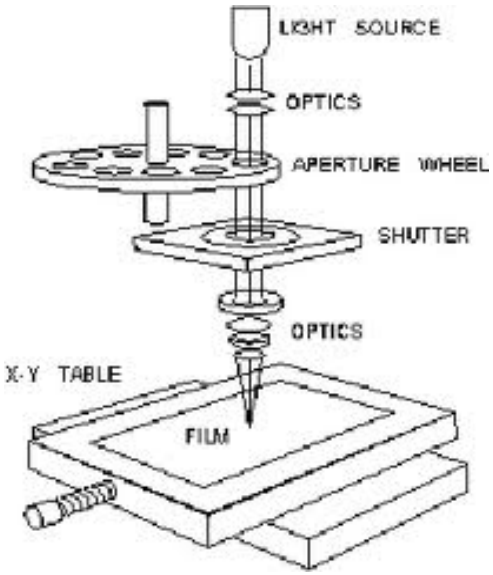

The board can be GOOD if the Phototool is good

(minus Manufacturing tolerances)

QUALITY CONTROL IS CRUCIAL TO CHECK TOLERANCE LEVELS

# Photoplotting equipment

- Photo plot on Silver halide films
- Use either 4 mil or 7 mil films but 7mil is preferred
- Gerber files are input data
- AutoCAD drawings are accepted
- Lithographic film used
- Large film sizes used  e.g. 32" x 28"
- Drum type; vacuum hold on film
- Multiple plots can be done
- Plots can be fitted to PCB panel size
- Scan and Edit of tech files possible
- Chemical processing follows plotting
- Stabilization in controlled conditions for at least 4-6h
- Laser plotters (raster) cost about Rs. 70 lakhs
- Resolution as high as 40000dpi
- Accuracy (positioning): +/- 2-4um
- Min line width 35 um; 25 um currently expensive
- Negative and positive masks can be plotted
- Other masks-  for Solder mask, silk screen
- Use red or mild-green safe lights for loading film
- Data transfer Protocol: Gerber, RS 274-X
- Light sources- different;
  Xenon-LCD Image projection technology
- Laser Direct Imaging is now becoming accepted
  Requires a compatible photoresist




*Vector photoplotter*

*Laser photoplotter*

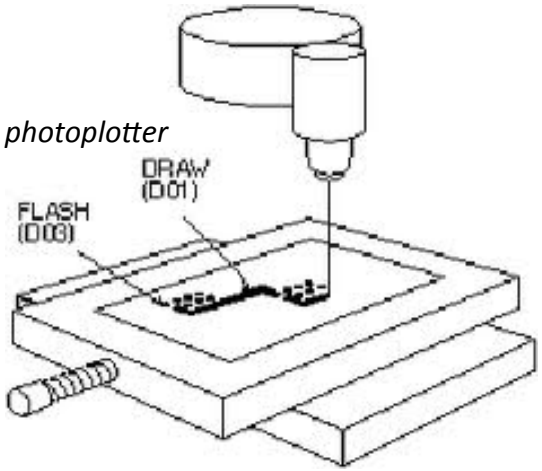
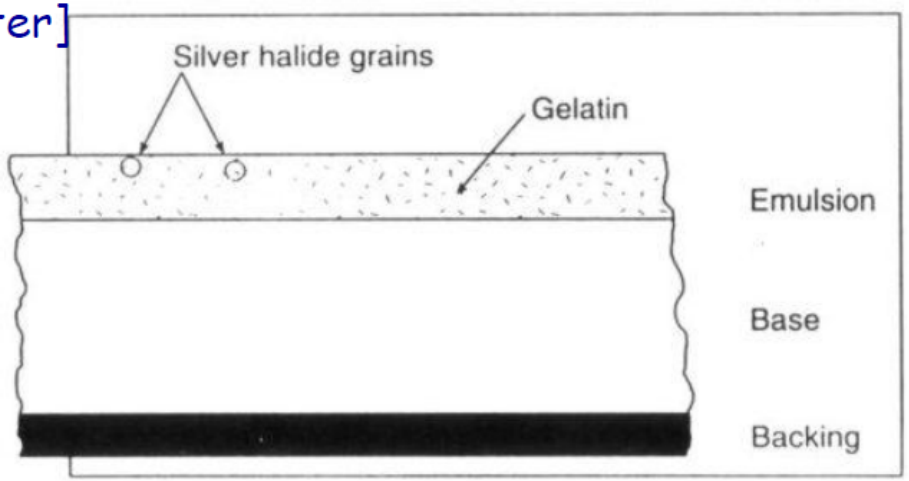



*Fig. source: everythingpcb.com*

# Structure of Photo film

1. Protective Layer
2. Emulsion [Silver Halide in Gelatin]
3. Sub layer [Adhesion Promoter]
4. Base [Polyester film]
5. Sub Layer
6. Backing
7. Light absorbing chemicals




Ag-X halide
Cl
Br
I

catalytic

Total thickness

100, 175 microns

# Silver halide photo tool

*handle carefully*

Possible Defects

- Pin holes ✓
- Scratches ✓
- Lift-off of flakes ✓
- Inadequate contrast ✓ Black & White
- No flatness

Di-azo films are used on shop floor

- Exposure
- Developing
  - Latent image made visible
    - Metol or Hydroquinone
  - Reducing action to metallic silver
  - Time and agitation important; concn. of solution
  - Orthochromatic or "Lith" films used
  - Safe lights for processing- red safe lights
- Stopper bath- 1% acetic acid solution
- Fixer bath
  - Sodium thiosulfate; permanently 'fixes' the image
- Wash, dry and stabilize
- Dimensional stability required; 4mil and 7mil films
- Diazo films- dry developing using ammonia
  - Exposed areas turn amber color on ammonia
  - Does cut off UV light as black silver halide- better registration
  - Available as 7mil film only- better handling in shop floor
  - Can be used for making multiple copies to avoid errors

*Recycling?*

# Basic Steps in Manufacture
# Single sided board

- Design
- Photo-tooling (1:1)
- Image/ Print — Cu surface of PWB / CCL
- Etch (unwanted Cu)
- Drill holes for component mounting
- Protect Cu (Solder)
- Solder mask
- Assemble (PTH)

# Double sided board manufacture

2-layer

- Design
- Photo-tooling (1:1)
- Drill holes (PTH)
- Plate (electroless)
- Image circuit
- Plate (Cu electroplate)
- Plate (Sn or Sn-Pb electroplate)
- Strip
- Etch
- Strip and Protect before assembly

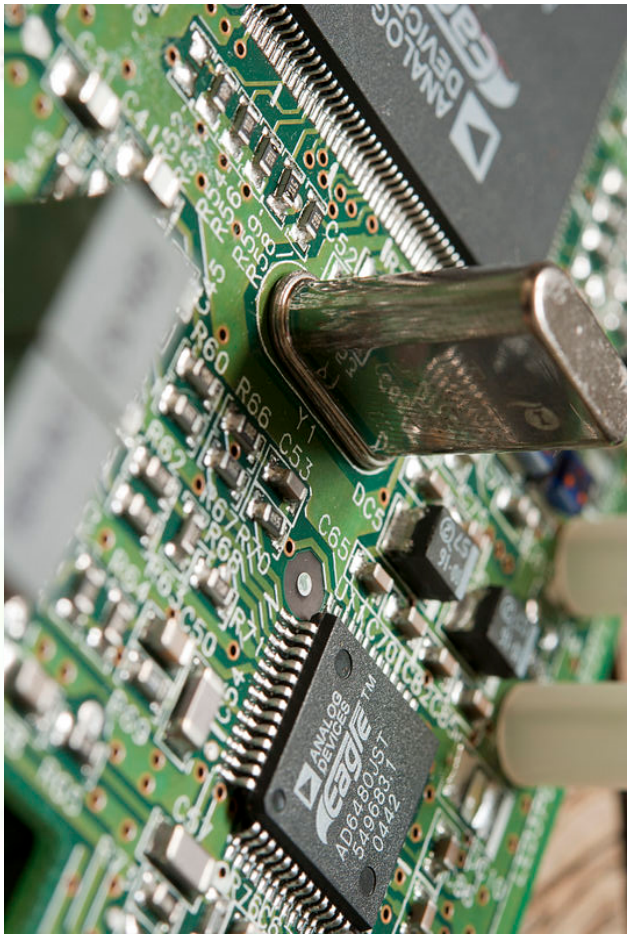


*Fig. source: Wikimedia Commons 2011*