Continuing..

PRINTED WIRING BOARD TECHNOLOGIES

Key advantages

- Photovia: Lowest cost due to parallel processing
- CO_2 laser: Fastest drill rate, any dielectric can be drilled, to open copper on the copper plane-need to switch to chemical or YAG
- *YAG laser: Copper can be drilled, smallest holes possible, any dielectric can be drilled
- Plasma: Very cost-effective parallel process, high yield, environmentally clean, almost any dielectric material can be processed

Yttrium aluminium garnet (YAG), $Y_3Al_2(AlO_4)_3$

Nd:YAG (neodymium-doped yttrium aluminium garnet); Nd:$Y_3Al_5O_{12}$

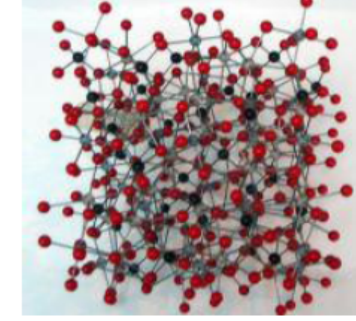


Fig. source: Garnet encyclopedia: www.absoluteastronomy.com

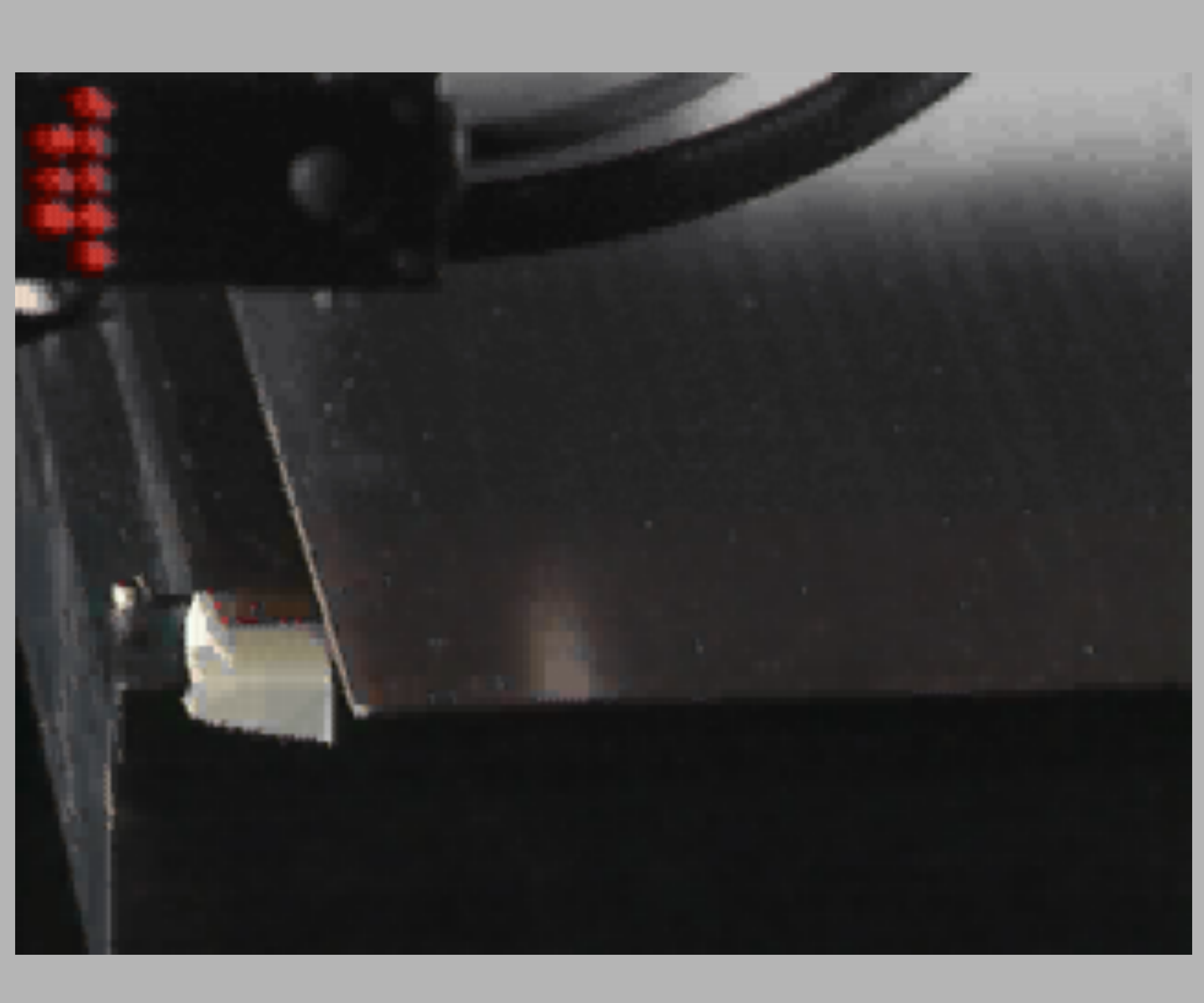


Fig. source: Mr SLN Murthy

LASER DRILLING

IBM's Surface Laminar Circuit

- Surface Laminar Circuit™: "An Organic Packaging Solution"
- SLC structure has two major parts
  - FR 4 substrate and
  - SLC layer built up (SBU technology)
- It is a methodology to have a PCB as a MCM-L and use existing PCB technologies

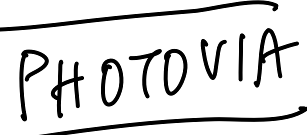
Outline

- Use of photo-polymer to build additional layers of dielectric on a normal PWB core
- Photo-imaging creates blind and buried vias
- Eliminates mechanical NC drilling
- Build up on both sides
- No glass fabric in the polymer; hence light and thin board
- 2-4 additional layers can be built
- Now referred to as SBU technology
  - Sequential Build-Up Technology

Features

- High density ~1998-Production
  - 1mil via
  - 1mil line and space
- SMT pads on blind photo via
- More design freedom, routing capability
- Ability to accommodate flip chip and bare die; hence classifies under MCM-L
- Used currently in video camcorders and telecommunication products

- PCMCIA Card
  - 0.7mm thick with 6 layers
  - 2 build up layers one side of a 4 layer FR4
  - FCA Chip 1:
    - 7.5mm square
  - FCA Chip 2
    - 4.0 x 10.8 mm square

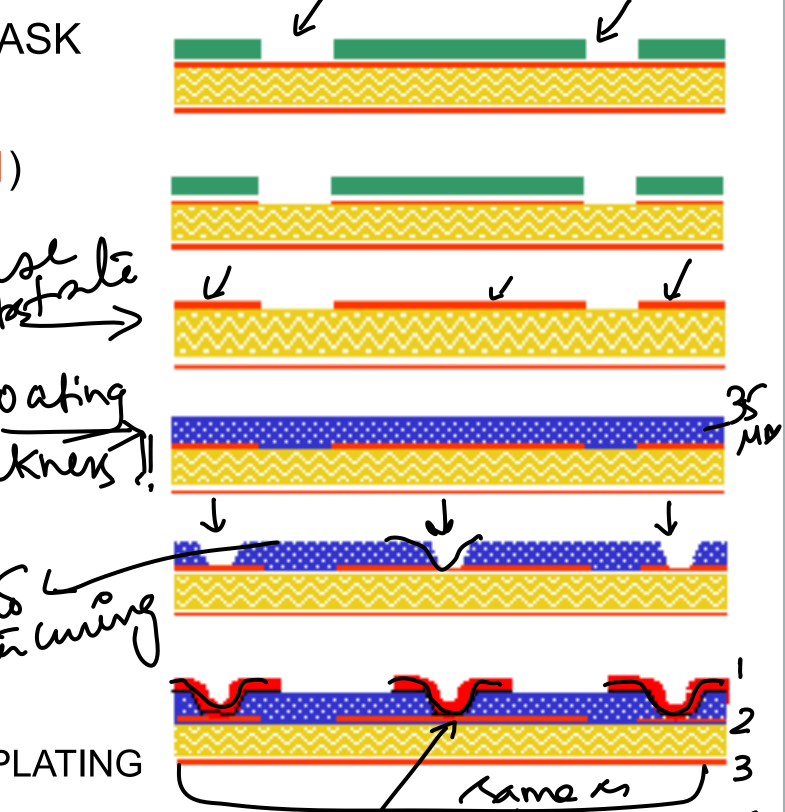


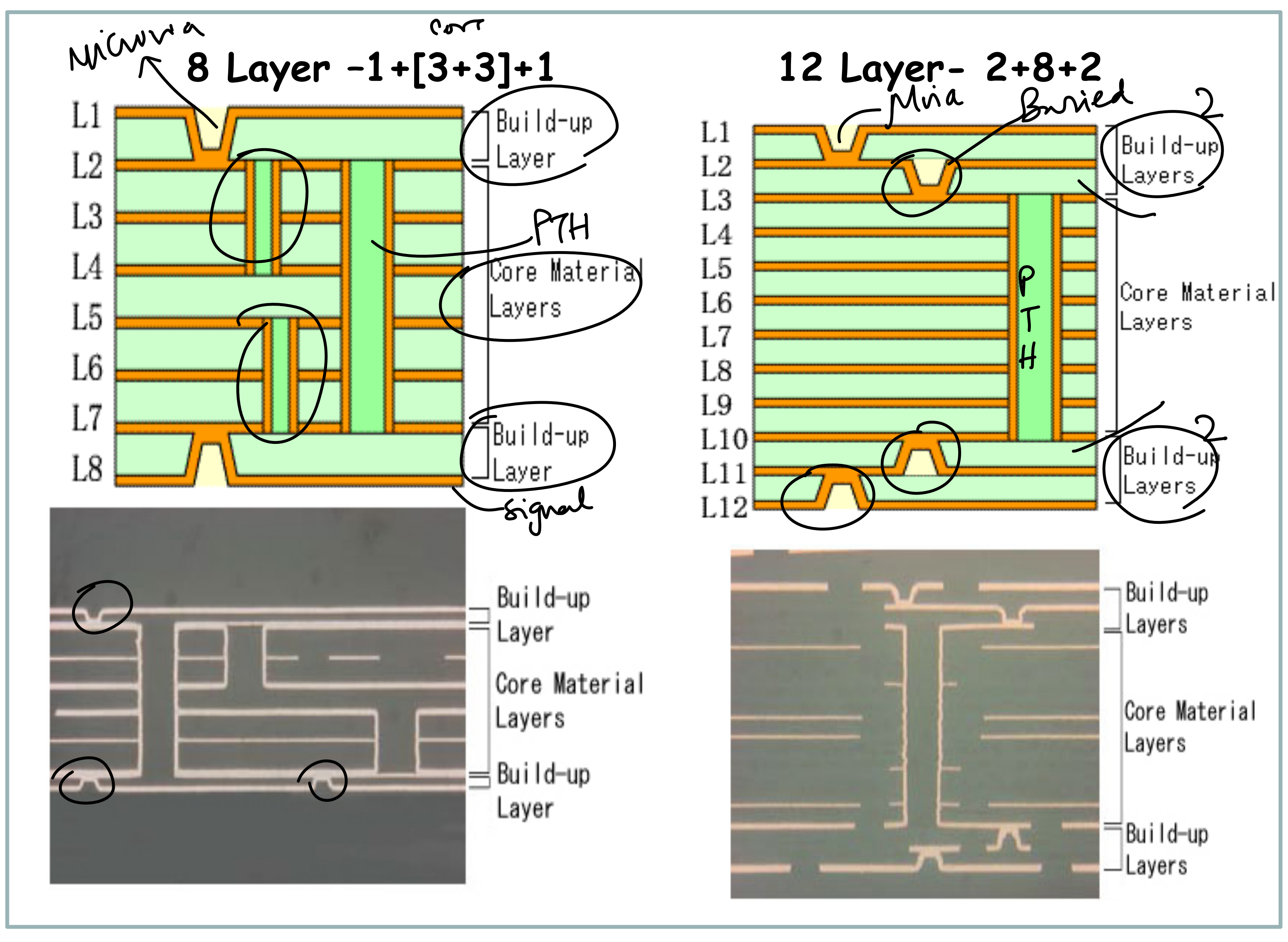
- Single chip BGA
  - 25mm square
  - 0.8mm thick with 6 layers
  - 1 build up layer on both sides of 4 layer FR4
  - FCA Chip:
    - 8.05 x 8.1 mm
    - smallest via ~90um

Source: Dr. Tsukada, IBM Yasu, Japan

1. CHOOSE SUBSTRATE; SURFACE PREPARATION
2. COAT PHOTORESIST AND PRE-BAKE
3. PHOTO-EXPOSE, DEVELOP, CURE USING MASK
4. SUB-ETCH COPPER LAYER (**LAYER 1**)
5. STRIP PHOTORESIST
6. APPLY PHOTO-POLYMER DIELECTRIC
7. PHOTO-EXPOSE, DEVELOP, FINAL CURE
8. METALLIZATION PROCESS
   - ELECTROLESS PLATING, ELECTROPLATING

(**LAYER 2**)




8 Layer -1+[3+3]+1
L1
L2
L3
L4
L5
L6
L7
L8
Build-up Layer
Core Material Layers
Build-up Layer
Build-up Layer
Core Material Layers
Build-up Layer
12 Layer- 2+8+2
L1
L2
L3
L4
L5
L6
L7
L8
L9
L10
L11
L12
Build-up Layers
Core Material Layers
Build-up Layers
Build-up Layers
Core Material Layers
Build-up Layers
PTH
Buried
signal
core
P T H

characteristic	photo-liquid	photo-film	laser-RCC	Laser-MP	plasma
dielectric cost	medium/high	high	high	medium/high	high
via size (lab)	50µm	100µm	75µm	100µm	100µm
line width	75	75	100	100	75
line space	75	75	100	100	85
via diameter in production	125	125	100	175	100
max via layers	3×2	1×2	1×2	8	4
dielectric thickness	40–80	60–80	60	100–250	50
dielectric thickness control	difficult	good	good	good	good
dielectric constant	3.8	3.8	3.8	3.5	3.5
glass transition temperature	130°C	170°C	170°C	170°C	170–200°C
process issues	pinholes	conformability	conformability	via filling	via shape
process issues	adhesion	adhesion	hole cleaning		non-uniform via
process issues	thickness control				slow process

Process	Company	Material	Lines/Spaces	Via/Land	Via Process Diameter
DV-Multi	**NEC**	Epoxy Film	80-50/ 80-50 µm	100/250 µm	Photo
IBSS	**Ibiden**	Epoxy Film	75-50/ 75-50 µm	150-100/ 250-150 µm	Photo
ALIVH	**Matsushita**	Aramid Epoxy	60/90	150/300 µm	Laser
PERL (Plasma Etched Rdistribution Layers)	**Hewlett-Packard** **HADCO** **Worldwiser**	Epoxy film PI/ Aramid	75/50 µm and 75/50 µm	125-90/250-1 65 µm>	Plasma Plasma/Laser
Build-up Substrate	**Fujitsu**	Epoxy	40/40 µm	90/140 µm	Photo
VB-2	**Victor**	Epoxy	10-95/100-75 µm	200-100/µm	Photo
B²IT	**Toshiba**	BT Laminate	90/90 µm	200/300 µm	Paste/Bump
Multi-Layer Build-Up	**Shinko**	Multiple	40/40 µm	50/110 µm	Laser/Photo
SLC (Surface Laminar Circuit)	**IBM Yasu**	Epoxy Liquid	75/50 µm anD	125-90/250-1 65 µm	Photo
Hitavia	**Hitachi**		100/100	200/500	
Viathin	**Sheldahl**	PI	50/37.5 µm	60-25/140-75 µm & 85/50/200-16 5 µm	Laser
ViaPly	**CTS**	PI/Aramid	75/75 µm	125/125 µm	Photo
TLPS	**Ormet**	PI	50/50 µm	25/200 µm	Photo
DYCOstrate	**Dyconex**	PI	100/125 µm	75/300 µm	Plasma

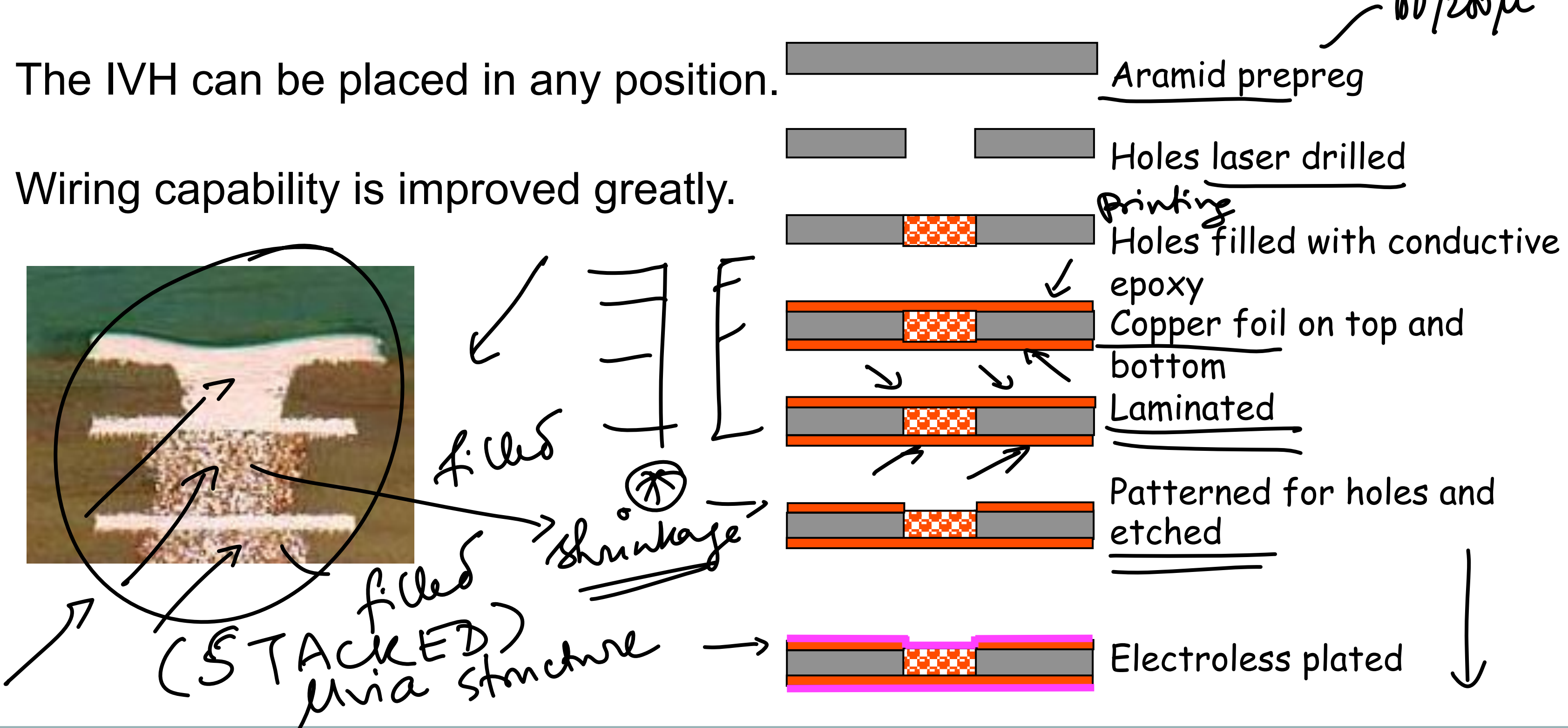
ALIVH Technology- an SBU methodology

ALIVH boards (Any Layer Interstitial (inner) Via Hole) needs no through-hole.

This is because any two layers are electrically connected by IVH (Interstitial Via Hole).

The IVH can be placed in any position.

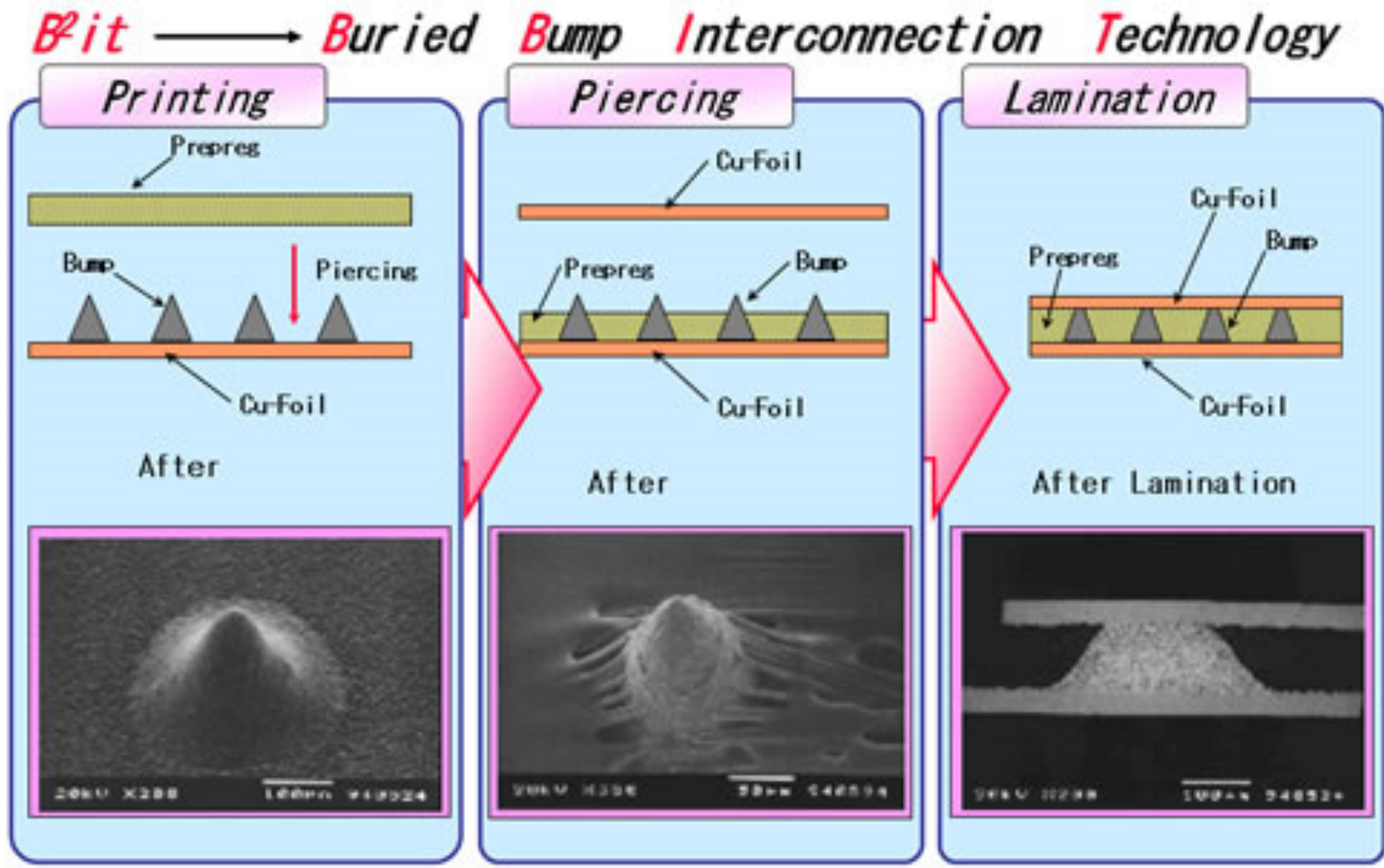
Wiring capability is improved greatly.



Via in Pad

Plated thorough hole (PTH) is filled by epoxy resin and plated by Cu as lid.
Via in Pad structure can save surface area for wiring enabling the PTH pad to be able to mount SMT devices.
Flow property of conductive epoxy or other resin crucial for minimal shrinkage and electrical contact between layers.
Minimum PTH diameter is 0.15mm, aspect ratio can be 8-10.

1. Provides a flat coplanar surface for component attachment
2. More traces on PCB escaping devices through rout channels
3. Increased component density due to absence of periphery vias
4. Potential EMI benefits due to lower inductance
5. Thermal dissipation (either at the lead joints or under devices by means of heat pipes
6. No via plugging by soldermask required at the component locations



B²IT is a Toshiba Process Technology

1. Conductive Ag bumps are printed on a sheet of Cu foil.
2. Prepreg is pierced through by the bumps
3. Another sheet of Cu is also laminated and a two sided B2IT board is manufactured.